Renesas Electronics America Inc - M30291FATHP#U3AAI1 Datasheet

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Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
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Quick Reference to Pages Classified by Address

Address	Register	Symbol	Page
0180_{16}			
0181_{16}			
0182_{16}			
0183_{16}			
0184_{16}			
0185_{16}			
0186_{16}			
$01B0_{16}$			
$01B1_{16}$			
$01B2_{16}$			
$01B3_{16}$	Flash memory control register 4 (Note 2)	FMR4	342
$01B4_{16}$			
$01B5_{16}$	Flash memory control register 1 (Note 2)	FMR1	341
$01B6_{16}$			
$01B7_{16}$	Flash memory control register 0 (Note 2)	FMR0	341
$01B8_{16}$			
$01B9_{16}$			
$01BA_{16}$			
$01BB_{16}$			
$01BC_{16}$			
0200_{16}	CAN0 message control register 0	C0MCTL0	292
0201_{16}	CAN0 message control register 1	C0MCTL1	292
0202_{16}	CAN0 message control register 2	C0MCTL2	292
0203_{16}	CAN0 message control register 3	C0MCTL3	292
0204_{16}	CAN0 message control register 4	C0MCTL4	292
0205_{16}	CAN0 message control register 5	C0MCTL5	292
0206_{16}	CAN0 message control register 6	C0MCTL6	292
0207_{16}	CAN0 message control register 7	C0MCTL7	292
0208_{16}	CAN0 message control register 8	C0MCTL8	292
0209_{16}	CAN0 message control register 9	C0MCTL9	292
$020A_{16}$	CAN0 message control register 10	C0MCTL10	292
$020B_{16}$	CAN0 message control register 11	C0MCTL11	292
$020C_{16}$	CAN0 message control register 12	C0MCTL12	292
$020D_{16}$	CAN0 message control register 13	C0MCTL13	292
$020E_{16}$	CAN0 message control register 14	C0MCTL14	292
$020F_{16}$	CAN0 message control register 15	C0MCTL15	292
0210_{16} 0211_{16}	CAN0 control register	C0CTLR	293
0212_{16} 0213_{16}	CAN0 status register	C0STR	294
0214_{16} 0215_{16}	CAN0 slot status register	C0SSTR	295
0216_{16} 0217_{16}	CAN 0 interrupt control register	C0ICR	296
0218_{16} 0219_{16}	CAN0 extended ID register	C0IDR	296
$021A_{16}$ $021B_{16}$	CAN0 configuration register	C0CONR	297
$021C_{16}$	CAN0 receive error count register	C0RECR	298
$021D_{16}$	CAN0 transmit error count register	C0TECR	298
$021E_{16}$ $021F_{16}$	CAN0 time stamp register	C0TSR	299
0210_{16}			
$02FE_{16}$			
$02FF_{16}$			

Address	Register	Symbol	Page
0240_{16}			
0241_{16}			
0242_{16} 0243_{16}	CAN0 acceptance filter support register	C0AFS	299
0244_{16}			
0245_{16}			
0246_{16}			
0247_{16}			
0248_{16}			
0249_{16}			
$024A_{16}$			
$024C_{16}$			
$024D_{16}$			
$024E_{16}$			
$024F_{16}$			
0250_{16}			
0251_{16}			
0252_{16}			
0253_{16}			
0254_{16}			
0255_{16}			
0256_{16}			
0257_{16}			
0258_{16}			
0259_{16}			
$025A_{16}$	Three-phase protect control register	TPRC	139
$025B_{16}$			
$025C_{16}$	0n-chip oscillator control register	ROCR	50
$025D_{16}$	Pin assignment control register	PACR	177, 326
$025E_{16}$	Peripheral clock select register	PCLKR	52
$025F_{16}$	CAN0 clock select register	CCLKR	53
$02E0_{16}$	I^{2}C0 data shift register	S00	258
$02E1_{16}$			
$02E2_{16}$	I^{2}C0 address register	S0D0	257
$02E3_{16}$	I^{2}C0 control register 0	S1D0	259
$02E4_{16}$	I^{2}C0 clock control register	S20	258
$02E5_{16}$	I^{2}C0 start/stop condition control register	S2D0	263
$02E6_{16}$	I^{2}C0 control register 1	S3D0	261
$02E7_{16}$	I^{2}C0 control register 2	S4D0	262
$02E8_{16}$	I^{2}C0 status register	S10	260
$02E9_{16}$			
$02EA_{16}$			
$02FE_{16}$			
$02FF_{16}$			

Note 1: The blank areas are reserved and cannot be accessed by users.
Note 2: This register is included in the flash memory version.

Table 1.5 Product List (3) -V Version **As of March, 2007**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30290FAVHP	96 K + 4 K	8 K	PLQP0080KB-A (80P6Q-A)	Flash Memory	U3, U5, U7, U9
M30290FCVHP	128 K + 4 K	12 K			
M30291FAVHP	96 K + 4 K	8 K	PLQP0064KB-A (64P6Q-A)		
M30291FCVHP	128 K + 4 K	12 K			
M30290M8V-XXXHP	64 K	4 K	PLQP0080KB-A (80P6Q-A)	Mask ROM	U0
M30290MAV-XXXHP	96 K	8 K			
M30290MCV-XXXHP	128 K	12 K			
M30291M8V-XXXHP	64 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30291MAV-XXXHP	96 K	8 K			
M30291MCV-XXXHP	128 K	12 K			

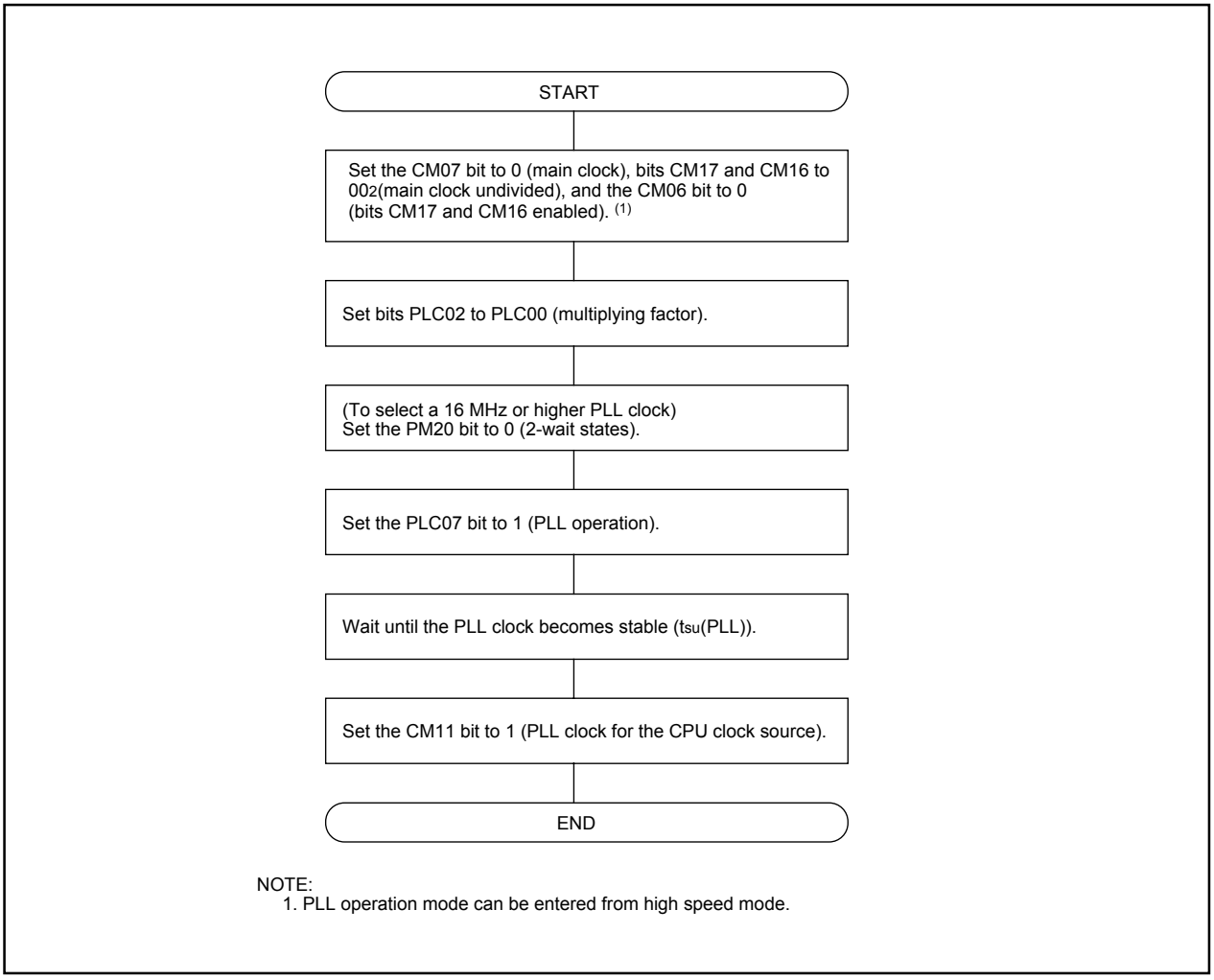


Figure 7.10 Procedure to Use PLL Clock as CPU Clock Source

Figure 7.11 shows the state transition from normal operation mode to stop mode and wait mode. **Figure 7.12** shows the state transition in normal operation mode.

Table 7.7 shows a state transition matrix describing allowed transition and setting. The vertical line shows current state and horizontal line shows state after transition.

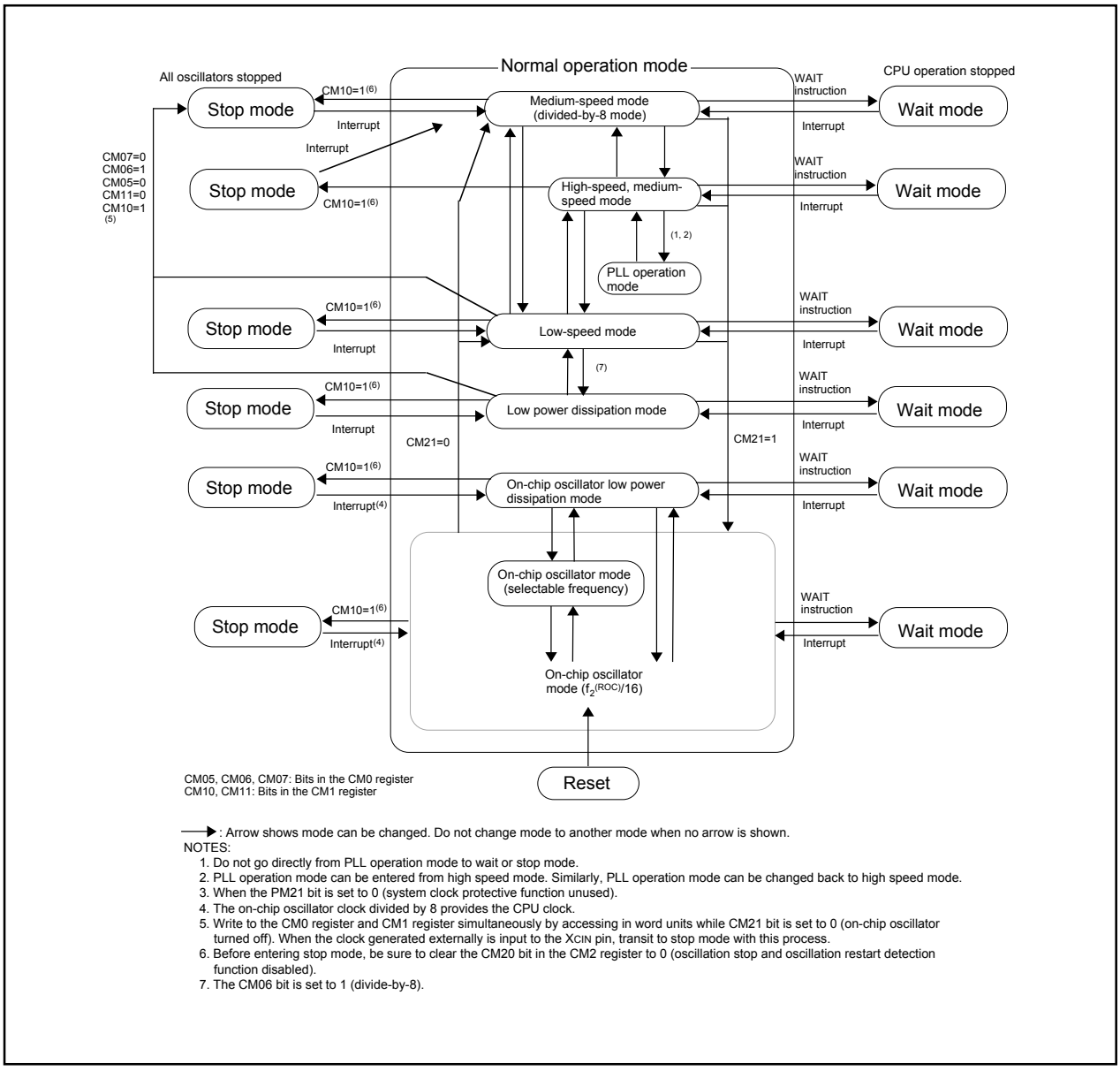


Figure 7.11 State Transition to Stop Mode and Wait Mode

9.3.1 I Flag

The I flag enables or disables the maskable interrupt. Setting the I flag to 1 (= enabled) enables the maskable interrupt. Setting the I flag to 0 (= disabled) disables all maskable interrupts.

9.3.2 IR Bit

The IR bit is set to 1 (= interrupt requested) when an interrupt request is generated. Then, when the interrupt request is accepted and the CPU branches to the corresponding interrupt vector, the IR bit is cleared to 0 (= interrupt not requested).
The IR bit can be cleared to 0 in a program. Note that do not write 1 to this bit.

9.3.3 ILVL2 to ILVL0 Bits and IPL

Interrupt priority levels can be set using bits ILVL2 to ILVL0.
Table 9.3 shows the settings of interrupt priority levels and **Table 9.4** shows the interrupt priority levels enabled by the IPL.

The following are conditions under which an interrupt is accepted:
· I flag = 1
· IR bit = 1
· interrupt priority level > IPL

The I flag, IR bit, bits ILVL2 to ILVL0, and IPL are independent of each other. In no case do they affect one another.

Table 9.3 Settings of Interrupt Priority Levels

ILVL2 to ILVL0 bits	Interrupt priority level	Priority order
000_2	Level 0 (interrupt disabled)	———
001_2	Level 1	Low ↓
010_2	Level 2	
011_2	Level 3	
100_2	Level 4	
101_2	Level 5	
110_2	Level 6	
111_2	Level 7	High

Table 9.4 Interrupt Priority Levels Enabled by IPL

IPL	Enabled interrupt priority levels
000_2	Interrupt levels 1 and above are enabled
001_2	Interrupt levels 2 and above are enabled
010_2	Interrupt levels 3 and above are enabled
011_2	Interrupt levels 4 and above are enabled
100_2	Interrupt levels 5 and above are enabled
101_2	Interrupt levels 6 and above are enabled
110_2	Interrupt levels 7 and above are enabled
111_2	All maskable interrupts are disabled

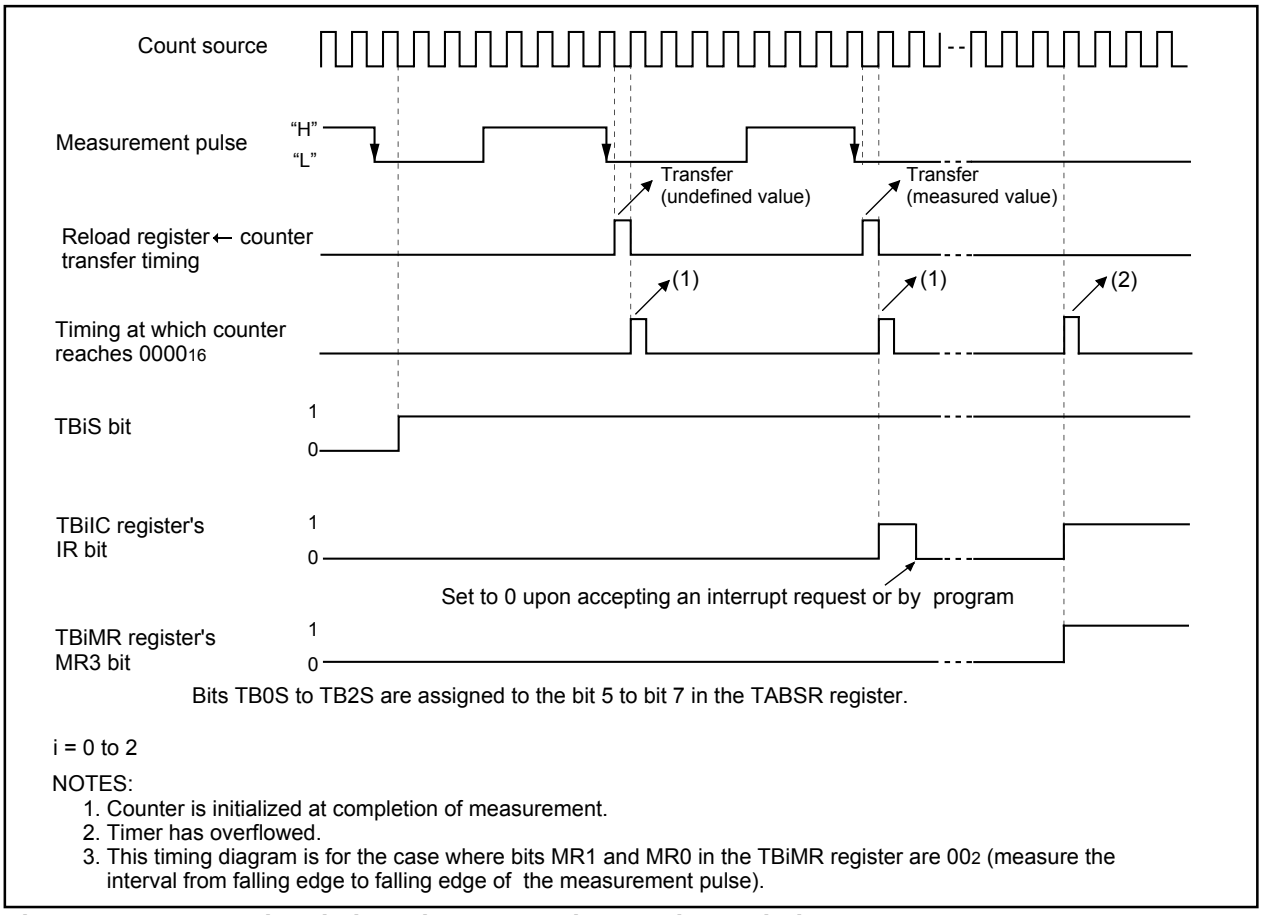


Figure 12.21 Operation timing when measuring a pulse period

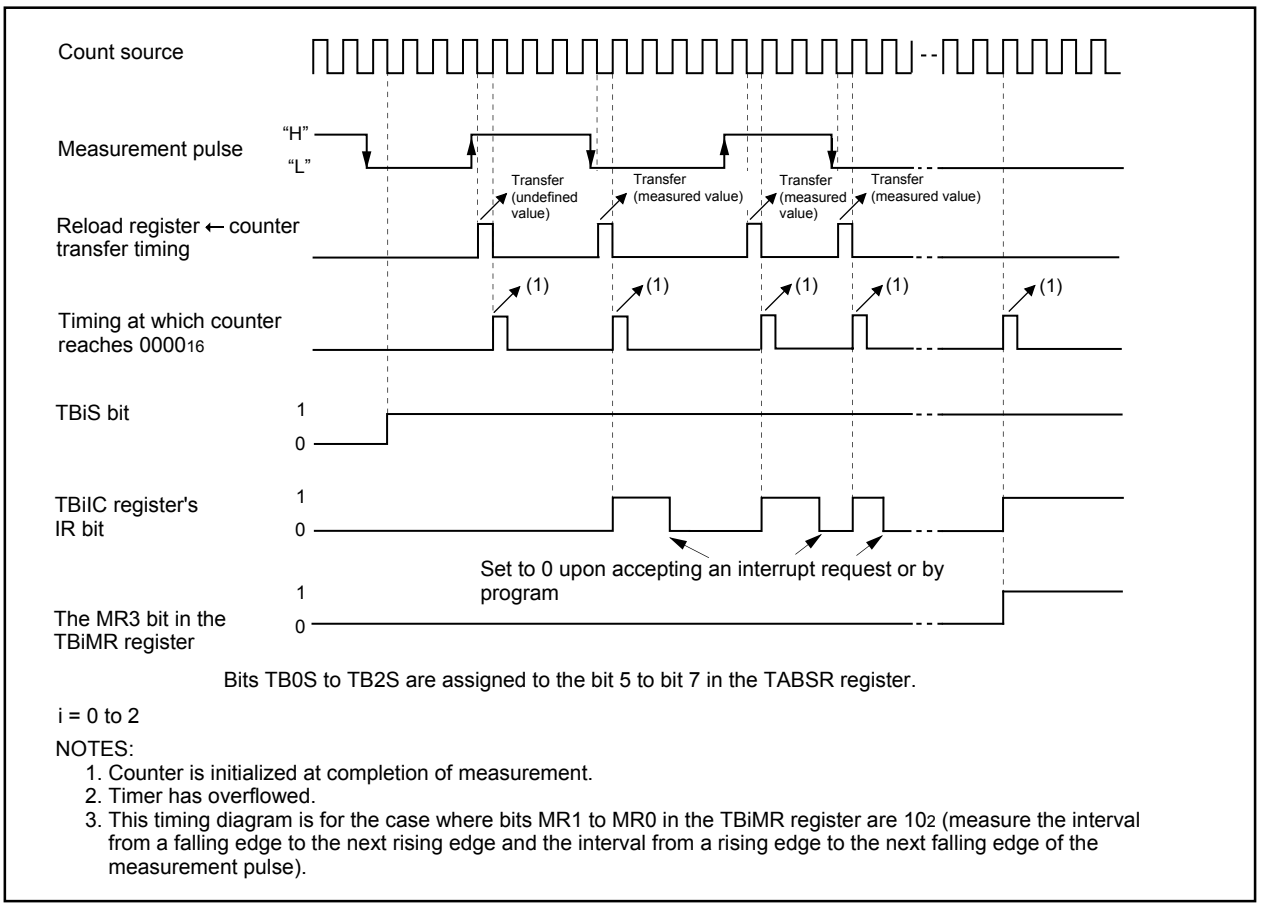


Figure 12.22 Operation timing when measuring a pulse width

Three-phase PWM Control Register 0 (1)

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
INVC0	034816	0016

Bit Symbol	Bit Name	Function	RW
INV00	Effective interrupt output polarity select bit(3)	0: ICTB2 counter is incremented by 1 on the rising edge of timer A1 reload control signal 1: ICTB2 counter is incremented by 1 on the falling edge of timer A1 reload control signal	RW
INV01	Effective interrupt output specification bit(2, 3)	0: ICTB2 counter incremented by 1 at a timer B2 underflow 1: Selected by INV00 bit	RW
INV02	Mode select bit(4)	0: Three-phase motor control timer function unused 1: Three-phase motor control timer function (5)	RW
INV03	Output control bit(6)	0: Three-phase motor control timer output disabled (5) 1: Three-phase motor control timer output enabled	RW
INV04	Positive and negative phases concurrent output disable bit	0: Simultaneous active output enabled 1: Simultaneous active output disabled	RW
INV05	Positive and negative phases concurrent output detect flag	0: Not detected yet 1: Already detected (7)	RW
INV06	Modulation mode select bit(8)	0: Triangular wave modulation mode 1: Sawtooth wave modulation mode (9)	RW
INV07	Software trigger select bit	Setting this bit to 1 generates a transfer trigger. If the INV06 bit is 1, a trigger for the dead time timer is also generated. The value of this bit when read is 0	RW

NOTES:

1. Write to this register after setting the PRC1 bit in the PRCR register to 1 (write enable). Note also that bits INV00 to INV02, bits INV04 and INV06 can only be rewritten when timers A1, A2, A4 and B2 are idle.
2. If this bit needs to be set to 1, set any value in the ICTB2 register before writing to it.
3. Effective when the INV11 bit in the INV1 register is 1 (three-phase mode 1). If INV11 is set to 0 (three-phase mode 0), the ICTB2 counter is incremented by 1 each time the timer B2 underflows, regardless of whether the INV00 and INV01 bits are set. When setting the INV01 bit to 1, the first interrupt is generated when the timer B2 underflows n-1 times, if n is the value set in the ICTB2 counter. Subsequent interrupts are generated every n times the timer B2 underflow.
4. Setting the INV02 bit to 1 activates the dead time timer, U/V/W-phase output control circuits and ICTB2 counter.
5. When the INV02 bit is set to 1 and the INV03 bit is set to 0, $\overline{U}$, U, $\overline{V}$, V, $\overline{W}$, W pins, including pins shared with other output functions, enter a high-impedance state. When INV03 is set to 1, U/V/W corresponding pins generate the three-phase PWM output.
6. The INV03 bit is set to 0 in the following cases:
   - When reset
   - When positive and negative go active (INV05 = 1) simultaneously while INV04 bit is 1
   - When set to 0 by program
   - When input on the $\overline{SD}$ pin changes state from “H” to “L” regardless of the value of the INVCR1 bit. (The INV03 bit cannot be set to 1 when $\overline{SD}$ input is “L”.) INV03 is set to 0 when both bits INV05 and INV04 are set to 1.

Item	INV06=0	INV06=1
Mode	Triangular wave modulation mode	Sawtooth wave modulation mode
Timing at which transferred from registers IDB0 to IDB1 to three-phase output shift register	Transferred only once synchronously with the transfer trigger after writing to registers IDB0 to IDB1	Transferred every transfer trigger
Timing at which dead time timer trigger is generated when INV16 bit is 0	Synchronous with the falling edge of timer A1, A2, or A4 one-shot pulse	Synchronous with the transfer trigger and the falling edge of timer A1, A2, or A4 one-shot pulse
INV13 bit	Effective when INV11 is set to 1 and INV06 is set to 0	No effect

Transfer trigger: Timer B2 underflow, write to the INV07 bit or write to the TB2 register when the INV10 bit is set to 1.

9: If the INV06 bit is set to 1, set the INV11 bit to 0 (three-phase mode 0) and set the PWCON bit to 0 (timer B2 reloaded by a timer B2 underflow)

10. When the PFCi (i = 0 to 5) bit in the PFCR register is set to 1 (three-phase PWM output), individual pins are enabled to output.

Figure 12.26 INVC0 Register

12.3.2 Three-phase/Port Output Switch Function

When the INVC03 bit in the INVC0 register set to 1 (Timer output enabled for three-phase motor control) and setting the PFCi (i=0 to 5) in the PFCR register to 0 (I/O port), the three-phase PWM output pin (U, $\overline{U}$, V, $\overline{V}$, W and $\overline{W}$) functions as I/O port. Each bit of the PFCi bits (i=0 to 5) is applicable for each one of three-phase PWM output pins. **Figure 12.37** shows the example of three-phase/port output switch function. **Figure 12.38** shows the PFCR register and the three-phase protect control register.

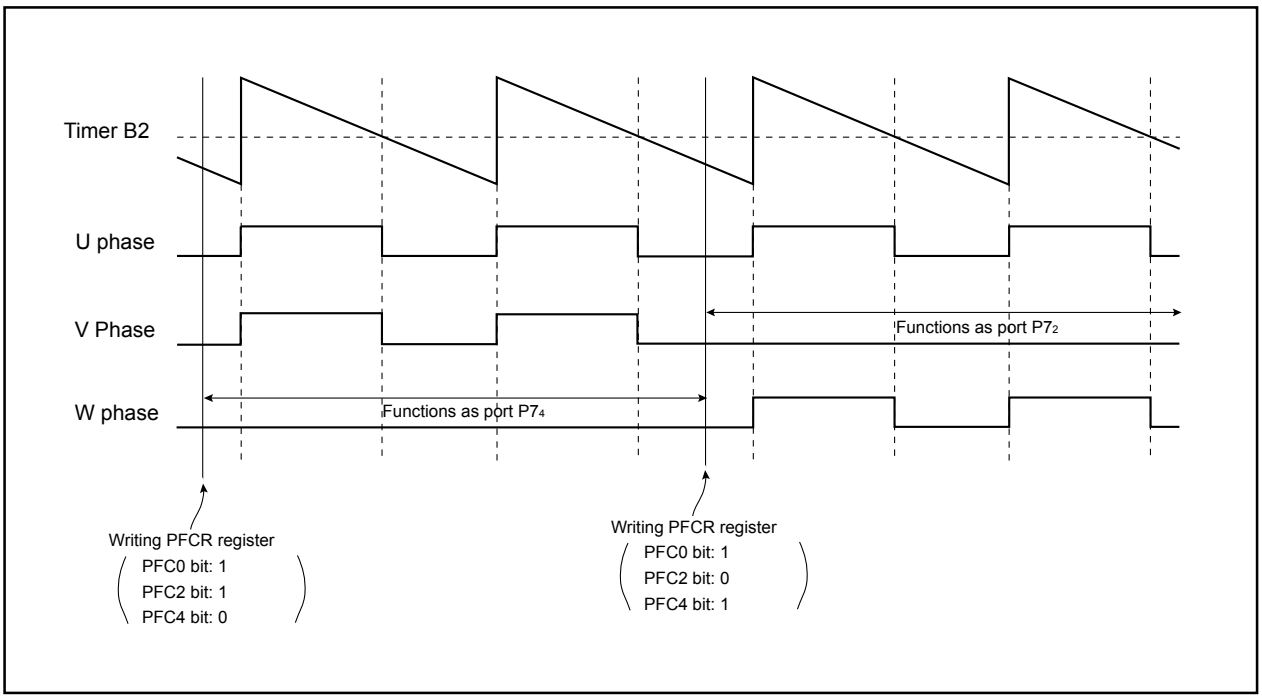


Figure 12.37 Usage Example of Three-phse/Port Output Switch Function

13.1.1 Base Timer Reset Register(G1BTRR)

The G1BTRR register provides the capability to reset the base timer when the base timer count value matches the value stored in the G1BTRR register. The G1BTRR register is enabled by the RST4 bit in the G1BCR0 register. This function is identical in operation to the G1PO0 base timer reset that is enabled by the RST1 bit in the G1BCR0 reigster. If the free-running operation is not selected, the channel 0 can be used for a waveform generation when the base timer is reset by the G1BTRR register. Do not enable bits RST1 and RST4 simultaneously.

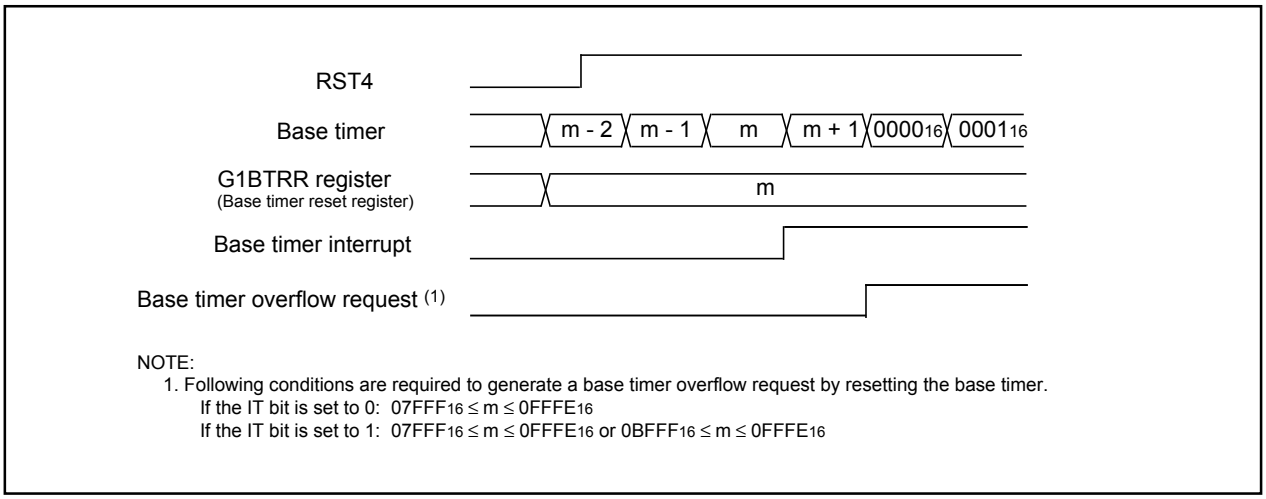


Figure 13.15 Base Timer Reset operation by Base Timer Reset Register

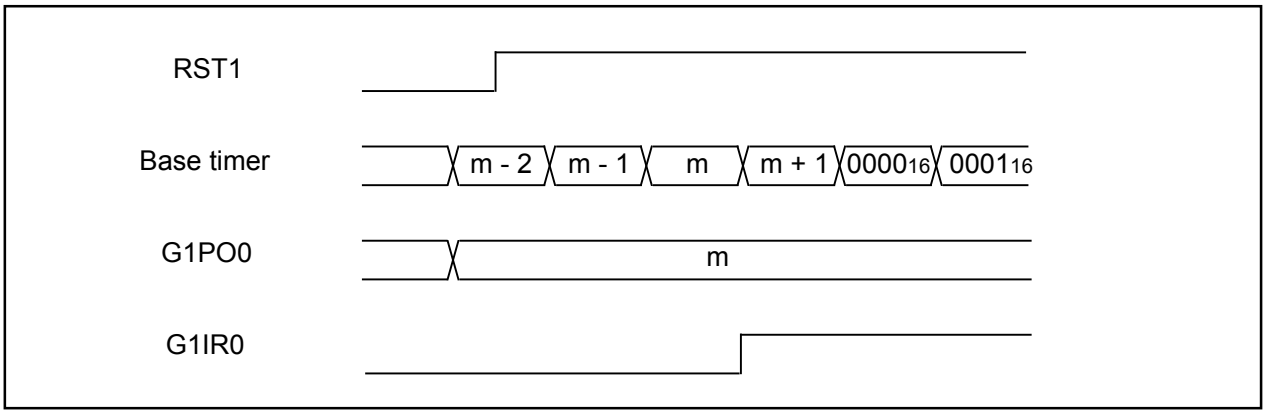


Figure 13.16 Base Timer Reset operation by G1PO0 register

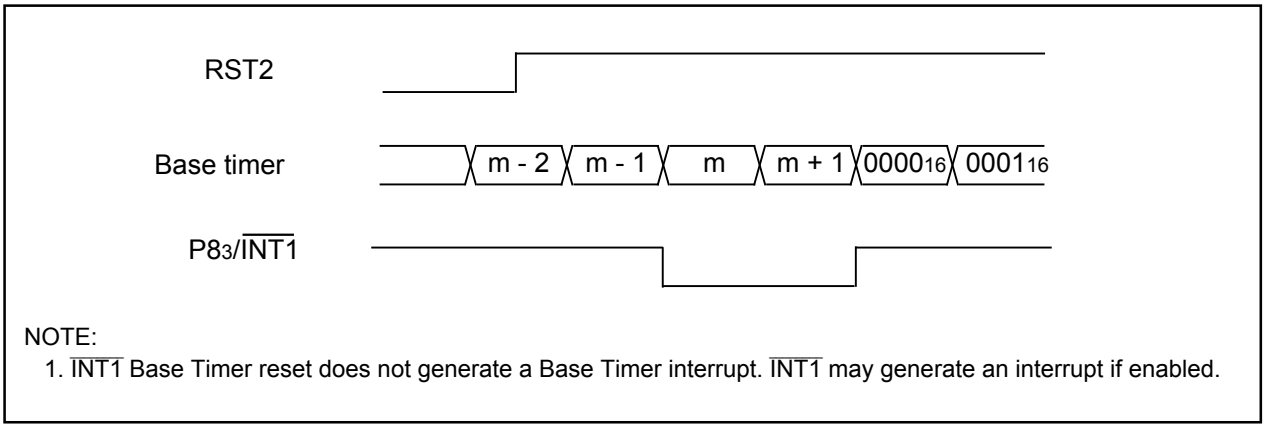


Figure 13.17 Base Timer Reset operation by $\overline{INT1}$

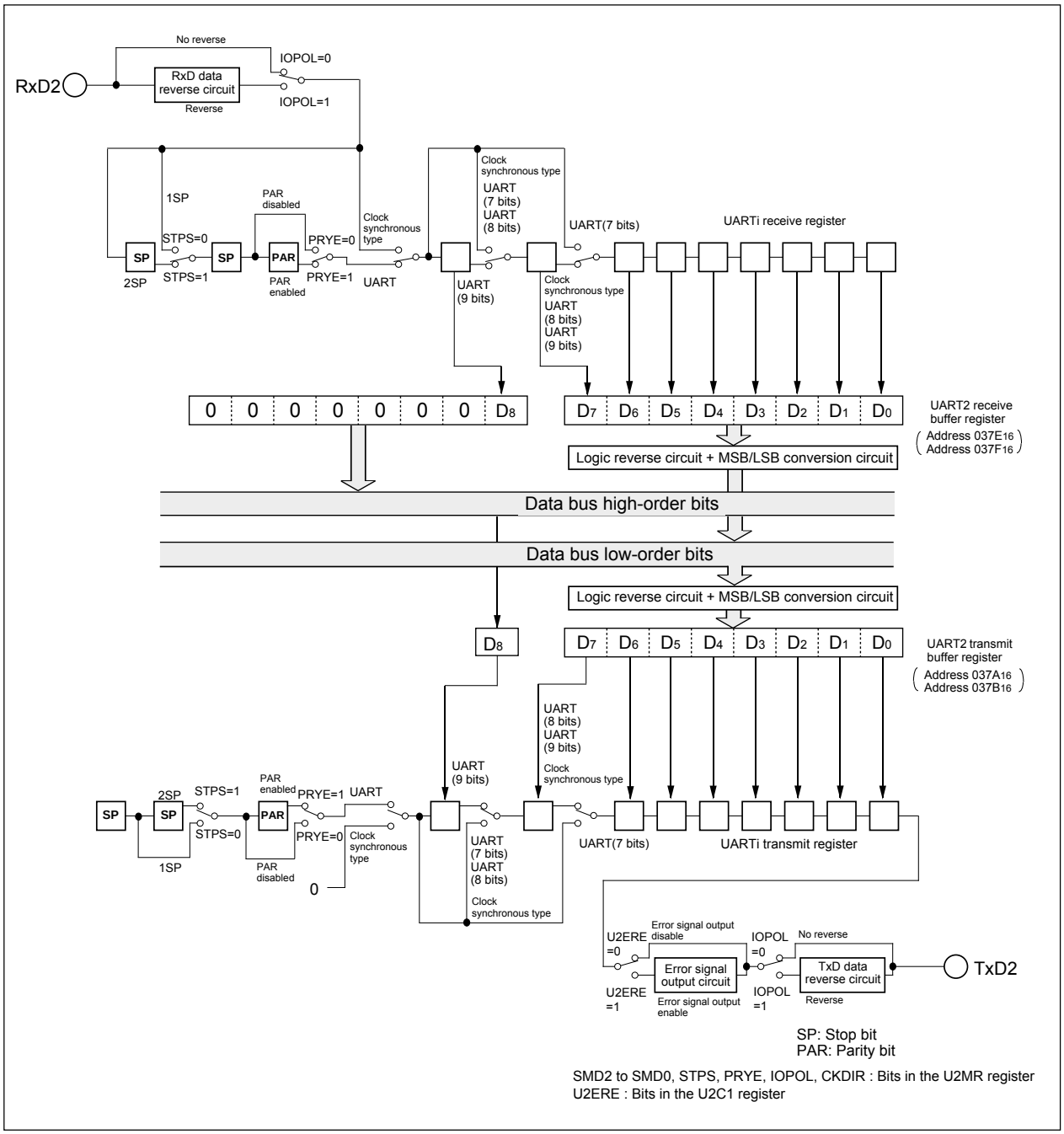


Figure 14.3 Block diagram of UART2 transmit/receive unit

14.1.2.4 Serial Data Logic Switching Function (UART2)

The data written to the U2TB register has its logic reversed before being transmitted. Similarly, the received data has its logic reversed when read from the U2RB register. **Figure 14.19** shows serial data logic.

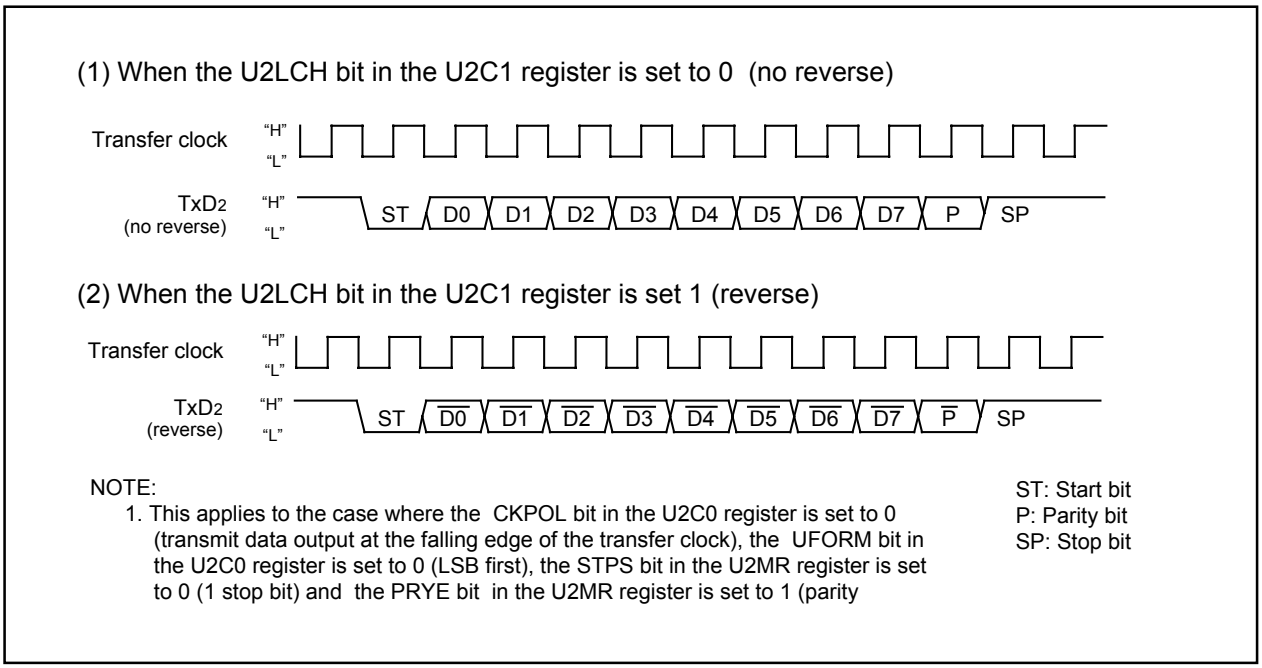


Figure 14.19 Serial Data Logic Switching

14.1.2.5 TxD and RxD I/O Polarity Inverse Function (UART2)

This function inverses the polarities of the TxD2 pin output and RxD2 pin input. The logic levels of all input/output data (including the start, stop and parity bits) are inversed. **Figure 14.20** shows the TxD pin output and RxD pin input polarity inverse.

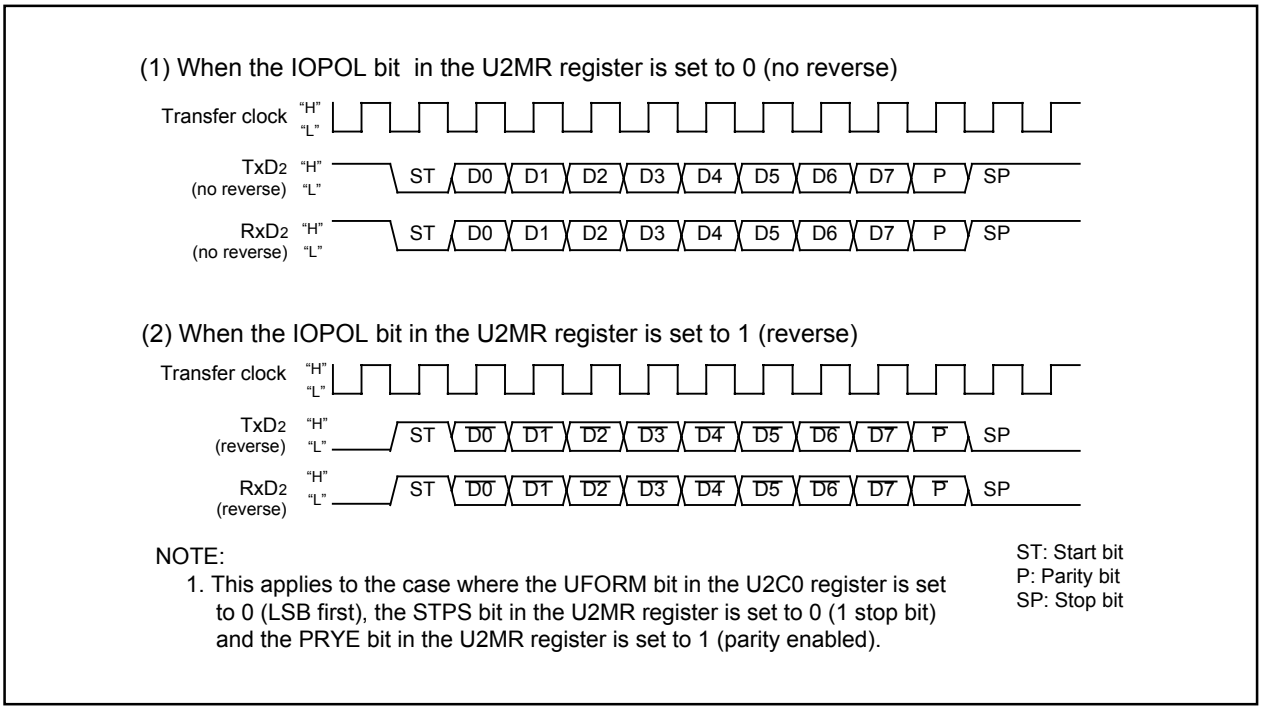


Figure 14.20 TxD and RxD I/O Polarity Inverse

15.1.7 Delayed Trigger Mode 0

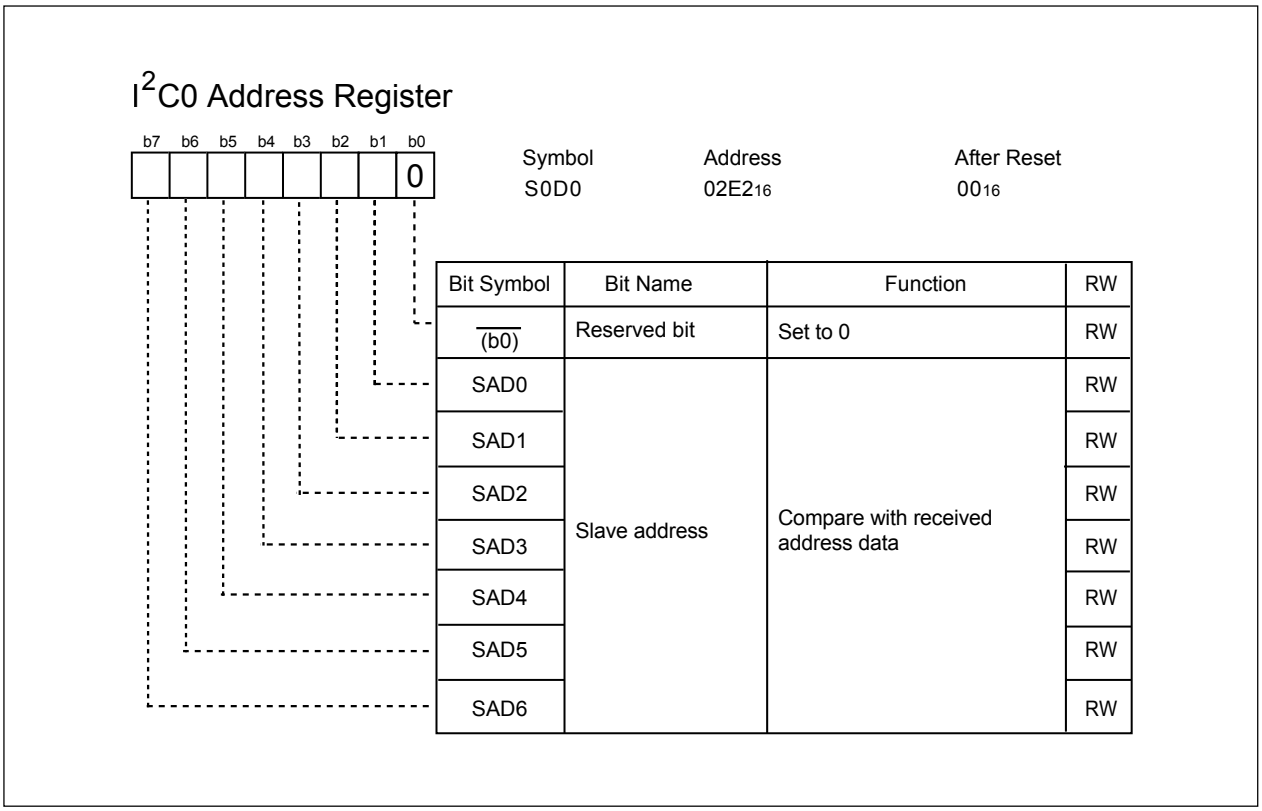
In delayed trigger mode 0, analog voltages applied to the selected pins are converted one-by-one to a digital code. The delayed trigger mode 0 used in combination with A/D trigger mode of Timer B. The Timer B0 underflow starts a single sweep conversion. After completing the AN_0 pin conversion, the AN_1 pin is not sampled and converted until the Timer B1 underflow is generated. When the Timer B1 underflow is generated, the single sweep conversion is restarted with the AN_1 pin. **Table 15.10** shows the delayed trigger mode 0 specifications. **Figure 15.19** shows the operation example in delayed trigger mode 0. **Figures 15.20** and **15.21** show each flag operation in the ADSTAT0 register that corresponds to the operation example. **Figure 15.22** shows registers ADCON0 to ADCON2 in delayed trigger mode 0. **Figure 15.23** shows the ADTRGCON register in delayed trigger mode 0 and **Table 15.11** shows the trigger select bit setting in delayed trigger mode 0.

Table 15.10 Delayed Trigger Mode 0 Specifications

Item	Specification
Function	Bits SCAN1 and SCAN0 in the ADCON1 register and bits ADGSEL1 and ADGSEL0 in the ADCON2 register select pins. Analog voltage applied to the input voltage of the selected pins are converted one-by-one to the digital code. At this time, timer B0 underflow generation starts AN_0 pin conversion. Timer B1 underflow generation starts conversion after the AN_1 pin. (1)
A/D Conversion Start	AN_0 pin conversion start condition •When Timer B0 underflow is generated if Timer B0 underflow is generated again before Timer B1 underflow is generated , the conversion is not affected •When Timer B0 underflow is generated during A/D conversion of pins after the AN_1 pin, conversion is halted and the sweep is restarted from the AN_0 pin again AN_1 pin conversion start condition •When Timer B1 underflow is generated during A/D conversion of the AN_0 pin, the input voltage of the AN_1 pin is sampled. The AN_1 conversion and the rest of the sweep start when AN_0 conversion is completed.
A/D Conversion Stop Condition	•When single sweep conversion from the AN_0 pin is completed •Set the ADST bit to 0 (A/D conversion halted)(2)
Interrupt request generation timing	A/D conversion completed
Analog input pin	Select from AN_0 to AN_1 (2 pins), AN_0 to AN_3 (4 pins), AN_0 to AN_5 (6 pins) and AN_0 to AN_7 (8 pins)(3)
Readout of A/D conversion result	Readout one of registers AN0 to AN7 that corresponds to the selected pins

NOTES:

1. Set the larger value than the value of the timer B0 register to the timer B1 register. The count source for timer B0 and timer B1 must be the same.
2. Do not write 1 (A/D conversion started) to the ADST bit in delayed trigger mode 0. When write 1, unexpected interrupts may be generated.
3. $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, and $AN3_0$ to $AN3_2$ can be used in the same way as AN_0 to AN_7. However, all input pins need to belong to the same group.



Bit Symbol	Bit Name	Function	RW
$\overline{(b0)}$	Reserved bit	Set to 0	RW
SAD0	Slave address	Compare with received address data	RW
SAD1			RW
SAD2			RW
SAD3			RW
SAD4			RW
SAD5			RW
SAD6			RW

Figure 16.2 S0D0 Register

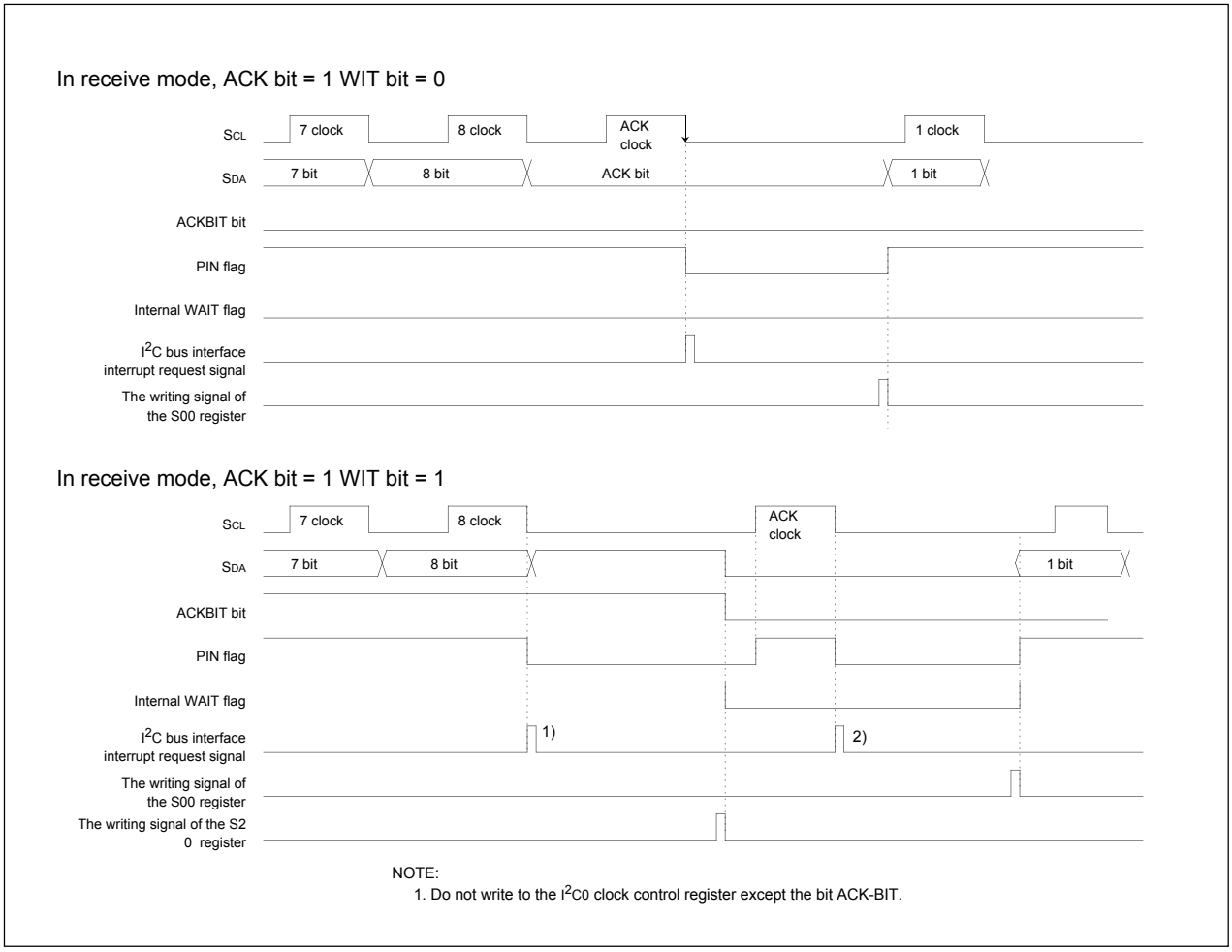


Figure 16.12 The timing of the interrupt generation at the completion of the data receive

16.6.3 Bits 2,3 : Port Function Select Bits PED, PEC

If the ES0 bit in the S1D0 register is set to 1 (I^2C bus interface enabled), the SDAMM functions as an output port. When the PED bit is set to 1 and the SCLMM functions as an output port when the PEC bit is set to 1. Then the setting values of bits P2_0 and P2_1 in the port P2 register are output to the I^2C bus, regardless of he internal SCL/SDA output signals. (SCL/SDA pins are onnected to I^2C bus interface circuit)

The bus data can be read by reading the port pi direction register in input mode, regardless of the setting values of the PED and PEC bits. **Table 16.5** shows the port specification.

Table 16.5 Port specifications

Pin Name	ES9 Bit	PED Bit	P20 Port Direction Register	Function
P20	0	-	0/1	Port I/O function
	1	0	-	SDA I/O function
	1	1	-	SDA input function, port output function
Pin Name	ES0 Bit	PEC Bit	P21 Port Direction Register	Function
P21	0	-	0/1	Port I/O function
	1	0	-	SCL I/O function
	1	1	-	SCL input function, port output funcion

20.7 Software Commands

Read or write 16-bit commands and data from or to even addresses in the user ROM area. When writing a command code, 8 high-order bits (D_{15}–D_8) are ignored.

Table 20.5 Software Commands

Command	First bus cycle			Second bus cycle		
	Mode	Address	Data (D_{15} to D_0)	Mode	Address	Data (D_{15} to D_0)
Read array	Write	X	xxFF16			
Read status register	Write	X	xx7016	Read	X	SRD
Clear status register	Write	X	xx5016			
Program	Write	WA	xx4016	Write	WA	WD
Block erase	Write	X	xx2016	Write	BA	xxD016

SRD: Status register data (D_7 to D_0)
WA : Write address (However,even address)
WD : Write data (16 bits)
BA : Highest-order block address (However,even address)
X : Any even address in the user ROM area
xx : 8 high-order bits of command code (ignored)

20.7.1 Read Array Command (FF16)

The read array command reads the flash memory.

Read array mode is entered by writing command code xxFF16 in the first bus cycle. Content of a specified address can be read in 16-bit unit after the next bus cycle. The MCU remains in read array mode until an another command is written. Therefore, contents of multiple addresses can be read consecutively.

20.7.2 Read Status Register Command (7016)

The read status register command reads the status register.

By writing command code xx7016 in the first bus cycle, the status register can be read in the second bus cycle (Refer to **20.8 Status Register**). Read an even address in the user ROM area. Do not execute this command in EW mode 1.

20.7.3 Clear Status Register Command (5016)

The clear status register command clears the status register to 0.

By writing xx5016 in the first bus cycle, and bits FMR06 to FMR07 in the FMR0 register and bits SR4 to SR5 in the status register are set to 0.

V_{CC} = 5V

Timing Requirements

(V_{CC} = 5V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 21.17 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on both edges)	80		ns

Table 21.18 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 21.19 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 21.20 A /D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ input cycle time (trigger able minimum)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input LOW pulse width	125		ns

Table 21.21 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	100		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	100		ns
$t_{d(C-Q)}$	TxDi output delay time		80	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	70		ns
$t_{h(C-D)}$	RxDi input hold time	90		ns

Table 21.22 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input HIGH pulse width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ input LOW pulse width	250		ns

22.6.1.4 Timer A (Pulse Width Modulation Mode)

1. The timer remains idle after reset. Set the mode, count source, counter value, etc. using bits TA0TGL and TA0TGH in the TAiMR (i = 0 to 4) register, the TAi register, the ONSF register and the TRGSR register before setting the TAiS bit in the TABSR register to 1 (count starts).
   Always make sure bits TA0TGL and TA0TGH in the TAiMR register, the ONSF register and the TRGSR register are modified while the TAiS bit remains 0 (count stops) regardless whether after reset or not.

2. The IR bit is set to 1 when setting a timer operation mode with any of the following procedures:
   • Select the PWM mode after reset.
   • Change an operation mode from timer mode to PWM mode.
   • Change an operation mode from event counter mode to PWM mode.
   To use the timer Ai interrupt (interrupt request bit), set the IR bit to 0 by program after the above listed changes have been made.

3. When setting TAiS register to 0 (count stop) during PWM pulse output, the following action occurs:
   • Stop counting.
   • When TAiOUT pin is output “H”, output level is set to “L” and the IR bit is set to 1.
   • When TAiOUT pin is output “L”, both output level and the IR bit remains unchanged.

4. If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is set to 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), the TA1OUT, TA2OUT and TA4OUT pins go to a high-impedance state.

22.7.2 Rewrite the ICOCiIC Register

When the interrupt request to the ICOCiIC register is generated during the instruction process, the IR bit may not be set to 1 (interrupt requested) and the interrupt request may not be acknowledged. At that time, when the bit in the G1IR register is held to 1 (interrupt requested), the following IC/OC interrupt request will not be generated. When changing the ICOCiIC register settiing, use the following instruction.

Subject instructions: AND, OR, BCLR, BSET

When initializing Timer S, change the ICOCiIC register setting with the request again after setting registers IOCiIC and G1IR to 00_{16}.

22.7.3 Waveform Generating Function

1. If the BTS bit in the G1BCR1 register is set to 0 (base timer is reset) when the waveform is generating and the base timer is stopped counting, the waveform output pin keeps the same output level. The output level will be changed when the base timer and the G1POj register match the setting value next time after the base timer starts counting again.
2. If the G1POCRj register is set when the waveform is generated, the same setting value of the IVL bit is applied to the waveform generating pin. Do not set the G1POCRj register when the waveform is generating.
3. When the RST1 bit in the G1BCR1 register is set to 1 (the base timer is reset by matching the G1PO0 register), the base timer is reset after two clock cycles of f_{BT1} when the base timer value matches the G1PO0 register value. A high-level ("H") signal is applied to the OUTC10 pin between the base timer value match to the base timer reset.

22.7.4 IC/OC Base Timer Interrupt

If the MCU is operated in the combination selected from **Table 22.1** for use when the RST4 bit in the G1BCR0 register is set to 1 (reset the base timer that matches the G1BTRR register) to reset the base timer, an IC/OC base timer interrupt request is generated twice.

Table 22.1 Uses of IT Bit in the G1BCR0 Register and G1BTRR Register

IT Bit in the G1BCR0 Register	G1BTRR Register
0 (bit 15 in the base timer overflows)	$07FFF_{16}$ to $0FFFE_{16}$
1 (bit 14 in the base timer overflows)	$03FFF_{16}$ to $0FFFE_{16}$ or $0BFFF_{16}$ to $0FFFE_{16}$

The second IC/OC base timer interrupt request is generated because the base timer overflow request is generated after one fBT1 clock cycle as soon as the base timer is reset.

One of the following conditions must be met in order not to generate the IC/OC base timer interrupt request twice:

1) When the RST4 bit is set to 1, set the G1BTRR register with a combination other than what is listed in **Table 22.1**.
2) Do not reset the base timer by matching the G1BTRR register. Reset the base timer by matching the G1P00 register. In other words, do not set the RST4 bit to 1 to reset the base timer. Set the RST1 bit in the G1BCR1 register to 1 (reset the base timer that matches the G1P00 register).

Rev.	Date	Description	
		Page	Summary
		360	Table 21.1 is partly revised.
		368	Section “21.4.2 EW1 Mode” is partly revised.
0.80	Sep/03/Y04	2,3	Table 1.2.1 and Table 1.2.2 are partly revised.
		6,7	Table 1.4.1 to Table 1.4.3 are partly revised.
		7	Figure 1.4.1 is partly revised.
		8,9	Figure 1.5.1 and Figure 1.5.2 are partly revised.
		21	Figure 4.7 is partly revised.
		24	Figure 4.10 is partly revised.
		26	Section “5.1.2 Hardware Reset 2” is partly revised.
		29 to 34	Section “5.5 Voltage Detection Circuit” is revised.
		80	Section “10.2 Cold start / Warm start” is added.
		322	Table 20.2 is partly revised.
		323	Table 20.3 is partly revised.
		325	Table 20.6 and Table 20.7 are partly revised.
		327	Table 20.9 is partly revised.
		331	Title of Table 20.23 is partly revised.
		335	Table 20.25 is partly revised.
		339	Title of Table 20.39 is partly revised.
		343	Table 20.41 is partly revised.
		344	Table 20.42 is partly revised.
		346	“Low Voltage Detection Circuit Electrical Characteristics” is deleted.
			Talbe 20.45 is partly revised.
		348	Table 20.47 is partly revised.
		352	Title of Table 20.61 is partly revised.
		356	Talbe 20.63 is partly revised.
		360	Title of Table 20.77 is partly revised.
		398	64P6Q-A package is revised.
1.00	Nov/01/Y04	All pages	Words standardized (on-chip oscillator, A/D)
		2, 3	Table1.2.1 and Table 1.2.2 are partly revised.
		8, 9	Table 1.4.4 to 1.4.6 and figure1.4.2 to 1.4.6 are added.
		28	“5.1.2 Hardware Reset 2” is partly revised.
		29	“5.4 Oscillation Stop Detection Reset” is partly revised.
		38	Table 7.1 is partly revised.
		41	Note 6 in Figure 7.3 is partly revised. b7 to b4 bit in Figure 7.4 is revised.
		42	Figure 7.5 is partly revised.
		43	“PCLKR register” in Figure 7.6 is partly revised.
		50	“7.6.1 Normal Operation Mode” is partly revised.
		51	Note 1 in Table 7.6.1.1 is partly revised.
		57	“7.8 Oscillation Stop and Re-oscillation Detect Function” is partly revised.

Rev.	Date	Description	
		Page	Summary
		9	• **Tables 1.6** to **1.8** Product Codes modified
		19, 20	• **Table 1.14 Pin Description** pin description on I/O ports modified
			Reset
		37	• **Figure 5.2 Reset Sequence** Vcc and ROC timings modified
			Processor Mode
		45	• **Figure 6.2 PM2 Register** Description on notes 5 and 6 modified
			Clock Generation Circuit
		52	• **Figure 7.6 PM2 Register** Description on notes 5 and 6 modified
		64	• **Figure 7.12 State Transition in Normal Mode** note 2 modified
			Protection
		69	• Description on protection modified
			• **Figure 8.1 PRCR Register** note 1 modified
			Interrupts
		88	• **Table 9.6 PC Value Saved in Stack Area When Address Match Interrupt Request I Acknowledged** instruction modified
			Watchdog Timer
		90	• **Figure10.2 WDTS Register** modified
			• **10.1 Count Source Protective Mode** description modified
			Timer
		129	• **Figure 12.28 ICTB2 Register** modified
			Multi-Master I^2C bus Interface
		256	• **Figure 16.1 Block Diagram of Multi-Master I^2C bus Interface** modified
			Flash Memory Version
		335	• **20.3.1 ROM Code Protect Function** register name modified
		340	• **20.5.2 Flash Memory Control Register 1** description on FMR17 bit modified
		341	• **Figure 20.6 FMR1 Register** note 2 modified
		343	• **Figure 20.9 Setting and Resetting of EW Mode 1** modified
			Electrical Characteristics
		369	• **Table 21.5 Flash Memory Version Electrical Characteristics** note 10 modified
		370	• Timing figure for td(P-R) and td(ROC) modified
		372	• **Table 21.9 Electrical Characteristics** parameter and measurement condition modified, note 5 deleted
		380	• **Table 21.25 Electrical Characteristics** measurement condition modified, note 5 deleted
		390	• **Tables 21.43 and 44 Flash Memory Version Electrical Characteristics** note 10 modified
		391	• Timing figure for td(P-R) and td(ROC) modified
		393	• **Table 21.47 Electrical Characteristics** parameter and condition modified, note