Renesas Electronics America Inc - M30291FATHP#U3AAJ7 Datasheet

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7.2 Sub Clock

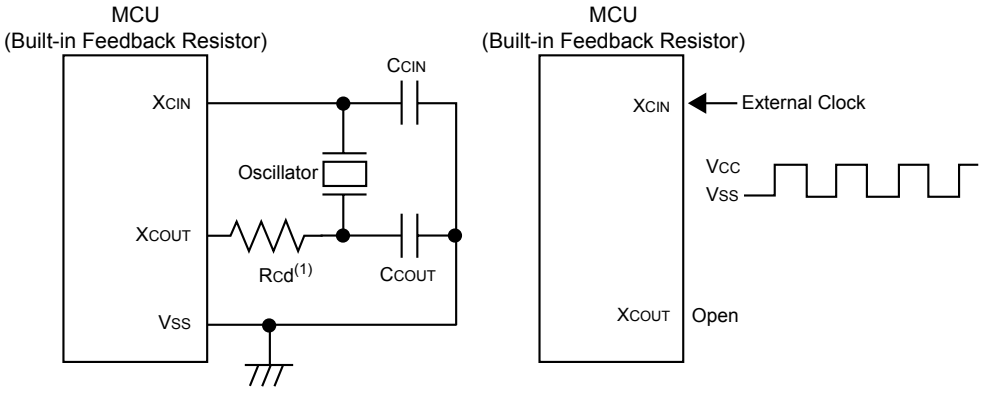
The sub clock is generated by the sub clock oscillation circuit. This clock is used as the clock source for the CPU clock, as well as the timer A and timer B count sources.

The sub clock oscillator circuit is configured by connecting a crystal resonator between the XCIN and XCOUT pins. The sub clock oscillator circuit contains a feedback resistor, which is disconnected from the oscillator circuit during stop mode in order to reduce the amount of power consumed in the chip. The sub clock oscillator circuit may also be configured by feeding an externally generated clock to the XCIN pin. **Figure 7.9** shows the examples of sub clock connection circuit.

After reset, the sub clock is turned off. At this time, the feedback resistor is disconnected from the oscillator circuit.

To use the sub clock for the CPU clock, set the CM07 bit in the CM0 register to 1 (sub clock) after the sub clock becomes oscillating stably.

During stop mode, all clocks including the sub clock are turned off. Refer to “power control”.



NOTE:
1. Place a damping resistor if required. Resistance values vary depending on the oscillator setting. Use values recommended by each oscillator manufacturer. Place a feedback resistor between XCIN and XCOUT if the oscillator manufacturer recommends placing the resistor externally.

Figure 7.9 Examples of Sub Clock Connection Circuit

9.3.1 I Flag

The I flag enables or disables the maskable interrupt. Setting the I flag to 1 (= enabled) enables the maskable interrupt. Setting the I flag to 0 (= disabled) disables all maskable interrupts.

9.3.2 IR Bit

The IR bit is set to 1 (= interrupt requested) when an interrupt request is generated. Then, when the interrupt request is accepted and the CPU branches to the corresponding interrupt vector, the IR bit is cleared to 0 (= interrupt not requested).
The IR bit can be cleared to 0 in a program. Note that do not write 1 to this bit.

9.3.3 ILVL2 to ILVL0 Bits and IPL

Interrupt priority levels can be set using bits ILVL2 to ILVL0.
Table 9.3 shows the settings of interrupt priority levels and **Table 9.4** shows the interrupt priority levels enabled by the IPL.

The following are conditions under which an interrupt is accepted:
· I flag = 1
· IR bit = 1
· interrupt priority level > IPL

The I flag, IR bit, bits ILVL2 to ILVL0, and IPL are independent of each other. In no case do they affect one another.

Table 9.3 Settings of Interrupt Priority Levels

ILVL2 to ILVL0 bits	Interrupt priority level	Priority order
000_2	Level 0 (interrupt disabled)	———
001_2	Level 1	Low ↓
010_2	Level 2	
011_2	Level 3	
100_2	Level 4	
101_2	Level 5	
110_2	Level 6	
111_2	Level 7	High

Table 9.4 Interrupt Priority Levels Enabled by IPL

IPL	Enabled interrupt priority levels
000_2	Interrupt levels 1 and above are enabled
001_2	Interrupt levels 2 and above are enabled
010_2	Interrupt levels 3 and above are enabled
011_2	Interrupt levels 4 and above are enabled
100_2	Interrupt levels 5 and above are enabled
101_2	Interrupt levels 6 and above are enabled
110_2	Interrupt levels 7 and above are enabled
111_2	All maskable interrupts are disabled

Timer Ai Mode Register (i=2 to 4)
(When using two-phase pulse signal processing)

b6	b5	b4	b3	b2	b1	b0
		0	1	0	0	0	1

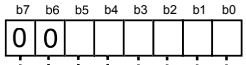
Symbol	Address	After Reset
TA2MR to TA4MR	0398_{16} to $039A_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	$^{b1\ b0}$ 0 1: Event counter mode	RW
TMOD1			RW
MR0	To use two-phase pulse signal processing, set this bit to 0		RW
MR1	To use two-phase pulse signal processing, set this bit to 0		RW
MR2	To use two-phase pulse signal processing, set this bit to 1		RW
MR3	To use two-phase pulse signal processing, set this bit to 0		RW
TCK0	Count operation type select bit	0: Reload type 1: Free-run type	RW
TCK1	Two-phase pulse signal processing operation select bit (1)(2)	0: Normal processing operation 1: Multiply-by-4 processing operation	RW

NOTES:
1. The TCK1 bit is valid for timer A3 mode register. No matter how this bit is set, timers A2 and A4 always operate in normal processing mode and x4 processing mode, respectively.
2. If two-phase pulse signal processing is desired, following register settings are required:
   - Set the TAiP bit in the UDF register to 1 (two-phase pulse signal processing function enabled).
   - Set bits TAiTGH and TAiTGL in the TRGSR register to 00_2 (TAiIN pin input).
   - Set the port direction bits for TAiIN and TAiOUT to 0 (input mode).

Figure 12.9 TA2MR to TA4MR Registers in Event Counter Mode (when using two-phase pulse signal processing with timer A2, A3 or A4)

Three-phase Output Buffer Register(i=0,1) (1)

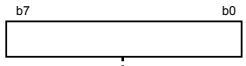


Symbol	Address	After Reset
IDB0	$034A_{16}$	00111111_2
IDB1	$034B_{16}$	00111111_2

Bit Symbol	Bit Name	Function	RW
DUi	U phase output buffer i	Write the output level 0: Active level 1: Inactive level When read, these bits show the three-phase output shift register value.	RW
DUBi	$\overline{U}$ phase output buffer i		RW
DVi	V phase output buffer i		RW
DVBi	$\overline{V}$ phase output buffer i		RW
DWi	W phase output buffer i		RW
DWBi	$\overline{W}$ phase output buffer i		RW
$\overline{(b7\text{-}b6)}$	Nothing is assigned. If necessary, set to 0. When read, these contents are 0		RO

NOTE:
1. Registers IDB0 and IDB1 values are transferred to the three-phase shift register by a transfer trigger. The value written to the IDB0 register aftera transfer trigger represents the output signal of each phase, and the next value written to the IDB1 register at the falling edge of the timer A1, A2, or A4 one-shot pulse represents the output signal of each phase.

Dead Time Timer (1, 2)

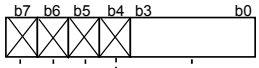


Symbol	Address	After Reset
DTT	$034C_{16}$	Undefined

Function	Setting Range	RW
Assuming the set value = n, upon a start trigger the timer starts counting the count souce selected by the INV12 bit and stops after counting it n times. The positive or negative phase whichever is going from an inactive to an active level changes at the same time the dead time timer stops.	1 to 255	WO

NOTES:
1. Use MOV instruction to write to this register.
2. Effective when the INV15 bit is set to 0 (dead time timer enable). If the INV15 bit is set to 1, the dead time timer is disabled and has no effect.

Timer B2 Interrupt Occurrences Frequency Set Counter



Symbol	Address	After Reset
ICTB2	$034D_{16}$	Undefined

Function	Setting Range	RW
If the INV01 bit is 0 (ICTB2 counter counted every time timer B2 underflows), assuming the set value = n, a timer B2 interrupt is generated at every *n*th occurrence of a timer B2 underflow. If the INV01 bit is 1 (ICTB2 counter count timing selected by the INV00 bit), assuming the set value = n, a timer B2 interrupt is generated at every *n*th occurrence of a timer B2 underflow that meets the condition selected by the INV00 bit. (1)	1 to 15	WO
Nothing is assigned. When write, set to "0". When read, the content is undefined.		—

NOTE:
1. Use MOV instruction to write to this register.
If the INV01 bit is set to 1, make sure the TB2S bit also is set to 0 (timer B2 count stopped) when writing to this register. If the INV01 bit is set to 0, although this register can be written even when the TB2S bit is set to 1 (timer B2 count start), do not write synchronously with a timer B2 underflow.

Figure 12.28 IDB0 Register, IDB1Register, DTT Register, and ICTB2 Register

13.5.1 Single-Phase Waveform Output Mode

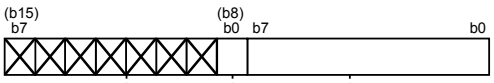
Output signal level of the OUTC1j pin becomes high ("H") when the INV bit in the G1POCRj (j=0 to 7) register is set to 0(output is not reversed) and the base timer value matches the G1POj (j=0 to 7) register value. The "H" signal switches to a low-level ("L") signal when the base timer reaches 0000_{16}. **Table 13.8** lists specifications of single-phase waveform mode. **Figure 13.22** lists an example of single-phase waveform mode operation.

Table 13.8 Single-phase Waveform Output Mode Specifications

Item	Specification
Output waveform	• Free-running operation (bits RST1, RST2, and RST4 of registers G1BCR1 and G1BCR0 are set to 0 (no reset)) Cycle : $\frac{65536}{f_{BT1}}$ Default output level width : $\frac{m}{f_{BT1}}$ Inverse level width : $\frac{65536-m}{f_{BT1}}$ • The base timer is cleared to 0000_{16} by matching the base timer with either following register (a) G1PO0 register (enabled by setting RST1 bit to 1, and RST4 and RST2 bits to 0), or (b) G1BTRR register (enabled by setting RST4 bit to 1, and RST2 and RST1 bits to 0) Cycle : $\frac{n+2}{f_{BT1}}$ Default output level width : $\frac{m}{f_{BT1}}$ Inverse level width $\frac{n+2-m}{f_{BT1}}$ m : setting value of the G1POj register (j=0 to 7), 0001_{16} to $FFFD_{16}$ n : setting value of the G1PO0 register or the G1BTRR register, 0001_{16} to $FFFD_{16}$
Waveform output start condition	The IFEj bit in the G1FE register is set to 1 (channel j function enabled)
Waveform output stop condition	The IFEj bit is set to 0 (channel j function disabled)
Interrupt request	The G1IRj bit in the G1IR register is set to 1 when the base timer value matches the G1POj register value (See **Figure 13.22**)
OUTC1j pin (1)	Pulse signal output pin
Selectable function	• Default value set function: Set starting waveform output level • Inverse output function: Waveform output signal is inversed and provided from the OUTC1j pin

NOTE:
1. Pins $OUTC1_0$ to $OUTC1_7$.

UARTi Transmit Buffer Register (i=0 to 2)(1)

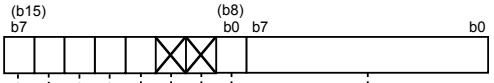


Symbol	Address	After Reset
U0TB	03A3$_{16}$-03A2$_{16}$	Undefined
U1TB	03AB$_{16}$-03AA$_{16}$	Undefined
U2TB	037B$_{16}$-037A$_{16}$	Undefined

Function	RW
Transmit data	WO
Nothing is assigned. If necessary, set to 0. When read, their contents are undefined	—

NOTES:
1. Use MOV instruction to write to this register.

UARTi Receive Buffer Register (i=0 to 2)

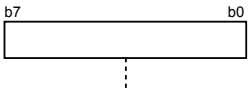


Symbol	Address	After Reset
U0RB	03A7$_{16}$-03A6$_{16}$	undefined
U1RB	03AF$_{16}$-03AE$_{16}$	undefined
U2RB	037F$_{16}$-037E$_{16}$	undefined

Bit Symbol	Bit Name	Function	RW
(b7-b0)	———	Receive data (D$_7$ to D$_0$)	RO
(b8)	———	Receive data (D$_8$)	RO
(b10-b9)	Nothing is assigned. If necessary, set to 0. When read, their contents are undefined		—
ABT	Arbitration lost detecting flag (2)	0 : Not detected 1 : Detected	RW
OER	Overrun error flag(1)	0 : No overrun error 1 : Overrun error found	RO
FER	Framing error flag(1)	0 : No framing error 1 : Framing error found	RO
PER	Parity error flag(1)	0 : No parity error 1 : Parity error found	RO
SUM	Error sum flag (1)	0 : No error 1 : Error found	RO

NOTES:
1. When the SMD2 to SMD0 bits in the UiMR register are set to 000$_2$ (serial I/O disabled) or the RE bit in the UiC1 register is set to 0 (reception disabled), all bits SUM, PER, FER and OER are set to 0 (no error). The SUM bit is set to 0 (no error) when all of the PER, FER and OER bits are set to 0 (no error). Also, bits PER and FER are set to 0 by reading the lower byte of the UiRB register.
2. The ABT bit is set to 0 by setting to 0 by program. (Writing 1 has no effect.) Nothing is assigned at the bit 11 in the U0RB and U1RB registers. If necessary, set to 0. When read, its content is 0.

UARTi Baud Rate Generation Register (i=0 to 2)(1, 2, 3)



Symbol	Address	After Reset
U0BRG	03A1$_{16}$	Undefined
U1BRG	03A9$_{16}$	Undefined
U2BRG	0379$_{16}$	Undefined

Function	Setting Range	RW
Assuming that set value = n, UiBRG divides the count source by n + 1	00$_{16}$ to FF$_{16}$	WO

NOTES:
1. Write to this register while serial I/O is neither transmitting nor receiving.
2. Use MOV instruction to write to this register.
   The transfer clock is shown below when the setting value in the UiBRG register is set as n.
   (1) When the CKDIR bit in the UiMR register to 0 (internal clock)
   • Clock synchronous serial I/O mode : fj/(2(n+1))
   • Clock asynchronous serial I/O (UART) mode : fj/(16(n+1))
   (2) When the CKDIR bit in the UiMR register to 1 (external clock)
   • Clock synchronous serial I/O mode : f_{EXT}
   • Clock asynchronous serial I/O (UART) mode : f_{EXT}/(16(n+1))
   fj : f1SIO, f2SIO, f8SIO, f32SIO
   f_{EXT} : Input from CLKi pin
3. Set the UiBRG register after setting bits CLK1 and CLK0 in the registers UiC0.

Figure 14.4 U0TB to U2TB, U0RB to U2RB, U0BRG to U2BRG Registers

Table 14.3 lists pin functions for the case where the multiple transfer clock output pin select function is deselected. **Table 14.4** lists the P6$_4$ pin functions during clock synchronous serial I/O mode.
Note that for a period from when the UARTi operation mode is selected to when transfer starts, the TxDi pin outputs an “H”. (If the N-channel open-drain output is selected, this pin is in a high-impedance state.)

Table 14.3 Pin Functions (When Not Select Multiple Transfer Clock Output Pin Function)(1)

Pin Name	Function	Method of Selection
TxDi (i = 0 to 2) (P6$_3$, P6$_7$, P7$_0$)	Serial data output	(Outputs dummy data when performing reception only)
RxDi (P6$_2$, P6$_6$, P7$_1$)	Serial data input	Set the PD6_2 bit and PD6_6 bit in the PD6 register, and PD7_1 bit in the PD7 register to 0 (Can be used as an input port when performing transmission only)
CLKi (P6$_1$, P6$_5$, P7$_2$)	Transfer clock output	Set the CKDIR bit in the UiMR register to 0
	Transfer clock input	Set the CKDIR bit in the UiMR register to 1 Set the PD6_1 bit and PD6_5 bit in the PD6 register, and the PD7_2 bit in the PD7 register to 0
$\overline{\text{CTS}}$i/$\overline{\text{RTS}}$i (P6$_0$, P6$_4$, P7$_3$)	$\overline{\text{CTS}}$ input	Set the CRD bit in the UiC0 register to 0 Set the CRS bit in the UiC0 register to 0 Set the PD6_0 bit and PD6_4 bit in the PD6 register is set to 0, the PD7_3 bit in the PD7 register to 0
	$\overline{\text{RTS}}$ output	Set the CRD bit in the UiC0 register to 0 Set the CRS bit in the UiC0 register to 1
	I/O port	Set the CRD bit in the UiC0 register to 1

NOTE:
1: When the U1MAP bit in PACR register is 1 (P7$_3$ to P7$_0$), UART1 pin is assgined to P7$_3$ to P7$_0$.

Table 14.4 P6$_4$ Pin Functions(1)

Pin Function	Bit Set Value					
	U1C0 register		UCON register			PD6 register
	CRD	CRS	RCSP	CLKMD1	CLKMD0	PD6_4
P6$_4$	1	—	0	0	—	Input: 0, Output: 1
$\overline{\text{CTS}}_1$	0	0	0	0	—	0
$\overline{\text{RTS}}_1$	0	1	0	0	—	—
$\overline{\text{CTS}}_0$(2)	0	0	1	0	—	0
CLKS$_1$	—	—	—	1(3)	1	—

NOTES:
1. When the U1MAP bit in PACR register is 1 (P7$_3$ to P7$_0$), this table lists the P7$_0$ functions.
2. In addition to this, set the CRD bit in the U0C0 register to 0 ($\overline{\text{CT0}}_0$/$\overline{\text{RT0}}_0$ enabled) and the CRS bit in the U0C0 register to 1 ($\overline{\text{RTS}}_0$ selected).
3. When the CLKMD1 bit is set to 1 and the CLKMD0 bit is set to 0, the following logic levels are output:
   • High if the CLKPOL bit in the U1C0 register is set to 0
   • Low if the CLKPOL bit in the U1C0 register is set to 1

14.1.2.2 Counter Measure for Communication Error

If a communication error occurs while transmitting or receiving in UART mode, follow the procedure below.

• Resetting the UiRB register (i=0 to 2)

(1) Set the RE bit in the UiC1 register to 0 (reception disabled)

(2) Set the RE bit in the UiC1 register to 1 (reception enabled)

• Resetting the UiTB register (i=0 to 2)

(1) Set bits SMD2 to SMD0 in UiMR register 000_2 (Serial I/O disabled)

(2) Set bits SMD2 to SMD0 in UiMR register 001_2, 101_2, 110_2

(3) 1 is written to TE bit in the UiC1 register (reception enabled), regardless of the TE bit

14.1.2.3 LSB First/MSB First Select Function

As shown in **Figure 14.18**, use the UFORM bit in the UiC0 register to select the transfer format. This function is valid when transfer data is 8 bits long.

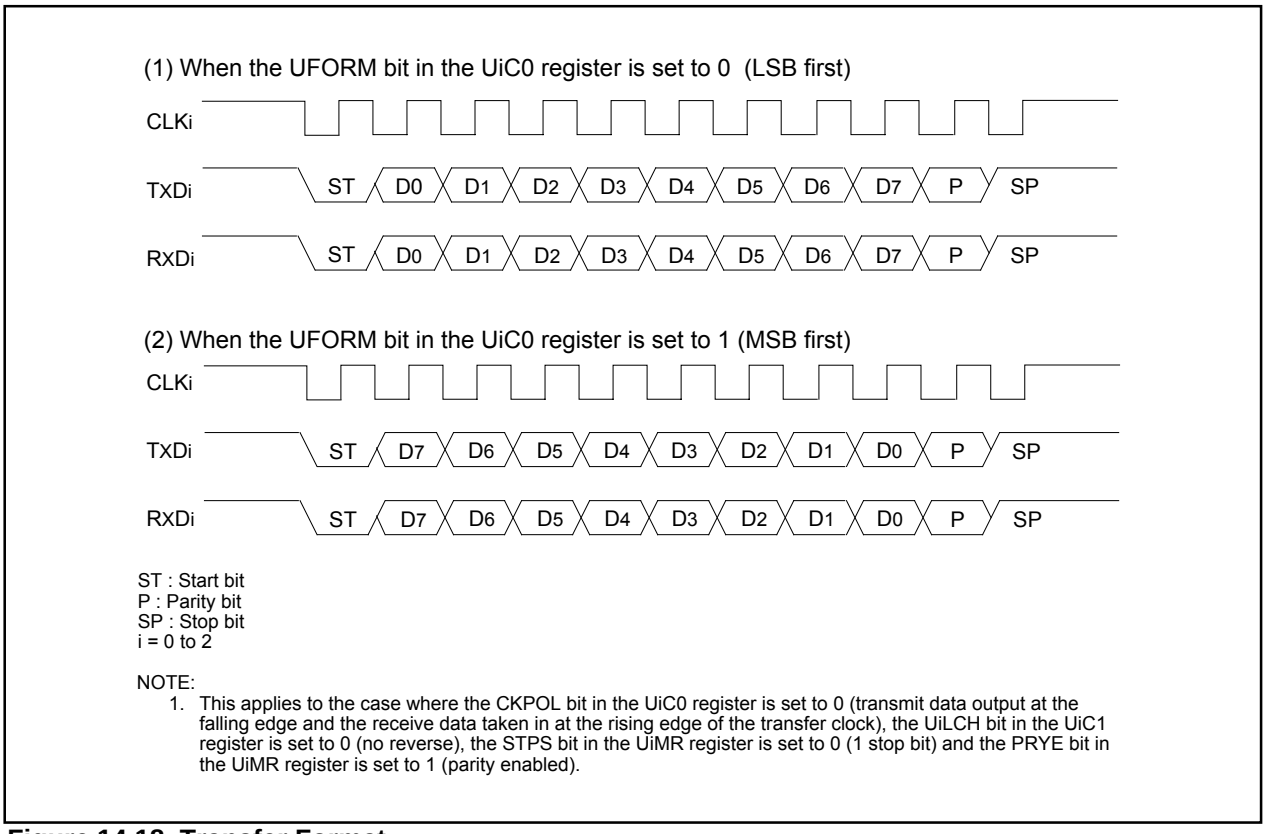


Figure 14.18 Transfer Format

14.2 SI/O3 and SI/O4

Note

The SI/O4 interrupt of peripheral function interrupt is not available in the 64-pin package.

SI/O3 and SI/O4 are exclusive clock-synchronous serial I/Os.

Figure 14.35 shows the block diagram of SI/O3 and SI/O4, and **Figure 14.36** shows the SI/O3 and SI/O4-related registers.

Table 14.20 shows the specifications of SI/O3 and SI/O4.

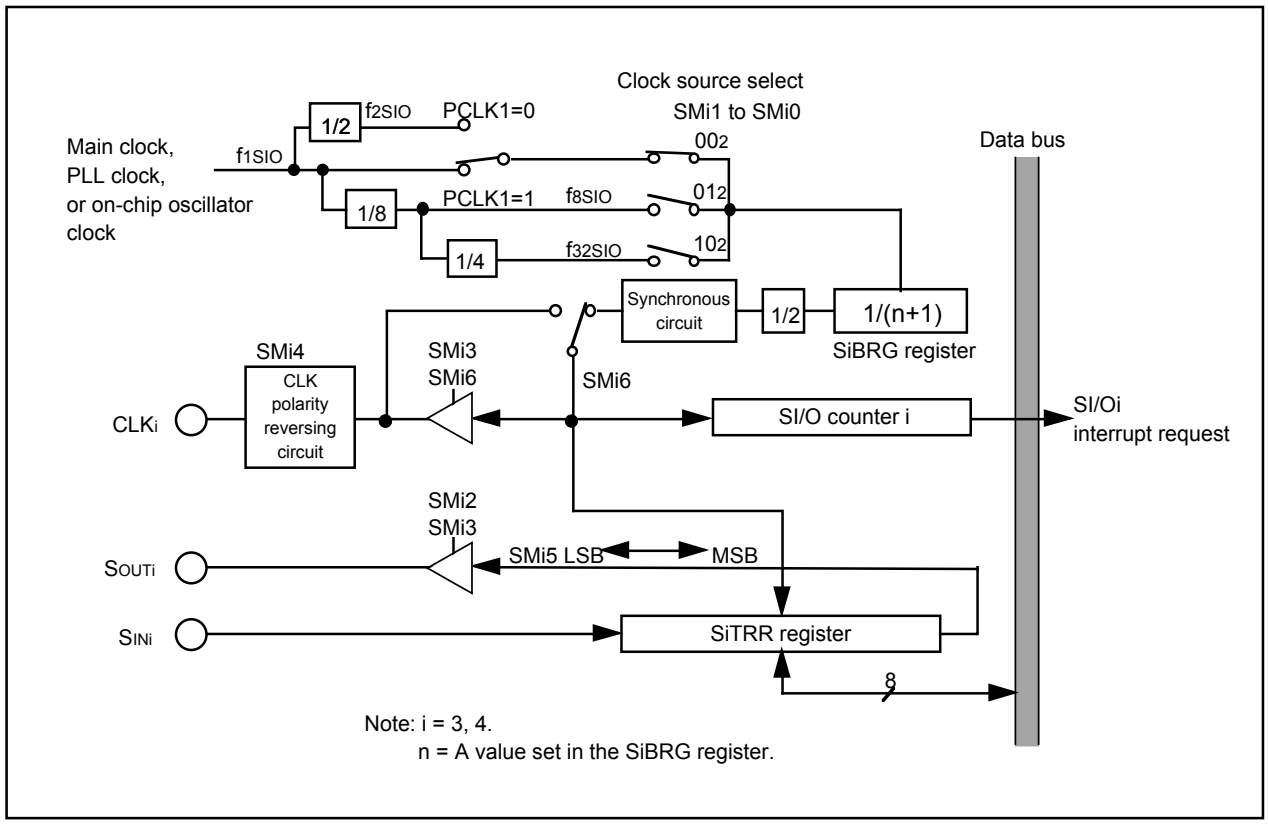


Figure 14.35 SI/O3 and SI/O4 Block Diagram

17.1 CAN Module-Related Registers

The CAN0 module has the following registers.

(1) CAN Message Box

A CAN module is equipped with 16 slots (16 bytes or 8 words each). Slots 14 and 15 can be used as Basic CAN.

- Priority of the slots: The smaller the number of the slot, the higher the priority, in both transmission and reception.
- A program can define whether a slot is defined as transmitter or receiver.

(2) Acceptance Mask Registers

A CAN module is equipped with 3 masks for the acceptance filter.

- CAN0 global mask register (C0GMR register: 6 bytes)
  Configuration of the masking condition for acceptance filtering processing to slots 0 to 13
- CAN0 local mask A register (C0LMAR register: 6 bytes)
  Configuration of the masking condition for acceptance filtering processing to slot 14
- CAN0 local mask B register (C0LMBR register: 6 bytes)
  Configuration of the masking condition for acceptance filtering processing to slot 15

(3) CAN SFR Registers

- CAN0 message control register j (C0MCTLj register: 8 bits × 16) (j = 0 to 15)
  Control of transmission and reception of a corresponding slot
- CANi control register (CiCTLR register: 16 bits) (i = 0, 1)
  Control of the CAN protocol
- CAN0 status register (C0STR register: 16 bits)
  Indication of the protocol status
- CAN0 slot status register (C0SSTR register: 16 bits)
  Indication of the status of contents of each slot
- CAN0 interrupt control register (C0ICR register: 16 bits)
  Selection of “interrupt enabled or disabled” for each slot
- CAN0 extended ID register (C0IDR register: 16 bits)
  Selection of ID format (standard or extended) for each slot
- CAN0 configuration register (C0CONR register: 16 bits)
  Configuration of the bus timing
- CAN0 receive error count register (C0RECR register: 8 bits)
  Indication of the error status of the CAN module in reception: the counter value is incremented or decremented according to the error occurrence.
- CAN0 transmit error count register (C0TECR register: 8 bits)
  Indication of the error status of the CAN module in transmission: the counter value is incremented or decremented according to the error occurrence.
- CAN0 time stamp register (C0TSR register: 16 bits)
  Indication of the value of the time stamp counter
- CAN0 acceptance filter support register (C0AFS register: 16 bits)
  Decoding the received ID for use by the acceptance filter support unit

Explanation of each register is given as follows.

17.1.3.2 C0CTLR Register

Figure 17.7 shows the C0CTLR register.

CAN0 Control Register

b7	b6	b5	b4	b3	b2	b1	b0
X							

Symbol	Address	After reset
C0CTLR	0210_{16}	$X0000001_2$

Bit Symbol	Bit Name	Function	RW
Reset	CAN module reset bit (Note 1)	0: Operation mode 1: Reset/initialization mode	RW
LoopBack	Loop back mode select bit (2)	0: Loop back mode disabled 1: Loop back mode enabled	RW
MsgOrder	Message order select bit (2)	0: Word access 1: Byte access	RW
BasicCAN	Basic CAN mode select bit (2)	0: Basic CAN mode disabled 1: Basic CAN mode enabled	RW
BusErrEn	Bus error interrupt enable bit (2)	0: Bus error interrupt disabled 1: Bus error interrupt enabled	RW
Sleep	Sleep mode select bit (2, 3)	0: Sleep mode disabled 1: Sleep mode enabled; clock supply stopped	RW
PortEn	CAN port enable bit (2, 3)	0: I/O port function 1: CTx/CRx function(4)	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined		—

NOTES:
1. When the Reset bit is set to 1 (CAN reset/initialization mode), check that the State_Reset bit in the C0STR register is set to 1 (Reset mode).
2. Change this bit only in the CAN reset/initialization mode.
3. When using CAN0 wake-up interrupt, set these bits to 1.
4. When the PortEn bit is set to 1, set the PD9_2 bit in the PD9 register to 0.

(b15) b7	b6	b5	b4	b3	b2	b1	(b8) b0
X	X		X				

Symbol	Address	After reset
C0CTLR	0211_{16}	$XX0X0000_2$

Bit Symbol	Bit Name	Function	RW
TSPreScale Bit1, Bit0	Time stamp prescaler(3)	b1 b0 0 0: Period of 1 bit time 0 1: Period of 1/2 bit time 1 0: Period of 1/4 bit time 1 1: Period of 1/8 bit time	RW
TSReset	Time stamp counter reset bit(1)	0: In an idle state 1: Force reset of the time stamp counter	RW
RetBusOff	Return from bus off command bit(2)	0: In an idle state 1: Force return from bus off	RW
— (b4)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined		—
RXOnly	Listen-only mode select bit (3)	0: Listen-only mode disabled 1: Listen-only mode enabled (4)	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined		—

NOTES:
1. When the TSReset bit is set to 1, the C0TSR register is set to 0000_{16}. After this, the bit is automatically set to 0.
2. When the RetBusOff bit is set to 1, registers C0RECR and C0TECR are set to 00_{16}. After this, the bit is automatically set to 0.
3. Change this bit only in the CAN reset/initialization mode.
4. When the listen-only mode is selected, do not request the transmission.

Figure 17.7 C0CTLR Register

17.2.2 CAN Operating Mode

The CAN operating mode is activated by setting the Reset bit in the C0CTLR register to 0. If the Reset bit is set to 0, check that the State_Reset bit in the C0STR register is set to 0.

If 11 consecutive recessive bits are detected after entering the CAN operating mode, the module initiates the following functions:

- The module's communication functions are released and it becomes an active node on the network and may transmit and receive CAN messages.
- Release the internal fault confinement logic including receive and transmit error counters. The module may leave the CAN operating mode depending on the error counts.

Within the CAN operating mode, the module may be in three different sub modes, depending on which type of communication functions are performed:

- Module idle : The modules receive and transmit sections are inactive.
- Module receives : The module receives a CAN message sent by another node.
- Module transmits : The module transmits a CAN message. The module may receive its own message simultaneously when the LoopBack bit in the C0CTLR register = 1 (Loop back mode enabled).

Figure 17.18 shows sub modes of the CAN operating mode.

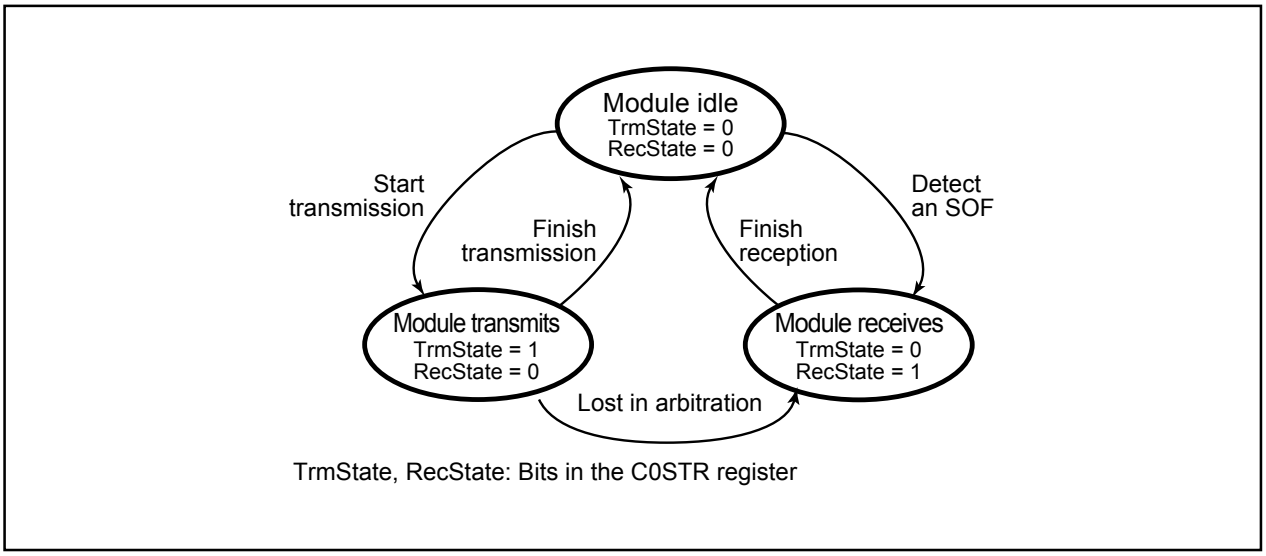


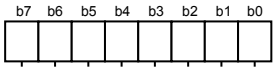
Figure 17.18 Sub Modes of CAN Operating Mode

17.2.3 CAN Sleep Mode

The CAN sleep mode is activated by setting the Sleep bit in the C0CTLR register to 1. It should never be activated from the CAN operating mode but only via the CAN reset/initialization mode.

Entering the CAN sleep mode instantly stops the clock supply to the module and thereby reduces power dissipation.

Pull-up Control Register 0 (1)

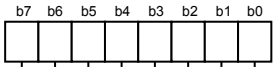


Symbol	Address	After Reset
PUR0	03FC16	0016

Bit Symbol	Bit Name	Function	RW
PU00	P00 to P03 pull-up	0: Not pulled up 1: Pulled up (1)	RW
PU01	P04 to P07 pull-up		RW
PU02	P10 to P13 pull-up		RW
PU03	P14 to P17 pull-up		RW
PU04	P20 to P23 pull-up		RW
PU05	P24 to P27 pull-up		RW
PU06	P30 to P33 pull-up		RW
PU07	P34 to P37 pull-up		RW

NOTE:
1. The pin for which this bit is 1 (pulled up) and the direction bit is 0 (input mode) is pulled up.

Pull-up Control Register 1

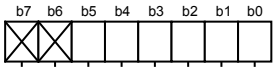


Symbol	Address	After Reset
PUR1	03FD16	0016

Bit Symbol	Bit Name	Function	RW
—— (b3-b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—
PU14	P60 to P63 pull-up	0: Not pulled high 1: Pulled high (1)	RW
PU15	P64 to P67 pull-up		RW
PU16	P70 to P73 pull-up		RW
PU17	P74 to P77 pull-up		RW

NOTE:
1. The pin for which this bit is 1 (pulled up) and the direction bit is 0 (input mode) is pulled up.

Pull-up Control Register 2



Symbol	Address	After Reset
PUR2	03FE16	0016

Bit Symbol	Bit Name	Function	RW
PU20	P80 to P83 pull-up	0: Not pulled up 1: Pulled up (1)	RW
PU21	P84 to P87 pull-up		RW
PU22	P90 to P93 pull-up		RW
PU23	P95 to P97 pull-up		RW
PU24	P100 to P103 pull-up		RW
PU25	P104 to P107 pull-up		RW
—— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—

NOTE:
1. The pin for which this bit is 1 (pulled up) and the direction bit is 0 (input mode) is pulled up.

Figure 19.8 PUR0 to PUR2 Registers

Table 21.4 Flash Memory Version Electrical Characteristics (1) for 100/1000 E/W cycle products

[Program Space and Data Space in U3 and U5: Program Space in U7 and U9]

Symbol	Parameter		Standard			Unit
			Min.	Typ.(2)	Max.	
-	Program and Erase Endurance(3)		100/1000(4, 11)			cycles
-	Word Program Time (Vcc=5.0V, Topr=25° C)			75	600	µs
-	Block Erase Time (Vcc=5.0V, Topr=25° C)	2-Kbyte Block		0.2	9	s
		8-Kbyte Block		0.4	9	s
		16-Kbyte Block		0.7	9	s
		32-Kbyte Block		1.2	9	s
td(SR-ES)	Duration between Suspend Request and Erase Suspend				8	ms
tPS	Wait Time to Stabilize Flash Memory Circuit				15	µs
-	Data Hold Time (5)		20			years

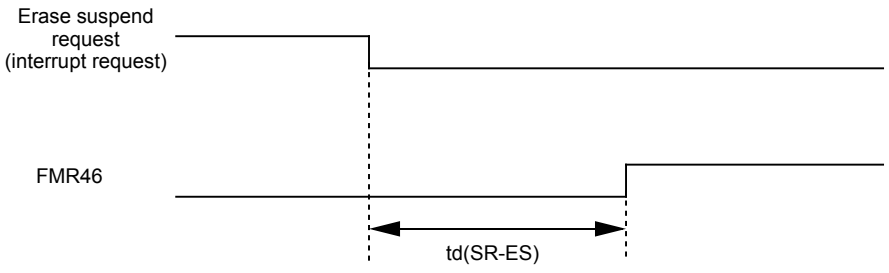
Table 21.5 Flash Memory Version Electrical Characteristics (6) 10000 E/W cycle products (Option)

[Data Space in U7 and U9(7)]

Symbol	Parameter	Standard			Unit
		Min.	Typ.(2)	Max.	
-	Program and Erase Endurance(3, 8, 9)	10000(4, 10)			cycles
-	Word Program Time (Vcc= 5.0 V, Topr = 25° C)		100		µs
-	Block Erase Time (Vcc= 5.0 V, Topr = 25° C) (2-Kbyte block)		0.3		s
td(SR-ES)	Duration between Suspend Request and Erase Suspend			8	ms
tPS	Wait Time to Stabilize Flash Memory Circuit			15	µs
-	Data Hold Time (5)	20			years

NOTES:

1. Referenced to Vcc= 2.7 to 5.5 V at Topr = 0 to 60° C (program space), unless otherwise specified.
2. Vcc= 5.0 V; Topr= 25° C
3. Program and erase endurance is defined as number of program-erase cycles per block.
   If program and erase endurance is *n* cycle (*n* = 100, 1000, 10000), each block can be erased and programmed *n* cycles.
   For example, if a 2-Kbyte block A is erased after programming one-word data to each address 1,024 times, this counts as one program and erase endurance. Data cannot be programmed to the same address more than once without erasing the block. (rewrite prohibited).
4. Number of E/W cycles for which operation is guranteed (1 to minimum value are guaranteed).
5. Topr= 55° C
6. Referenced to Vcc= 2.7 to 5.5 V at Topr= -40 to 85° C(U7) / -20 to 85° C (U9) unless otherwise specifie.
7. **Table 21.5** applies for data space in U7 and U9 when program and erase endurance is more than 1,000 cycles. Otherwise, use **Table 21.4**.
8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 128 times maximum before erase becomes necessary. Maintaining an equal number of times erasure between block A and block B will also improve efficiency. It is recommended to track the total number of erasure performed per block and to limit the number of erasure.
9. If an erase error is generated during block erase, execute the clear status register command and block erase command at least 3 times until an erase error is not generated.
10. When executing more than 100 times rewrites, set one wait state per block access by setting the FMR17 bit in the FMR1 register 1 to 1 (wait state). When accessing to all other blocks and internal RAM, wait state can be set by the PM17 bit, regardless of the FMR17 bit setting value.
11. The program and erase endurance is 100 cycles for program space and data space in U3 and U5; 1,000 cycles for program space in U7 and U9.
12. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for further details on the E/W failure rate.



V_{CC} = 5V

Table 21.8 Electrical Characteristics (Note 1)

Symbol	Parameter				Condition	Standard			Unit
						Min.	Typ.	Max.	
V_{OH}	Output High ("H") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$			I_{OH}=-5mA	V_{CC}-2.0		V_{CC}	V
V_{OH}	Output High ("H") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$			I_{OH}=-200µA	V_{CC}-0.3		V_{CC}	V
V_{OH}	Output High ("H") Voltage		X_{OUT}	High Power	I_{OH}=-1mA	V_{CC}-2.0		V_{CC}	V
				Low Power	I_{OH}=-0.5mA	V_{CC}-2.0		V_{CC}	
	Output High ("H") Voltage		X_{COUT}	High Power	No load applied		2.5		V
				Low Power	No load applied		1.6		
V_{OL}	Output Low ("L") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$			I_{OL}=5mA			2.0	V
V_{OL}	Output Low ("L") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$			I_{OL}=200µA			0.45	V
V_{OL}	Output Low ("L") Voltage		X_{OUT}	High Power	I_{OL}=1mA			2.0	V
				Low Power	I_{OL}=0.5mA			2.0	
	Output Low ("L") Voltage		X_{COUT}	High Power	No load applied		0		V
				Low Power	No load applied		0		
V_{T+}-V_{T-}	Hysteresis	$TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB2_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS2}$, SCL, SDA, $CLK0$-$CLK2$, $TA2_{OUT}$-$TA4_{OUT}$, $\overline{KI0}$-$\overline{KI3}$, $RXD0$-$RXD2$, $SIN3$, $SIN4$				0.2		1.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$				0.2		2.5	V
V_{T+}-V_{T-}	Hysteresis	X_{IN}				0.2		0.8	V
I_{IH}	Input High ("H") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}			V_I=5V			5.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}			V_I=0V			-5.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$			V_I=0V	30	50	170	kΩ
Rf_{XIN}	Feedback Resistance		X_{IN}				1.5		MΩ
Rf_{XCIN}	Feedback Resistance		X_{CIN}				15		MΩ
V_{RAM}	RAM Standby Voltage				In stop mode	2.0			V

NOTES:

1. Referenced to V_{CC}=4.2 to 5.5V, V_{SS}=0V at Topr=-20 to 85 ° C / -40 to 85 ° C, f(BCLK)=20MHz unless otherwise specified.

21.3 V Version

Table 21.78 Absolute Maximum Ratings

Symbol	Parameter			Condition	Value	Unit
V_{CC}	Supply Voltage			V_{CC}=AV$_{CC}$	-0.3 to 6.5	V
AV$_{CC}$	Analog Supply Voltage			V_{CC}=AV$_{CC}$	-0.3 to 6.5	V
V_I	Input Voltage	P0$_0$ to P0$_7$, P1$_0$ to P1$_7$, P2$_0$ to P2$_7$, P3$_0$ to P3$_7$, P6$_0$ to P6$_7$, P7$_0$ to P7$_7$, P8$_0$ to P8$_7$, P9$_0$ to P9$_3$, P9$_5$ to P9$_7$, P10$_0$ to P10$_7$, X_{IN}, V_{REF}, $\overline{\text{RESET}}$, CNV_{SS}			-0.3 to V_{CC}+0.3	V
V_O	Output Voltage	P0$_0$ to P0$_7$, P1$_0$ to P1$_7$, P2$_0$ to P2$_7$, P3$_0$ to P3$_7$, P6$_0$ to P6$_7$, P7$_0$ to P7$_7$, P8$_0$ to P8$_7$, P9$_0$ to P9$_3$, P9$_5$ to P9$_7$, P10$_0$ to P10$_7$, X_{OUT}			-0.3 to V_{CC}+0.3	V
Pd	Power Dissipation			-40≤Topr≤85° C	300	mW
				85≤Topr≤125° C	200	mW
Topr	Operating Ambient Temperature	during CPU operation			-40 to 125	° C
		during flash memory program and erase operation	Program Space (Block 0 to Block 5)		0 to 60	° C
			Data Space (Block A, Block B)		-40 to 125	° C
Tstg	Storage Temperature				-65 to 150	° C

Vcc = 5V

Timing Requirements

(Vcc=5V, Vss=0V, at Topr=-40 to 125°C unless otherwise specified)

Table 21.86 External Clock Input (XIN input)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
tc	External Clock Input Cycle Time	Topr=-40° C to 105° C	50		ns
		Topr=-40° C to 125° C	62.5		ns
$tw_{(H)}$	External Clock Input High ("H") Width	Topr=-40° C to 105° C	20		ns
		Topr=-40° C to 125° C	25		ns
$tw_{(L)}$	External Clock Input Low ("L") Width	Topr=-40° C to 105° C	20		ns
		Topr=-40° C to 125° C	25		ns
tr	External Clock Rise Time	Topr=-40° C to 105° C		9	ns
		Topr=-40° C to 125° C		15	ns
tf	External Clock Fall Time	Topr=-40° C to 105° C		9	ns
		Topr=-40° C to 125° C		15	ns

6. When a count is started and the first effective edge is input, an undefined value is transferred to the reload register. At this time, timer Bi interrupt request is not generated.

7. A value of the counter is undefined at the beginning of a count. MR3 may be set to 1 and timer Bi interrupt request may be generated between a count start and an effective edge input.

8. For pulse width measurement, pulse widths are successively measured. Use program to check whether the measurement result is an “H” level width or an “L” level width.

22.6.3 Three-phase Motor Control Timer Function

When the IVPCR1 bit in the TB2SC register is set to 1 (three-phase output forced cutoff by SD pin input (high-impedance) enabled), the INV03 bit in the INVC0 register is set to 1 (three-phase motor control timer output enabled), and a low-level ("L") signal is applied to the $\overline{SD}$ pin while a three-phase PWM signal is output, the MCU is forced to cutoff and pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ are placed in a high-impedance state and the INV03 bit is set to 0 (three-phase motor control timer output disabled).
To resume the three-phase PWM signal output from pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$, set the INV03 bit to 1 and the IVPCR1 bit to 0 (three-phase output forced cutoff disabled) after the $\overline{SD}$ pin level becomes "H". Then set the IVPCR1 bit to 1 (three-phase output forced cutoff enabled) in order to enable the three-phase output forced cutoff function by input to the SD pin again.
The INV03 bit cannot be set to 1 while an "L" signal is input to the $\overline{SD}$ pin. To set the INV03 bit to 1 after forcible cutoff, write 1 to the INV03 bit and read the bit to ensure that it is set to 1 by program. Then set the IVPCR1 bit to 1 after setting it to 0.

22.15 Flash Memory Version

22.15.1 Functions to Inhibit Rewriting Flash Memory Rewrite

ID codes are stored in addresses 0FFFDF16, 0FFFE316, 0FFFEB16, 0FFFEF16, 0FFFF316, 0FFFF716, and 0FFFFB16. If wrong data are written to theses addresses, the flash memory cannot be read or written in standard serial I/O mode.

The ROMCP register is mapped in address 0FFFFF16. If wrong data is written to this address, the flash memory cannot be read or written in parallel I/O mode.

In the flash memory version of MCU, these addresses are allocated to the vector addresses ("H") of fixed vectors. The b3 to b0 in address 0FFFFF16 are reserved bits. Set these bits to 11112.

22.15.2 Stop Mode

When the MCU enters stop mode, execute the instruction which sets the CM10 bit to 1 (stop mode) after setting the FMR01 bit to 0 (CPU rewrite mode disabled) and disabling the DMA transfer.

22.15.3 Wait Mode

When the MCU enters wait mode, excute the WAIT instruction after setting the FMR01 bit to 0 (CPU rewrite mode disabled).

22.15.4 Low PowerDissipation Mode, On-Chip Oscillator Low Power Dissipation Mode

If the CM05 bit is set to 1 (main clock stop), the following commands must not be executed.

- Program
- Block erase

22.15.5 Writing Command and Data

Write the command code and data at even addresses.

22.15.6 Program Command

Write xx4016 in the first bus cycle and write data to the write address in the second bus cycle, and an auto program operation (data program and verify) will start. Make sure the address value specified in the first bus cycle is the same even address as the write address specified in the second bus cycle.

22.15.7 Operation Speed

When CPU clock source is main clock, before entering CPU rewrite mode (EW mode 0 or 1), select 10 MHz or less for BCLK using the CM06 bit in the CM0 register and bits CM17 to CM16 in the CM1 register.

Also, when CPU clock is f3(ROC) on-chip oscillator clock, before entering CPU rewrite mode (EW mode 0 or 1), set the ROCR3 to ROCR2 bits in the ROCR register to “divied by 4” or “divide by 8”.

On both cases, set the PM17 bit in the PM1 register to 1 (with wait state).

22.15.8 Instructions Inhibited Against Use

The following instructions cannot be used in EW mode 0 because the flash memory’s internal data is referenced: UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction

Rev.	Date	Description	
		Page	Summary
		258	• **Figure 16.3 S00 Register** Note is modified
		259	• **Figure 16.4 S1D0 Register** Reserved bit map modified
		260	• **Figure 16.5 S10 Register** b7-b6 modified
		262	• **Figure 16.7 S4D0 Register** Bit reserved map is modified
		269	• **16.5.1 Bit 0: Last Receive Bit (LRB)** modified
			• **16.5.2 Bit 1: General call detection flag (ADR0)** modified, note 1 modified
			• **16.5.3 Bit 2: Slave address comparison flag (AAS)** modified
		270	• **16.5.5 Bit 4: I^2C Bus Interface Interrupt Request Bit (PIN)** modified
			• **16.5.6 Bit 5: Bus Busy Flag (BB)** Bit names are modified
		271	• **16.5.8 Bit 7: Communication Mode Select bit (MST)** modified
		276	• **16.7.1 Bit0: Time-Out Detection Function Enable Bit (TOE)** is modified
			• **16.7.5 Bit7: STOP Condition Detection Interrupt Request Bit (SCPIN)** is modified
		279	• **16.11 Stop Condition Generation Method** Description added
		282	• **16.13 Address Data Communication** modified
			CAN Module
		292	• **Figure 17.6 C0MCTLj Register** RspLock bit's name changed, note 2 revised
		293	• **Figure 17.7 C0CTLR Register** Note 4 added, functions partially modified
		294	• **Figure 17.8 C0STR Register** Note 1 deleted, functions partially modified
		298	• **Figure 17.13 C0RECR Register** Note 2 deleted, note 1 partially modified
			• **Figure 17.14 C0TECR Register** Note 1 modified, note is relocated
		299	• **Figure 17.15 C0TSR Register** Note 1 modified
		300	• **Figure 17.17 Transition Between Operational Modes** Partially modified
		301	• **17.2.3 CAN Sleep Mode** Partially deleted
		304	• **Table 17.2 Example of Bit-Rate** 24-MHz is deleted
		308	• **17.8 Time Stamp Counter and Time Stamp Function** Partially deleted
		310	• **Figure 17.25 Timing of Receive Data Frame Sequence** IF to IFS
		311	• **Figure 17.26 Timing of Transmit Sequence** IF to IFS
			CRC Calculation Circuit
		313	• **18.1 CRC Snoop** Description partially added
			Programmable I/O Ports
		316	• Note added
			• **19.3 Pull-up Control Register 0 to 2** Description partially added
		317	• **19.6 Digital Debounce Function** Filter width formula modified
		318-321	• **Figure 19.1 I/O Ports (1) to Figure 19.4 I/O Ports (4**) are modified
		326	• **Figure 19.10 PACR Register** Note 1 is modified
		327	• **Figure 19.11 NDDR and P17DDR Register** Functions modified, notes are added
		328	• **Figure 19.12 Functioning of Digital Debounce Filter** modified, procedure note modified