Renesas Electronics America Inc - M30291FATHP#U3AAU3 Datasheet

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2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word "register," "bit," or "pin" to distinguish the three categories.

Examples the PM03 bit in the PM0 register
P3_5 pin, VCC pin

(2) Notation of Numbers

The indication "$_2$" is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication "$_{16}$" is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11_2
Hexadecimal: $EFA0_{16}$
Decimal: 1234

Table 4.3 SFR Information (3)

Address	Register	Symbol	After reset
0080₁₆	CAN0 message box 2: Identifier/DLC		XX₁₆
0081₁₆			XX₁₆
0082₁₆			XX₁₆
0083₁₆			XX₁₆
0084₁₆			XX₁₆
0085₁₆			XX₁₆
0086₁₆	CAN0 message box 2 : Data field		XX₁₆
0087₁₆			XX₁₆
0088₁₆			XX₁₆
0089₁₆			XX₁₆
008A₁₆			XX₁₆
008B₁₆			XX₁₆
008C₁₆			XX₁₆
008D₁₆			XX₁₆
008E₁₆	CAN0 message box 2 : Time stamp		XX₁₆
008F₁₆			XX₁₆
0090₁₆	CAN0 message box 3 : Identifier/DLC		XX₁₆
0091₁₆			XX₁₆
0092₁₆			XX₁₆
0093₁₆			XX₁₆
0094₁₆			XX₁₆
0095₁₆			XX₁₆
0096₁₆	CAN0 message box 3 : Data field		XX₁₆
0097₁₆			XX₁₆
0098₁₆			XX₁₆
0099₁₆			XX₁₆
009A₁₆			XX₁₆
009B₁₆			XX₁₆
009C₁₆			XX₁₆
009D₁₆			XX₁₆
009E₁₆	CAN0 message box 3 : Time stamp		XX₁₆
009F₁₆			XX₁₆
00A0₁₆	CAN0 message box 4: Identifier/DLC		XX₁₆
00A1₁₆			XX₁₆
00A2₁₆			XX₁₆
00A3₁₆			XX₁₆
00A4₁₆			XX₁₆
00A5₁₆			XX₁₆
00A6₁₆	CAN0 message box 4 : Data field		XX₁₆
00A7₁₆			XX₁₆
00A8₁₆			XX₁₆
00A9₁₆			XX₁₆
00AA₁₆			XX₁₆
00AB₁₆			XX₁₆
00AC₁₆			XX₁₆
00AD₁₆			XX₁₆
00AE₁₆	CAN0 message box 4 : Time stamp		XX₁₆
00AF₁₆			XX₁₆
00B0₁₆	CAN0 message box 5 : Identifier/DLC		XX₁₆
00B1₁₆			XX₁₆
00B2₁₆			XX₁₆
00B3₁₆			XX₁₆
00B4₁₆			XX₁₆
00B5₁₆			XX₁₆
00B6₁₆	CAN0 message box 5 : Data field		XX₁₆
00B7₁₆			XX₁₆
00B8₁₆			XX₁₆
00B9₁₆			XX₁₆
00BA₁₆			XX₁₆
00BB₁₆			XX₁₆
00BC₁₆			XX₁₆
00BD₁₆			XX₁₆
00BE₁₆	CAN0 message box 5 : Time stamp		XX₁₆
00BF₁₆			XX₁₆

Note 1: The blank areas are reserved and cannot be used by users.

X : Undefined

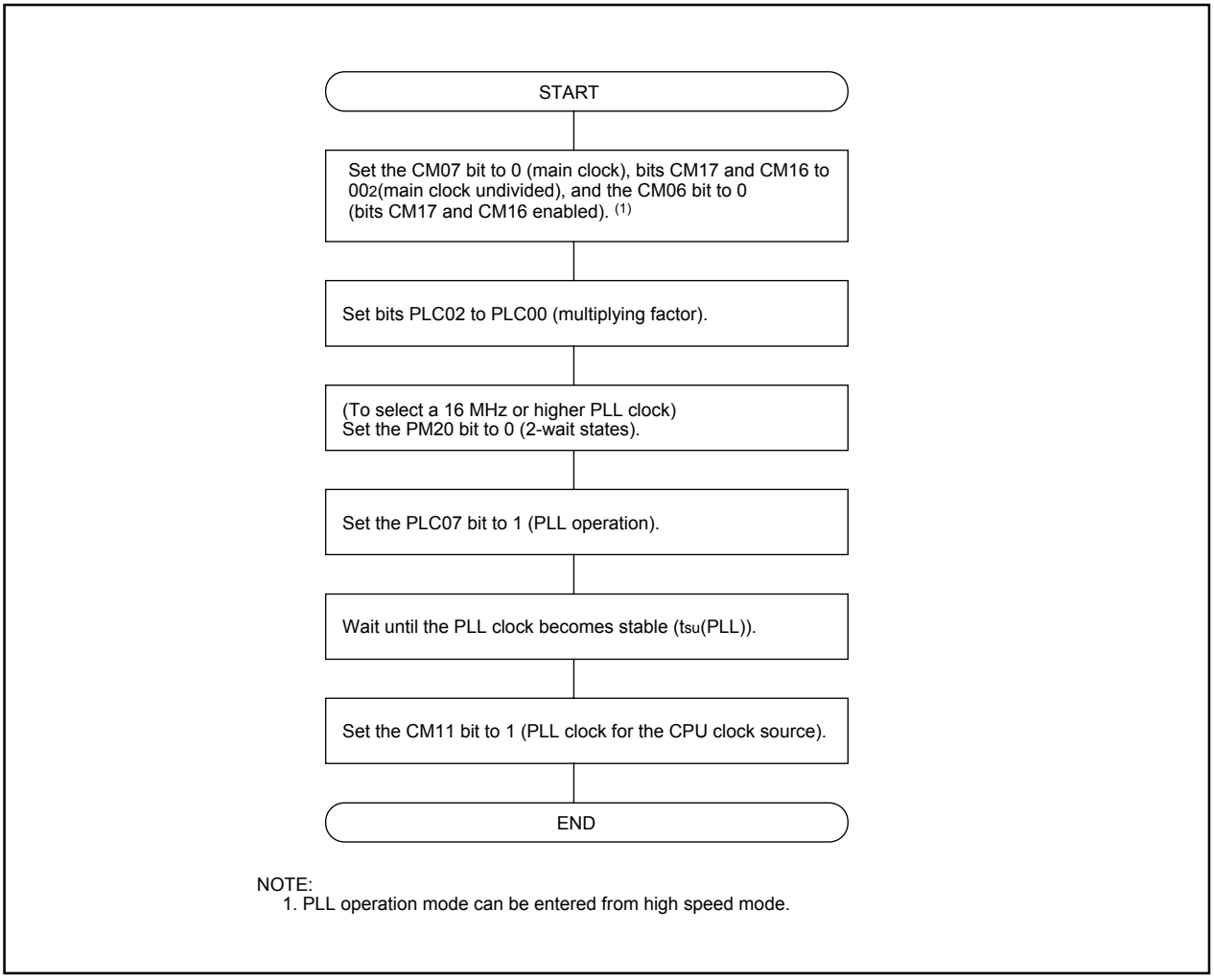


Figure 7.10 Procedure to Use PLL Clock as CPU Clock Source

Timer Ai Mode Register (i=0 to 4)
(When not using two-phase pulse signal processing)

b7	b6	b5	b4	b3	b2	b1	b0
		0				0	1

Symbol	Address	After Reset
TA0MR to TA4MR	039616 to 039A16	0016

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 1 : Event counter mode (1)	RW
TMOD1			RW
MR0	Pulse output function select bit	0: Pulse is not output (TAiOUT pin functions as I/O port) 1: Pulse is output (TAiOUT pin functions as pulse output pin)	RW
MR1	Count polarityselect bit (2)	0: Counts external signal's falling edge 1: Counts external signal's rising edge	RW
MR2	Up/down switching cause select bit	0: UDF register 1: Input signal to TAiOUT pin(3)	RW
MR3	Set to 0 in event counter mode		RW
TCK0	Count operation type select bit	0: Reload type 1: Free-run type	RW
TCK1	Can be 0 or 1 when not using two-phase pulse signal processing		RW

NOTES:
1. During event counter mode, the count source can be selected using registers ONSF and TRGSR.
2. Effective when bits TAiTGH and TAiTGL in the ONSF or TRGSR register are 002 (TAiIN pin input).
3. Decrement when input on TAiOUT pin is low or increment when input on that pin is high. The port direction bit for TAiOUT pin must be set to 0 (input mode).

Figure 12.8 TAiMR Register in Event Counter Mode (when not using two-phase pulse signal processing)

12.1.4 Pulse Width Modulation (PWM) Mode

In PWM mode, the timer outputs pulses of a given width in succession (see **Table 12.5**). The counter functions as either 16-bit pulse width modulator or 8-bit pulse width modulator. **Figure 12.12** shows TAiMR register in pulse width modulation mode. **Figures 12.13** and **12.14** show examples of how a 16-bit pulse width modulator operates and how an 8-bit pulse width modulator operates.

Table 12.5 Specifications in Pulse Width Modulation Mode

Item	Specification
Count source	f_1, f_2, f_8, f_{32}, f_{C32}
Count operation	• Decrement (operating as an 8-bit or a 16-bit pulse width modulator) • The timer reloads a new value at a rising edge of PWM pulse and continues counting • The timer is not affected by a trigger that occurs during counting
16-bit PWM	• High level width n / fj n : set value of TAi register (i=o to 4) • Cycle time $(2^{16}-1)$ / fj fixed fj: count source frequency (f_1, f_2, f_8, f_{32}, f_{C32})
8-bit PWM	• High level width n x (m+1) / fj n : set value of TAi register high-order address • Cycle time (2^8-1) x (m+1) / fj m : set value of TAi register low-order address
Count start condition	• TAiS bit in the TABSR register is set to 1 (= start counting) • The TAiS bit = 1 and external trigger input from the TAiIN pin • The TAiS bit = 1 and one of the following external triggers occurs • Timer B2 overflow or underflow, timer Aj (j=i-1, except j=4 if i=0) overflow or underflow, timer Ak (k=i+1, except k=0 if i=4) overflow or underflow
Count stop condition	TAiS bit is set to 0 (stop counting)
Interrupt request generation timing	PWM pulse goes “L”
TAiIN pin function	I/O port or trigger input
TAiOUT pin function	Pulse output
Read from timer	An undefined value is read by reading TAi register
Write to timer	• When not counting and until the 1st count source is input after counting start Value written to TAi register is written to both reload register and counter • When counting (after 1st count source input) Value written to TAi register is written to only reload register (Transferred to counter when reloaded next)

Timer B2 Special Mode Register (1)

b7	b6	b5	b4	b3	b2	b1	b0
X	0	0					

Symbol	Address	After Reset
TB2SC	039E16	X0000000₂

Bit Symbol	Bit Name	Function	RW
PWCON	Timer B2 reload timing switch bit (2)	0: Timer B2 underflow 1: Timer A output at odd-numbered	RW
IVPCR1	Three-phase output port $\overline{SD}$ control bit 1 (3, 4, 7)	0: Three-phase output forcible cutoff by $\overline{SD}$ pin input (high impedance) disabled 1: Three-phase output forcible cutoff by $\overline{SD}$ pin input (high impedance) enabled	RW
TB0EN	Timer B0 operation mode select bit	0: Other than A/D trigger mode 1: A/D trigger mode (5)	RW
TB1EN	Timer B1 operation mode select bit	0: Other than A/D trigger mode 1: A/D trigger mode (5)	RW
TB2SEL	Trigger select bit (6)	0: TB2 interrupt 1: Underflow of TB2 interrupt generation frequency setting counter [ICTB2]	RW
$\overline{\text{(b6-b5)}}$	Reserved bits	Set to 0	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. Write to this register after setting the PRC1 bit in the PRCR register to 1 (write enabled).
2. If the INV11 bit is 0 (three-phase mode 0) or the INV06 bit is 1 (triangular wave modulation mode), set this bit to 0 (timer B2 underflow).
3. When setting the IVPCR1 bit to 1 (three-phase output forcible cutoff by $\overline{SD}$ pin input enabled), Set the PD8$_5$ bit to 0 (= input mode).
4. Related pins are U(P8$_0$), $\overline{U}$(P8$_1$), V(P7$_2$), $\overline{V}$(P7$_3$), W(P7$_4$), $\overline{W}$(P7$_5$). When a high-level ("H") signal is applied to the $\overline{SD}$ pin and set the IVPCR1 bit to 0 after forcible cutoff, pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ are exit from the high-impedance state. If a low-level ("L") signal is applied to the $\overline{SD}$ pin, three-phase motor control timer output will be disabled (INV03=0). At this time, when the IVPCR1 bit is 0, pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ become programmable I/O ports. When the IVPCR1 bit is set to 1, pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ are placed in a high-impedance state regardless of which function of those pins is used.
5. When this bit is used in delayed trigger mode 0, set bits TB0EN and TB1EN to 1 (A/D trigger mode).
6. When setting the TB2SEL bit to 1 (underflow of TB2 interrupt generation frequency setting counter[ICTB2]), set the INV02 bit to 1 (three-phase motor control timer function).
7. Refer to "**19.6 Digital Debounce Function**" for the $\overline{SD}$ input.

The effect of $\overline{SD}$ pin input is below.
1.Case of INV03 = 1(Three-phase motor control timer output enabled)

IVPCR1 bit	$\overline{SD}$ pin inputs(3)	Status of U/V/W pins	Remarks
1 (Three-phase output forcrible cutoff enable)	H	Three-phase PWM output	
	L(1)	High impedance(4)	Three-phase output forcrible cutoff
0 (Three-phase output forcrible cutoff disable)	H	Three-phase PWM output	
	L(1)	Input/output port(2)	

NOTES:
1. When "L" is applied to the $\overline{SD}$ pin, INV03 bit is changed to 0 at the same time.
2. The value of the port register and the port direction register becomes effective.
3. When $\overline{SD}$ function is not used, set to 0 (Input) in PD8$_5$ and pullup to "H" in $\overline{SD}$ pin from outside.
4. To leave the high-impedance state and restart the three-phase PWM signal output after the three-phase PWM signal output forced cutoff, set the IVPCR1 bit to 0 after the $\overline{SD}$ pin input level becomes high ("H").

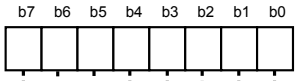
2.Case of INV03 = 0(Three-phase motor control timer output disabled)

IVPCR1 bit	$\overline{SD}$ pin inputs	Status of U/V/W pins	Remarks
1 (Three-phase output forcrible cutoff enable)	H	Peripheral input/output or input/output port	
	L	High impedance	Three-phase output forcrible cutoff(1)
0 (Three-phase output forcrible cutoff disable)	H	Peripheral input/output or input/output port	
	L	Peripheral input/output or input/output port	

NOTE:
1. The three-phase output forcrible cutoff function becomes effective if the INPCR1 bit is set to 1 (three-phase output forcrible cutoff function enable) even when the INV03 bit is 0 (three-phase motor control timer output disalbe)

Figure 12.30 TB2SC Register

Time Measurement Control Register j (j=0 to 7)

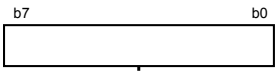


Symbol	Address	After Reset
G1TMCR0 to G1TMCR3	0318_{16}, 0319_{16}, $031A_{16}$, $031B_{16}$	00_{16}
G1TMCR4 to G1TMCR7	$031C_{16}$, $031D_{16}$, $031E_{16}$, $031F_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
CTS0	Time measurement trigger select bit	b1 b0 0 0: No time measurement 0 1: Rising edge 1 0: Falling edge 1 1: Both edges	RW
CTS1			RW
DF0	Digital filter function select bit	b3 b2 0 0: No digital filter 0 1: Do not set to this value 1 0: f_{BT1} 1 1: f_1 or f_2 (1)	RW
DF1			RW
GT	Gate function select bit (2)	0: Gate function is not used 1: Gate function is used	RW
GOC	Gate function clear select bit (2, 3, 4)	0: Not cleared 1: The gate is cleared when the base timer matches the G1POk register	RW
GSC	Gate function clear bit (2, 3)	The gate is cleared by setting the GSC bit to 1	RW
PR	Prescaler function select bit (2)	0: Not used 1: Used	RW

NOTES:
1. When the PCLK0 bit in the PCLKR register is set to 0, the count source is f_2 cycles. And when the PCLK0 bit is set to 1, the count source is f_1 cycles.
2. These bits are in registers G1TMCR6 and G1TMCR7. Set all bits 4 to 7 in registers G1TMCR0 to G1TMCR5 to 0.
3. These bits are enabled when the GT bit is set to 1.
4. The GOC bit is set to 0 after the gate function is cleared. See **Figure 13.7** for details on the G1POk register (k=4 when j=6 and k=5 when j=7).

Time Measurement Prescale Register j (j=6,7)(1)



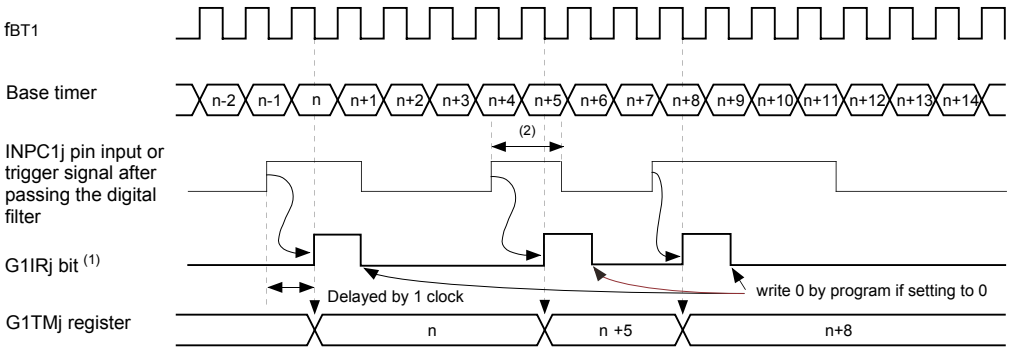
Symbol	Address	After Reset
G1TPR6 to G1TPR7	0324_{16}, 0325_{16}	00_{16}

Function	Setting Range	RW
As the setting value is n, time is measured whenever a trigger input is counted by *n+1* (2)	00_{16} to FF_{16}	RW

NOTES:
1. The G1TPR6 to G1TPR7 registers reflect the base timer value, synchronizing with the count source f_{BT1} cycles.
2. The first prescaler, after the PR bit in the G1TMCRj register is changed from 0 (not used) to 1 (used), may be divided by *n*, rather than *n+1*. The subsequent prescaler is divided by *n+1*.

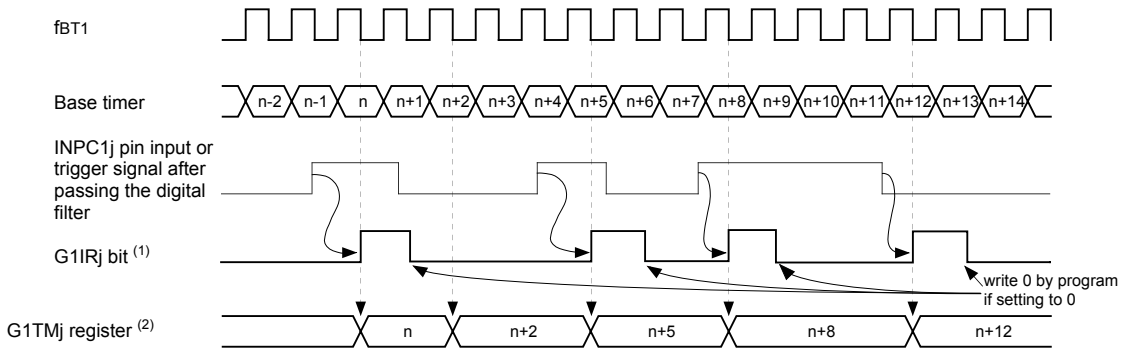
Figure 13.5 G1TMCR0 to G1TMCR7 Registers, and G1TPR6 to G1TPR7 Registers

(a) When selecting the rising edge as a timer measurement trigger
(Bits CTS1 and CTS0 in the G1TMCRj register (j=0 to 7)=01$_2$)



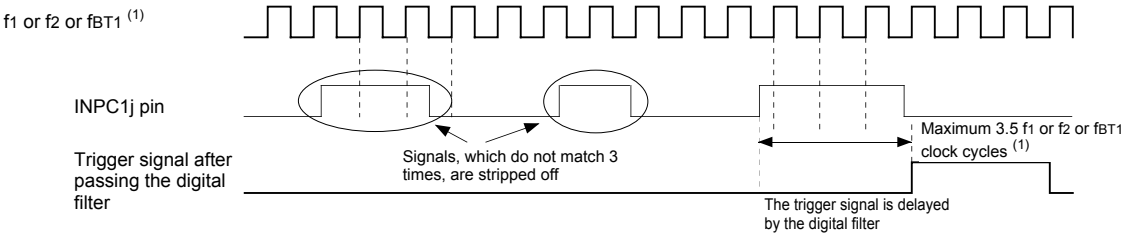
NOTES :
1. Bits in the G1IR register.
2. Input pulse applied to the INPC1j pin requires 1.5 fBT1 clock cycles or more.

(b) When selecting both edges as a timer measurement trigger
(Bits CTS1 and CTS0 = 11$_2$)



NOTES :
1. Bits in the G1IR register.
2. No interrupt is generated if the MCU receives a trigger signal when the G1IRj bit is set to 1. However, the value of the G1TMj register is updated.

(c) Trigger signal when using digital filter
(Bits DF1 to DF0 in the G1TMCRj register =10$_2$ or 11$_2$)



NOTE:
1. fBT1 when bits DF1 to DF0 are set to 10$_2$, and f1 or f2 when set to 11$_2$.

Figure 13.20 Time Measurement Function (2)

Table 14.11 Registers to Be Used and Settings in I^2C bus mode (1) (Continued)

Register	Bit	Function	
		Master	Slave
U2TB	0 to 7	Set transmission data	Set transmission data
U2RB(1)	0 to 7	Reception data can be read	Reception data can be read
	8	ACK or NACK is set in this bit	ACK or NACK is set in this bit
	ABT	Arbitration lost detection flag	Invalid
	OER	Overrun error flag	Overrun error flag
U2BRG	0 to 7	Set bit rate	Invalid
U2MR(1)	SMD2 to SMD0	Set to 010_2	Set to 010_2
	CKDIR	Set to 0	Set to 1
	IOPOL	Set to 0	Set to 0
U2C0	CLK1, CLK0	Select the count source for the U2BRG register	Invalid
	CRS	Invalid because CRD = 1	Invalid because CRD = 1
	TXEPT	Transmit buffer empty flag	Transmit buffer empty flag
	CRD	Set to 1	Set to 1
	NCH	Set to 1	Set to 1
	CKPOL	Set to 0	Set to 0
	UFORM	Set to 1	Set to 1
U2C1	TE	Set this bit to 1 to enable transmission	Set this bit to 1 to enable transmission
	TI	Transmit buffer empty flag	Transmit buffer empty flag
	RE	Set this bit to 1 to enable reception	Set this bit to 1 to enable reception
	RI	Reception complete flag	Reception complete flag
	U2IRS	Invalid	Invalid
	U2RRM, U2LCH, U2ERE	Set to 0	Set to 0
U2SMR	IICM	Set to 1	Set to 1
	ABC	Select the timing at which arbitration-lost is detected	Invalid
	BBS	Bus busy flag	Bus busy flag
	3 to 7	Set to 0	Set to 0
U2SMR2	IICM2	Refer to **Table 14.13**	Refer to **Table 14.13**
	CSC	Set this bit to 1 to enable clock synchronization	Set to 0
	SWC	Set this bit to 1 to have SCL_2 output fixed to L at the falling edge of the 9th bit of clock	Set this bit to 1 to have SCL_2 output fixed to “L” at the falling edge of the 9^{th} bit of clock
	ALS	Set this bit to 1 to have SDA_2 output stopped when arbitration-lost is detected	Set to 0
	STAC	Set to 0	Set this bit to 1 to initialize UART2 at start condition detection
	SWC2	Set this bit to 1 to have SCL_2 output forcibly pulled low	Set this bit to 1 to have SCL_2 output forcibly pulled low
	SDHI	Set this bit to 1 to disable SDA_2 output	Set this bit to 1 to disable SDA_2 output
	7	Set to 0	Set to 0
U2SMR3	0, 2, 4 and NODC	Set to 0	Set to 0
	CKPH	Refer to **Table 14.13**	Refer to **Table 14.13**
	DL2 to DL0	Set the amount of SDA_2 digital delay	Set the amount of SDA_2 digital delay

NOTE:

1. Not all bits in the register are described above. Set those bits to 0 when writing to the registers in I^2C bus mode.

A/D Control Register 0 (1)

b7	b6	b5	b4	b3	b2	b1	b0
			1	0			

Symbol	Address	After Reset
ADCON0	$03D6_{16}$	$00000XXX_2$

Bit Symbol	Bit Name	Function	RW
CH0	Analog input pin select bit	Invalid in single sweep mode	RW
CH1			RW
CH2			RW
MD0	A/D operation mode select bit 0	b4 b3 1 0: Single sweep mode or Simultaneous sample sweep mode	RW
MD1			RW
TRG	Trigger select bit	0: Software trigger 1: Hardware trigger ($\overline{\text{ADTRG}}$ trigger)	RW
ADST	A/D conversion start flag	0: A/D conversion disabled 1: A/D conversion started	RW
CKS0	Frequency select bit 0	See **Table 15.2**	RW

NOTE:
1. If the ADCON0 register is rewritten during A/D conversion, the conversion result will be undefined.

A/D Control Register 1 (1)

b7	b6	b5	b4	b3	b2	b1	b0
X	X	1			0		

Symbol	Address	After Reset
ADCON1	$03D7_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
SCAN0	A/D sweep pin select bit (2)	When single sweep mode is selected, b1 b0 0 0: AN_0 to AN_1 (2 pins) 0 1: AN_0 to AN_3 (4 pins) 1 0: AN_0 to AN_5 (6 pins) 1 1: AN_0 to AN_7 (8 pins)	RW
SCAN1			RW
MD2	A/D operation mode select bit 1	0: Other than repeat sweep mode 1	RW
BITS	8/10-bit mode select bit	0: 8-bit mode 1: 10-bit mode	RW
CKS1	Frequency select bit 1	See **Table 15.2**	RW
VCUT	Vref connect Bit (3)	1: Vref connected	RW
$\overline{\text{(b7-b6)}}$	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—

NOTES:
1. If the ADCON1 register is rewritten during A/D conversion, the conversion result will be undefined.
2. AN_{00} to AN_{07}, AN_{20} to AN_{27}, and AN_{30} to AN_{32} can be used in the same way as AN_0 to AN_7. Use bits ADGSEL1 and ADGSEL 0 in the ADCON2 register to select the desired pin.
3. If the VCUT bit is reset from 0 (Vref unconnected) to 1 (Vref connected), wait for 1 μs or more before starting A/D conversion.

A/D Control Register 2(1)

b7	b6	b5	b4	b3	b2	b1	b0
X	X	0		0			

Symbol	Address	After Reset
ADCON2	$03D4_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
SMP	A/D conversion method select bit	0: Without sample and hold 1: With sample and hold	RW
ADGSEL0	A/D input group select bit	b2 b1 0 0: Select port P10 group 0 1: Select port P9 group 1 0: Select port P0 group 1 1: Select port P1/P9 group	RW
ADGSEL1			RW
$\overline{\text{(b3)}}$	Reserved bit	Set to 0	RW
CKS2	Frequency select bit 2	See **Table 15.2**	RW
TRG1	Trigger select bit	Set to 0 in single sweep mode	RW
$\overline{\text{(b7-b6)}}$	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—

NOTE:
1. If the ADCON2 register is rewritten during A/D conversion, the conversion result will be undefined.

Figure 15.11 ADCON0 to ADCON2 Registers in Single Sweep Mode

I2C0 Start/stop Condition Control Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
S2D0	02E516	000110102

Bit Symbol	Bit Name	Function	RW
SSC0	START/STOP condition setting bits(1)	Setting for detection condition of START/STOP condition. See **Table 16.2**	RW
SSC1			RW
SSC2			RW
SSC3			RW
SSC4			RW
SIP	SCL/SDA interrupt pin polarity select bit	0: Active in falling edge 1: Active in rising edge	RW
SIS	SCL/SDA interrupt pin select bit	0: SDA enabled 1: SCL enabled	RW
STSPSEL	START/STOP condition generation select bit	0: Short setup/hold time mode 1: Long setup/hold time mode	RW

NOTE:
1. Do not set 000002 or odd values.

Figure 16.8 S2D0 Register

Table 16.2 Recommended setting (SSC4-SSC0) start/stop condition at each oscillation frequency

Oscillation f1 (MHz)	I2C bus system clock select	I2C bus system clock(MHz)	SSC4-SSC0(1)	SCL release time (cycle)	Setup time (cycle)	Hold time (cycle)
10	1 / 2f1(2)	5	XXX11110	6.2 µs (31)	3.2 µs (16)	3.0 µs (15)
8	1 / 2f1(2)	4	XXX11010	6.75 µs(27)	3.5 µs (14)	3.25 µs(13)
			XXX11000	6.25 µs(25)	3.25 µs (13)	3.0 µs (12)
8	1 / 8f1(2)	1	XXX00100	5.0 µs (5)	3.0 µs (3)	2.0 µs (2)
4	1 / 2f1(2)	2	XXX01100	6.5 µs (13)	3.5 µs (7)	3.0 µs (6)
			XXX01010	5.5 µs (11)	3.0 µs (6)	2.5 µs (5)
2	1 / 2f1(2)	1	XXX00100	5.0 µs (5)	3.0 µs (3)	2.0 µs (2)

NOTES:
1. Do not set odd values or 000002 to START/STOP condition setting bits (SSC4 to SSC0)
2. When the PCLK0 bit in the PCLKR register is set to 1.

16.4.5 Bit 7: I2C bus Interface Pin Input Level Select Bit (TISS)

The TISS bit selects the input level of the SCL and SDA pins for the multi-master I2C bus interface. When the TISS bit is set to 1, the P20 and P21 become the SMBus input level.

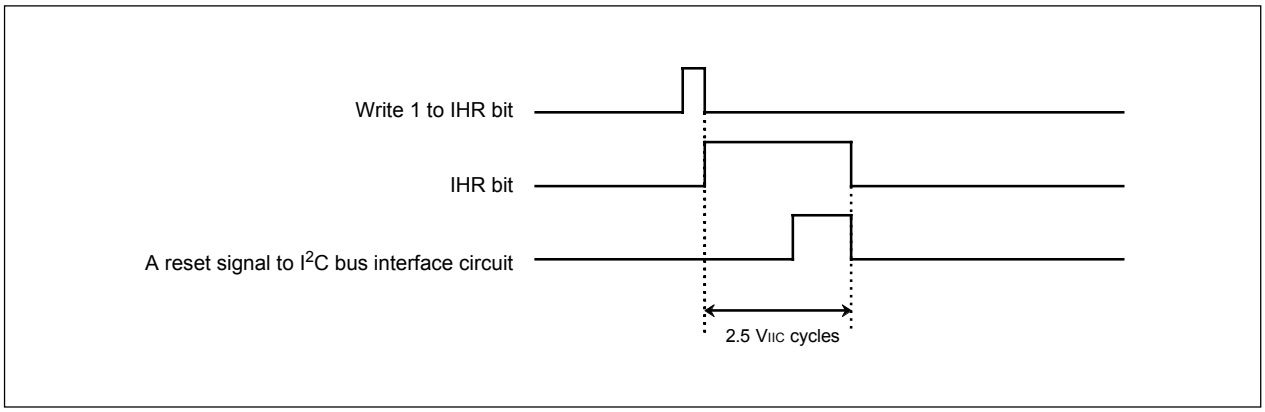


Figure 16.10 The timing of reset to the I2C bus interface circuit

ROM Code Protect Control Address(5)

b7	b6	b5	b4	b3	b2	b1	b0
				1	1	1	1

Symbol: ROMCP
Address: 0FFFFF16
Factory Setting: FF16 (4)

Bit Symbol	Bit Name	Function	RW
$\overline{(b5\text{-}b0)}$	Reserved Bit	Set to 1	RW
ROMCP1	ROM Code Protect Level 1 Set Bit (1, 2, 3, 4)	b7 b6 00: } Enables protect 01: } 10: 11: Disables protect	RW RW

NOTES:
1. When the ROM code protect is active by the ROMCP1 bit setting, the flash memory is protected against reading or rewriting in parallel I/O mode.
2. Set the bit 5 to bit 0 to 1111112 when the ROMCP1 bit is set to a value other than 112. When the bit 5 to bit 0 are set to values other than 1111112, the ROM code protection may not become active by setting the ROMCP1 bit to a value other than 112.
3. To make the ROM code protection inactive, erase a block including the ROMCP address in standard serial I/O mode or CPU rewrite mode.
4. The ROMCP address is set to FF16 when a block, including the ROMCP address, is erased.
5. When a value of the ROMCP address is 0016 or FF16, the ROM code protect function is disabled.

Figure 20.4 ROMCP Address

Address		
0FFFDF16 to 0FFFDC16	ID1	Undefined instruction vector
0FFFE316 to 0FFFE016	ID2	Overflow vector
0FFFE716 to 0FFFE416		BRK instruction vector
0FFFEB16 to 0FFFE816	ID3	Address match vector
0FFFEF16 to 0FFFEC16	ID4	Single step vector
0FFFF316 to 0FFFF016	ID5	Watchdog timer vector
0FFFF716 to 0FFFF416	ID6	$\overline{\text{DBC}}$ vector
0FFFFB16 to 0FFFF816	ID7	$\overline{\text{NMI}}$ vector
0FFFFF16 to 0FFFFC16	ROMCP	Reset vector

4 bytes

Figure 20.5 Address for ID Code Stored

20.8.4 Full Status Check

If an error occurs, bits FMR06 to FMR07 in the FMR0 register are set to 1, indicating a specific error. Therefore, execution results can be comfirmed by verifying these status bits (full status check).

Table 20.7 lists errors and FMR0 register state. **Figure 20.14** shows a flow chart of the full status check and handling procedure for each error.

Table 20.7 Errors and FMR0 Register Status

FMR0 register (SRD register) status		Error	Error occurrence condition
FMR07 (SR5)	FMR06 (SR4)		
1	1	Command sequence error	• An incorrect commands is written • A value other than xxD0$_{16}$ or xxFF$_{16}$ is written in the second bus cycle of the block erase command (1) • When the block erase command is executed on an protected block • When the program command is executed on protected blocks
1	0	Erase error	• The block erase command is executed on an unprotected block but the program operation is not successfully completed
0	1	Program error	• The program command is executed on an unprotected block but the program operation is not successfully completed

Note 1: The flash memory enters read array mode by writing command code xxFF$_{16}$ in the second bus cycle of these commands. The command code written in the first bus cycle becomes invalid.

Table 20.8 Pin Descriptions (Flash Memory Standard Serial I/O Mode)

Pin	Name		I/O	Descriptio n
VCC,VSS	Power input			Apply the voltage guaranteed for Program and Erase to Vcc pin and 0 V to Vss pin.
CNVSS	CNVSS		I	Connect to Vcc pin.
$\overline{\text{RESET}}$	Reset input		I	Reset input pin. While $\overline{\text{RESET}}$ pin is “L”, wait for td(ROC).
XIN	Clock input		I	Connect a ceramic resonator or crystal oscillator between XIN and XOUT pins. To input an externally generated clock, input it to XIN pin and open XOUT pin.
XOUT	Clock output		O	
AVCC, AVSS	Analog power supply input			Connect AVss to Vss and AVcc to Vcc, respectively.
VREF	Reference voltage input		I	Enter the reference voltage for AD conversion.
P00 to P07	Input port P0		I	Input “H” or “L” signal or leave open.
P10 to P15, P17	Input port P1		I	Input “H” or “L” signal or leave open.
P16	Input port P1		I	Connect this pin to Vcc while $\overline{\text{RESET}}$ pin is “L”. (2)
P20 to P27	Input port P2		I	Input "H" or “L” level signal or leave open.
P30 to P37	Input port P3		I	Input "H" or “L” level signal or leave open.
P60 to P63	Input port P6		I	Input "H" or “L” level signal or leave open.
P64	BUSY output		O	Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 2: Monitor signal output pin for boot program operation check
P65	SCLK input		I	Standard serial I/O mode 1: Serial clock input pin Standard serial I/O mode 2: Input “L”.
P66	RxD input		I	Serial data input pin
P67	TxD output		O	Serial data output pin (1)
P70 to P77	Input port P7		I	Input “H” or “L” signal or leave open.
P80 to P84, P87	Input port P8		I	Input “H” or “L” signal or leave open.
P85	$\overline{\text{RP}}$ input		I	Connect this pin to Vss while $\overline{\text{RESET}}$ pin is “L”. (2)
P86	$\overline{\text{CE}}$ input		I	Connect this pin to Vcc while $\overline{\text{RESET}}$ pin is “L”. (2)
P90 to P92, P95 to P97	Input port P9		I	Input “H” or “L” signal or leave open.
P93	Input port P93	Normal-ver.	I/O	“H” signal is output for specific time. Input “H” signal or leave open.
		T-ver./V-ver.	I	Input “H” or “L” signal or leave open.
P100 to P107	Input port P10		I	Input “H” or “L” signal or leave open.

NOTES:

1. When using standard serial I/O mode 1, to input “H” to the TxD pin is necessary while the $\overline{\text{RESET}}$ pin is held “L”. Therefore, connect this pin to VCC via a resistor. Adjust the pull-up resistor value on a system not to affect a data transfer after reset, because this pin changes to a data-output pin
2. Set the following, either or both.
   -Connect the $\overline{\text{CE}}$ pin to VCC.
   -Connect the $\overline{\text{RP}}$ pin to VSS and P16 pin to VCC.

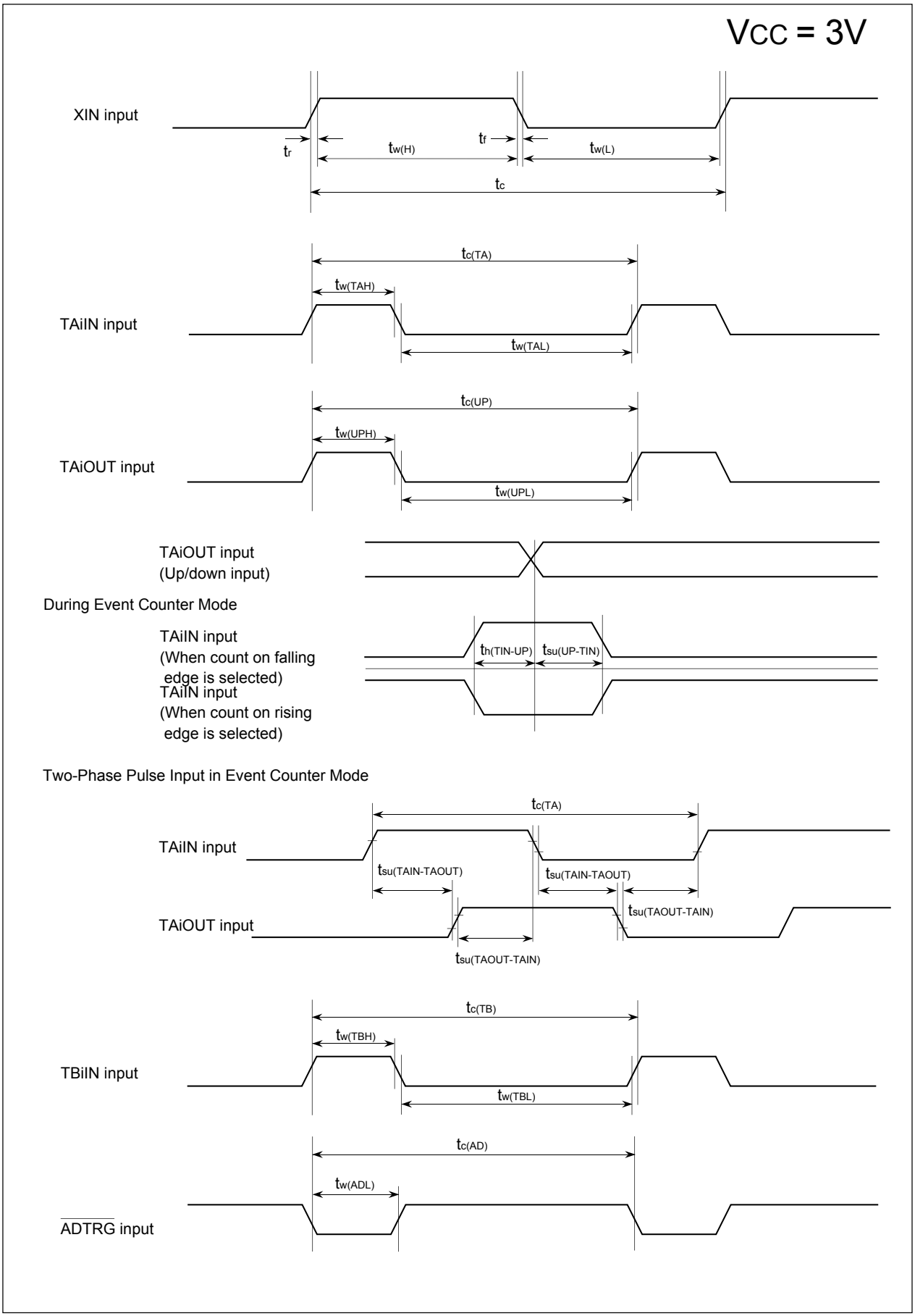


Figure 21.10 Timing Diagram (1)

22.5 DMAC

22.5.1 Write to DMAE Bit in DMiCON Register

When both of the conditions below are met, follow the steps below.

(a) Conditions
- The DMAE bit is set to 1 again while it remains set (DMAi is in an active state).
- A DMA request may occur simultaneously when the DMAE bit is being written.

(b) Procedure

(1) Write 1 to the DMAE bit and DMAS bit in DMiCON register simultaneously(1).

(2) Make sure that the DMAi is in an initial state(2) in a program.

If the DMAi is not in an initial state, the above steps should be repeated.

NOTES:

1. The DMAS bit remains unchanged even if 1 is written. However, if 0 is written to this bit, it is set to 0 (DMA not requested). In order to prevent the DMAS bit from being modified to 0, 1 should be written to the DMAS bit when 1 is written to the DMAE bit. In this way the state of the DMAS bit immediately before being written can be maintained.
   Similarly, when writing to the DMAE bit with a read-modify-write instruction, 1 should be written to the DMAS bit in order to maintain a DMA request which is generated during execution.

2. Read the TCRi register to verify whether the DMAi is in an initial state. If the read value is equal to a value which was written to the TCRi register before DMA transfer start, the DMAi is in an initial state. (If a DMA request occurs after writing to the DMAE bit, the value written to the TCRi register is 1.) If the read value is a value in the middle of transfer, the DMAi is not in an initial state.

22.14 Mask ROM Version

22.14.1 Internal ROM Area

In the masked ROM version, do not write to internal ROM area. Writing to the area may increase power consumption.

22.14.2 Reserved Bit

The b3 to b0 in addresses $0FFFFF_{16}$ are reserved bits. Set these bits to 1111_2.

22.15 Flash Memory Version

22.15.1 Functions to Inhibit Rewriting Flash Memory Rewrite

ID codes are stored in addresses 0FFFDF16, 0FFFE316, 0FFFEB16, 0FFFEF16, 0FFFF316, 0FFFF716, and 0FFFFB16. If wrong data are written to theses addresses, the flash memory cannot be read or written in standard serial I/O mode.

The ROMCP register is mapped in address 0FFFFF16. If wrong data is written to this address, the flash memory cannot be read or written in parallel I/O mode.

In the flash memory version of MCU, these addresses are allocated to the vector addresses ("H") of fixed vectors. The b3 to b0 in address 0FFFFF16 are reserved bits. Set these bits to 11112.

22.15.2 Stop Mode

When the MCU enters stop mode, execute the instruction which sets the CM10 bit to 1 (stop mode) after setting the FMR01 bit to 0 (CPU rewrite mode disabled) and disabling the DMA transfer.

22.15.3 Wait Mode

When the MCU enters wait mode, excute the WAIT instruction after setting the FMR01 bit to 0 (CPU rewrite mode disabled).

22.15.4 Low PowerDissipation Mode, On-Chip Oscillator Low Power Dissipation Mode

If the CM05 bit is set to 1 (main clock stop), the following commands must not be executed.

- Program
- Block erase

22.15.5 Writing Command and Data

Write the command code and data at even addresses.

22.15.6 Program Command

Write xx4016 in the first bus cycle and write data to the write address in the second bus cycle, and an auto program operation (data program and verify) will start. Make sure the address value specified in the first bus cycle is the same even address as the write address specified in the second bus cycle.

22.15.7 Operation Speed

When CPU clock source is main clock, before entering CPU rewrite mode (EW mode 0 or 1), select 10 MHz or less for BCLK using the CM06 bit in the CM0 register and bits CM17 to CM16 in the CM1 register.

Also, when CPU clock is f3(ROC) on-chip oscillator clock, before entering CPU rewrite mode (EW mode 0 or 1), set the ROCR3 to ROCR2 bits in the ROCR register to “divied by 4” or “divide by 8”.

On both cases, set the PM17 bit in the PM1 register to 1 (with wait state).

22.15.8 Instructions Inhibited Against Use

The following instructions cannot be used in EW mode 0 because the flash memory’s internal data is referenced: UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction

K

N

O

P

R

S

T

U