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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	55
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30291fchp-u3a

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connection
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Registers
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Quick Reference to Pages Classified by Address

Address	Register	Symbol	Page
0380₁₆	Count start flag	TABSR	104, 118, 132
0381₁₆	Clock prescaler reset flag	CPSRF	105,118
0382₁₆	One-shot start flag	ONSF	105
0383₁₆	Trigger select register	TRGSR	105,132
0384₁₆	Up-down flag	UDF	104
0385₁₆			
0386₁₆ 0387₁₆	Timer A0 register	TA0	104
0388₁₆ 0389₁₆	Timer A1 register	TA1	104
038A₁₆ 038B₁₆	Timer A2 register	TA2	104
038C₁₆ 038D₁₆	Timer A3 register	TA3	104
038E₁₆ 038F₁₆	Timer A4 register	TA4	104
0390₁₆ 0391₁₆	Timer B0 register	TB0	118
0392₁₆ 0393₁₆	Timer B1 register	TB1	118
0394₁₆ 0395₁₆	Timer B2 register	TB2	118
0396₁₆	Timer A0 mode register	TA0MR	103
0397₁₆	Timer A1 mode register	TA1MR	133
0398₁₆	Timer A2 mode register	TA2MR	133
0399₁₆	Timer A3 mode register	TA3MR	103
039A₁₆	Timer A4 mode register	TA4MR	133
039B₁₆	Timer B0 mode register	TB0MR	117
039C₁₆	Timer B1 mode register	TB1MR	117
039D₁₆	Timer B2 mode register	TB2MR	133
039E₁₆	Timer B2 special mode register	TB2SC	131
039F₁₆			
03A0₁₆	UART0 transmit/receive mode register	U0MR	175
03A1₁₆	UART0 bit rate generator	U0BRG	174
03A2₁₆ 03A3₁₆	UART0 transmit buffer register	U0TB	174
03A4₁₆	UART0 transmit/receive control register 0	U0C0	176
03A5₁₆	UART0 transmit/receive control register 1	U0C1	177
03A6₁₆ 03A7₁₆	UART0 receive buffer register	U0RB	174
03A8₁₆	UART1 transmit/receive mode register	U1MR	175
03A9₁₆	UART1 bit rate generator	U1BRG	174
03AA₁₆ 03AB₁₆	UART1 transmit buffer register	U1TB	174
03AC₁₆	UART1 transmit/receive control register 0	U1C0	176
03AD₁₆	UART1 transmit/receive control register 1	U1C1	177
03AE₁₆ 03AF₁₆	UART1 receive buffer register	U1RB	174
03B0₁₆	UART transmit/receive control register 2	UCON	176
03B1₁₆			
03B2₁₆			
03B3₁₆			
03B4₁₆ 03B5₁₆	CRC snoop address register	CRCSAR	314
03B6₁₆	CRC mode register	CRCMR	314
03B7₁₆			
03B8₁₆	DMA0 request cause select register	DM0SL	93
03B9₁₆			
03BA₁₆	DMA1 request cause select register	DM1SL	94
03BB₁₆			
03BC₁₆ 03BD₁₆	CRC data register	CRCD	314
03BE₁₆	CRC input register	CRCIN	314
03BF₁₆			

Address	Register	Symbol	Page
03C0₁₆ 03C1₁₆	A/D register 0	AD0	226
03C2₁₆ 03C3₁₆	A/D register 1	AD1	226
03C4₁₆ 03C5₁₆	A/D register 2	AD2	226
03C6₁₆ 03C7₁₆	A/D register 3	AD3	226
03C8₁₆ 03C9₁₆	A/D register 4	AD4	226
03CA₁₆ 03CB₁₆	A/D register 5	AD5	226
03CC₁₆ 03CD₁₆	A/D register 6	AD6	226
03CE₁₆ 03CF₁₆	A/D register 7	AD7	226
03D0₁₆			
03D1₁₆			
03D2₁₆	A/D trigger control register	ADTRGCON	225
03D3₁₆	A/D convert status register 0	ADSTAT0	226
03D4₁₆	A/D control register 2	ADCON2	224
03D5₁₆			
03D6₁₆	A/D control register 0	ADCON0	224
03D7₁₆	A/D control register 1	ADCON1	224
03D8₁₆			
03D9₁₆			
03DA₁₆			
03DB₁₆			
03DC₁₆			
03DD₁₆			
03DE₁₆			
03DF₁₆			
03E0₁₆	Port P0 register	P0	324
03E1₁₆	Port P1 register	P1	324
03E2₁₆	Port P0 direction register	PD0	323
03E3₁₆	Port P1 direction register	PD1	323
03E4₁₆	Port P2 register	P2	324
03E5₁₆	Port P3 register	P3	324
03E6₁₆	Port P2 direction register	PD2	323
03E7₁₆	Port P3 direction register	PD3	323
03E8₁₆			
03E9₁₆			
03EA₁₆			
03EB₁₆			
03EC₁₆	Port P6 register	P6	324
03ED₁₆	Port P7 register	P7	324
03EE₁₆	Port P6 direction register	PD6	323
03EF₁₆	Port P7 direction register	PD7	323
03F0₁₆	Port P8 register	P8	324
03F1₁₆	Port P9 register	P9	324
03F2₁₆	Port P8 direction register	PD8	323
03F3₁₆	Port P9 direction register	PD9	323
03F4₁₆	Port P10 register	P10	324
03F5₁₆			
03F6₁₆	Port P10 direction register	PD10	323
03F7₁₆			
03F8₁₆			
03F9₁₆			
03FA₁₆			
03FB₁₆			
03FC₁₆	Pull-up control register 0	PUR0	325
03FD₁₆	Pull-up control register 1	PUR1	325
03FE₁₆	Pull-up control register 2	PUR2	325
03FF₁₆	Port control register	PCR	326

Note : The blank areas are reserved and cannot be accessed by users.

Table 1.5 Product List (3) -V Version **As of March, 2007**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30290FAVHP	96 K + 4 K	8 K	PLQP0080KB-A (80P6Q-A)	Flash Memory	U3, U5, U7, U9
M30290FCVHP	128 K + 4 K	12 K			
M30291FAVHP	96 K + 4 K	8 K	PLQP0064KB-A (64P6Q-A)		
M30291FCVHP	128 K + 4 K	12 K			
M30290M8V-XXXHP	64 K	4 K	PLQP0080KB-A (80P6Q-A)	Mask ROM	U0
M30290MAV-XXXHP	96 K	8 K			
M30290MCV-XXXHP	128 K	12 K			
M30291M8V-XXXHP	64 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30291MAV-XXXHP	96 K	8 K			
M30291MCV-XXXHP	128 K	12 K			

Table 9.6 PC Value Saved in Stack Area When Address Match Interrupt Request Is Acknowledged

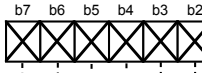
Instruction at the address indicated by the RMADi register	Value of the PC that is saved to the stack area
• 2-byte op-code instruction • 1-byte op-code instructions which are followed: ADD.B:S #IMM8,dest SUB.B:S #IMM8,dest AND.B:S #IMM8,dest OR.B:S #IMM8,dest MOV.B:S #IMM8,dest STZ.B #IMM8,dest STNZ.B #IMM8,dest STZX.B #IMM81,#IMM82,dest CMP.B:S #IMM8,dest PUSHM src POPM dest JMPS #IMM8 JSRS #IMM8 MOV.B:S #IMM,dest (However, dest=A0 or A1)	The address indicated by the RMADi register +2
Instructions other than the above	The address indicated by the RMADi register +1

Value of the PC that is saved to the stack area : Refer to “Saving Registers”.
Op-code is an abbreviation of Operation Code. It is a portion of instruction code.
Refer to Chapter 4 Instruction Code/Number of Cycles in M16C/60, M16C/20 Series Software Manual. Op-code is shown as a bold-framed figure directly below the Syntax.

Table 9.7 Relationship Between Address Match Interrupt Sources and Associated Registers

Address match interrupt sources	Address match interrupt enable bit	Address match interrupt register
Address match interrupt 0	AIER0	RMAD0
Address match interrupt 1	AIER1	RMAD1

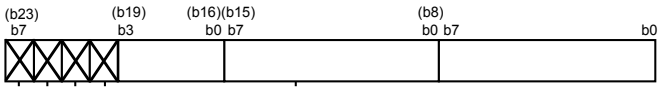
Address Match Interrupt Enable Register



Symbol: AIER
Address: 0009₁₆
After Reset: XXXXXX00₂

Bit Symbol	Bit Name	Function	RW
AIER0	Address match interrupt 0 enable bit	0 : Interrupt disabled 1 : Interrupt enabled	RW
AIER1	Address match interrupt 1 enable bit	0 : Interrupt disabled 1 : Interrupt enabled	RW
— (b7-b2)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined		—

Address Match Interrupt Register i (i = 0 to 1)

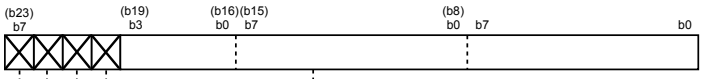


Symbol: RMAD0, RMAD1
Address: 0012₁₆ to 0010₁₆, 0016₁₆ to 0014₁₆
After Reset: X0000₁₆, X0000₁₆

Function	Setting Range	RW
Address setting register for address match interrupt	0000₁₆ to FFFFF₁₆	RW
Nothing is assigned. If necessary, set to 0. When read, the content is undefined		—

Figure 9.14 AIER Register, RMAD0 and RMAD1 Registers

DMAi Source Pointer (i = 0, 1) (1)

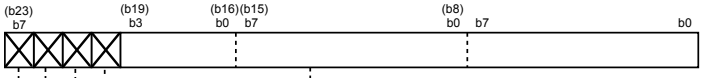


Symbol	Address	After Reset
SAR0	0022$_{16}$ to 0020$_{16}$	Undefined
SAR1	0032$_{16}$ to 0030$_{16}$	Undefined

Function	Setting Range	RW
Set the source address of transfer	00000$_{16}$ to FFFFF$_{16}$	RW
Nothing is assigned. If necessary, set 0. When read, the contents are 0		—

NOTE:
1. If the DSD bit in the DMiCON register is 0 (fixed), this register can only be written to when the DMAE bit in the DMiCON register is set to 0 (DMA disabled).
If the DSD bit is set to 1 (forward direction), this register can be written to at any time.
If the DSD bit is set to 1 and the DMAE bit is set to 1 (DMA enabled), the DMAi forward address pointer can be read from this register. Otherwise, the value written to it can be read.

DMAi Destination Pointer (i = 0, 1)(1)

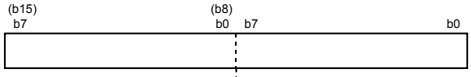


Symbol	Address	After Reset
DAR0	0026$_{16}$ to 0024$_{16}$	Undefined
DAR1	0036$_{16}$ to 0034$_{16}$	Undefined

Function	Setting Range	RW
Set the destination address of transfer	00000$_{16}$ to FFFFF$_{16}$	RW
Nothing is assigned. If necessary, set 0. When read, the contents are 0		—

NOTE:
1. If the DAD bit in the DMiCON register is 0 (fixed), this register can only be written to when the DMAE bit in the DMiCON register is set to 0 (DMA disabled).
If the DAD bit is set to 1 (forward direction), this register can be written to at any time.
If the DAD bit is set to 1 and the DMAE bit is set to 1 (DMA enabled), the DMAi forward address pointer can be read from this register. Otherwise, the value written to it can be read.

DMAi Transfer Counter (i = 0, 1)



Symbol	Address	After Reset
TCR0	0029$_{16}$, 0028$_{16}$	Undefined
TCR1	0039$_{16}$, 0038$_{16}$	Undefined

Function	Setting Range	RW
Set the transfer count minus 1. The written value is stored in the DMAi transfer counter reload register, and when the DMAE bit in the DMiCON register is set to 1 (DMA enabled) or the DMAi transfer counter underflows when the DMASL bit in the DMiCON register is 1 (repeat transfer), the value of the DMAi transfer counter reload register is transferred to the DMAi transfer counter. When read, the DMAi transfer counter is read	0000$_{16}$ to FFFF$_{16}$	RW

Figure 11.4 SAR0, SAR1, DAR0, DAR1, TCR0, and TCR1 Registers

Timer B2 Special Mode Register (1)

b7	b6	b5	b4	b3	b2	b1	b0
X	0	0					

Symbol	Address	After Reset
TB2SC	039E16	X0000000₂

Bit Symbol	Bit Name	Function	RW
PWCON	Timer B2 reload timing switch bit (2)	0: Timer B2 underflow 1: Timer A output at odd-numbered	RW
IVPCR1	Three-phase output port $\overline{SD}$ control bit 1 (3, 4, 7)	0: Three-phase output forcible cutoff by $\overline{SD}$ pin input (high impedance) disabled 1: Three-phase output forcible cutoff by $\overline{SD}$ pin input (high impedance) enabled	RW
TB0EN	Timer B0 operation mode select bit	0: Other than A/D trigger mode 1: A/D trigger mode (5)	RW
TB1EN	Timer B1 operation mode select bit	0: Other than A/D trigger mode 1: A/D trigger mode (5)	RW
TB2SEL	Trigger select bit (6)	0: TB2 interrupt 1: Underflow of TB2 interrupt generation frequency setting counter [ICTB2]	RW
$\overline{\text{(b6-b5)}}$	Reserved bits	Set to 0	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. Write to this register after setting the PRC1 bit in the PRCR register to 1 (write enabled).
2. If the INV11 bit is 0 (three-phase mode 0) or the INV06 bit is 1 (triangular wave modulation mode), set this bit to 0 (timer B2 underflow).
3. When setting the IVPCR1 bit to 1 (three-phase output forcible cutoff by $\overline{SD}$ pin input enabled), Set the PD8$_5$ bit to 0 (= input mode).
4. Related pins are U(P8$_0$), $\overline{U}$(P8$_1$), V(P7$_2$), $\overline{V}$(P7$_3$), W(P7$_4$), $\overline{W}$(P7$_5$). When a high-level ("H") signal is applied to the $\overline{SD}$ pin and set the IVPCR1 bit to 0 after forcible cutoff, pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ are exit from the high-impedance state. If a low-level ("L") signal is applied to the $\overline{SD}$ pin, three-phase motor control timer output will be disabled (INV03=0). At this time, when the IVPCR1 bit is 0, pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ become programmable I/O ports. When the IVPCR1 bit is set to 1, pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ are placed in a high-impedance state regardless of which function of those pins is used.
5. When this bit is used in delayed trigger mode 0, set bits TB0EN and TB1EN to 1 (A/D trigger mode).
6. When setting the TB2SEL bit to 1 (underflow of TB2 interrupt generation frequency setting counter[ICTB2]), set the INV02 bit to 1 (three-phase motor control timer function).
7. Refer to "**19.6 Digital Debounce Function**" for the $\overline{SD}$ input.

The effect of $\overline{SD}$ pin input is below.
1.Case of INV03 = 1(Three-phase motor control timer output enabled)

IVPCR1 bit	$\overline{SD}$ pin inputs(3)	Status of U/V/W pins	Remarks
1 (Three-phase output forcrible cutoff enable)	H	Three-phase PWM output	
	L(1)	High impedance(4)	Three-phase output forcrible cutoff
0 (Three-phase output forcrible cutoff disable)	H	Three-phase PWM output	
	L(1)	Input/output port(2)	

NOTES:
1. When "L" is applied to the $\overline{SD}$ pin, INV03 bit is changed to 0 at the same time.
2. The value of the port register and the port direction register becomes effective.
3. When $\overline{SD}$ function is not used, set to 0 (Input) in PD8$_5$ and pullup to "H" in $\overline{SD}$ pin from outside.
4. To leave the high-impedance state and restart the three-phase PWM signal output after the three-phase PWM signal output forced cutoff, set the IVPCR1 bit to 0 after the $\overline{SD}$ pin input level becomes high ("H").

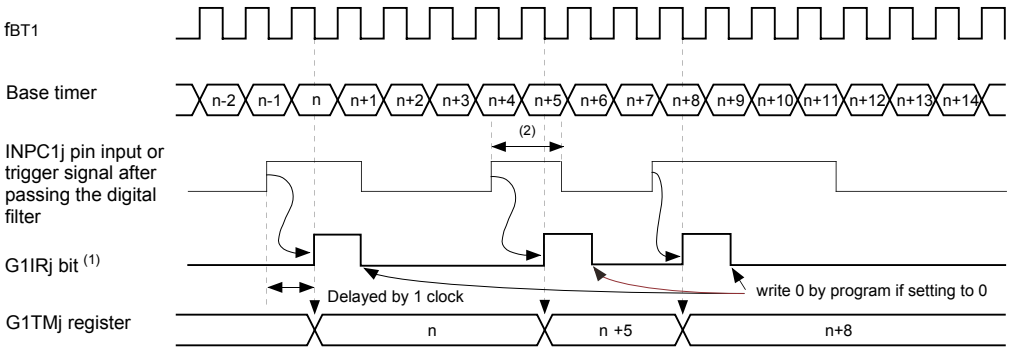
2.Case of INV03 = 0(Three-phase motor control timer output disabled)

IVPCR1 bit	$\overline{SD}$ pin inputs	Status of U/V/W pins	Remarks
1 (Three-phase output forcrible cutoff enable)	H	Peripheral input/output or input/output port	
	L	High impedance	Three-phase output forcrible cutoff(1)
0 (Three-phase output forcrible cutoff disable)	H	Peripheral input/output or input/output port	
	L	Peripheral input/output or input/output port	

NOTE:
1. The three-phase output forcrible cutoff function becomes effective if the INPCR1 bit is set to 1 (three-phase output forcrible cutoff function enable) even when the INV03 bit is 0 (three-phase motor control timer output disalbe)

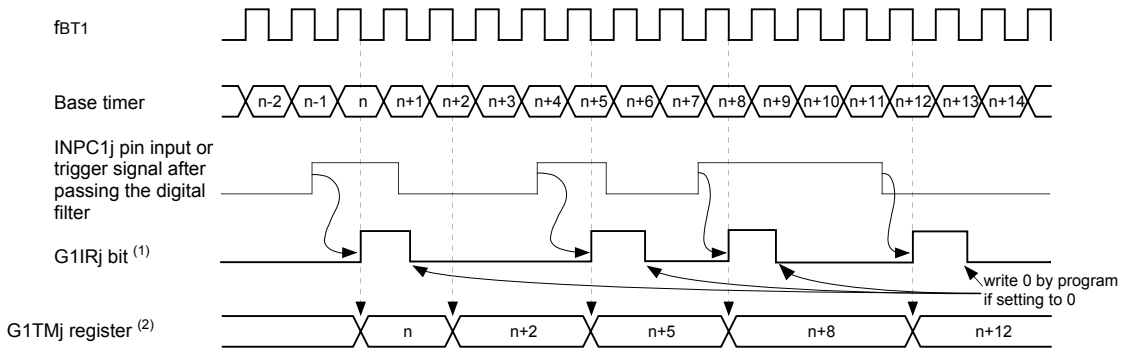
Figure 12.30 TB2SC Register

(a) When selecting the rising edge as a timer measurement trigger
(Bits CTS1 and CTS0 in the G1TMCRj register (j=0 to 7)=01$_2$)



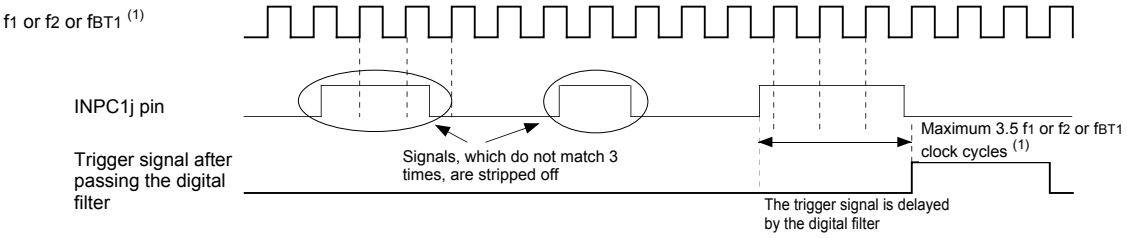
NOTES :
1. Bits in the G1IR register.
2. Input pulse applied to the INPC1j pin requires 1.5 fBT1 clock cycles or more.

(b) When selecting both edges as a timer measurement trigger
(Bits CTS1 and CTS0 = 11$_2$)



NOTES :
1. Bits in the G1IR register.
2. No interrupt is generated if the MCU receives a trigger signal when the G1IRj bit is set to 1. However, the value of the G1TMj register is updated.

(c) Trigger signal when using digital filter
(Bits DF1 to DF0 in the G1TMCRj register =10$_2$ or 11$_2$)



NOTE:
1. fBT1 when bits DF1 to DF0 are set to 10$_2$, and f1 or f2 when set to 11$_2$.

Figure 13.20 Time Measurement Function (2)

14.1.1.4 Continuous receive mode

When the UiRRM bit (i=0 to 2) is set to 1 (continuous receive mode), the TI bit in the UiC1 register is set to 0 (data present in the UiTB register) by reading the UiRB register. In this case, i.e., UiRRM bit is set to 1, do not write dummy data to the UiTB register in a program. The U0RRM and U1RRM bits are the bit 2 and bit 3 in the UCON register, respectively, and the U2RRM bit is the bit 5 in the U2C1 register.

14.1.1.5 Serial data logic switch function (UART2)

When the U2LCH bit in the U2C1 register is set to 1 (reverse), the data written to the U2TB register has its logic reversed before being transmitted. Similarly, the received data has its logic reversed when read from the U2RB register. **Figure 14.13** shows serial data logic.

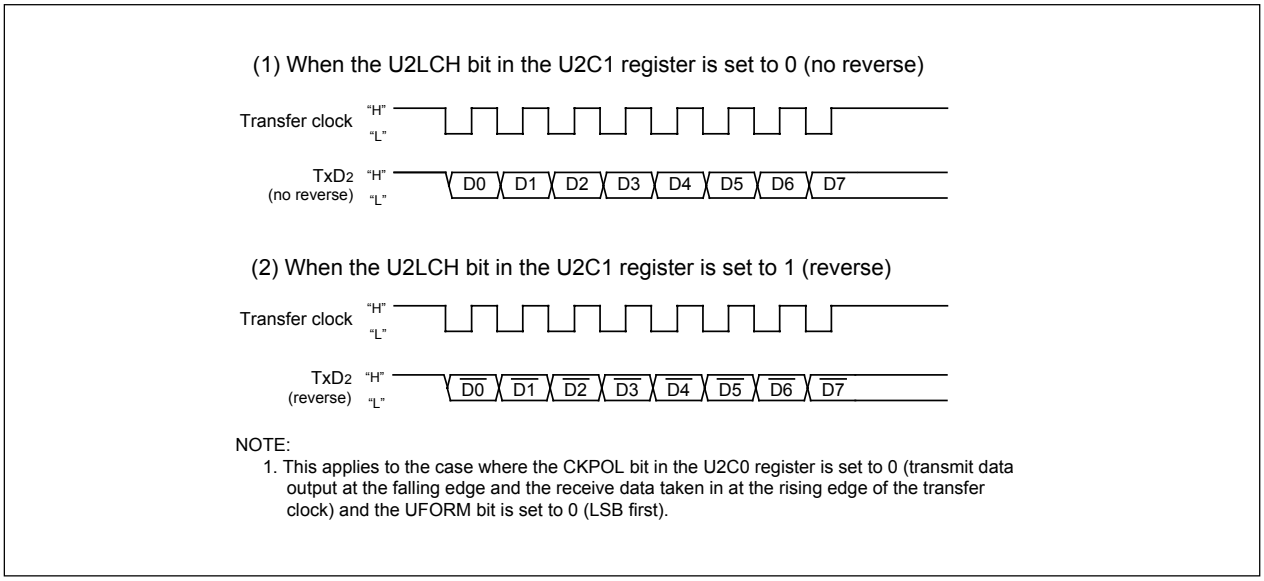


Figure 14.13 Serial data logic switch timing

14.1.1.6 Transfer clock output from multiple pins function (UART1)

The CLKMD1 to CLKMD0 bits in the UCON register can choose one from two transfer clock output pins. (See **Figure 14.14**) This function is valid when the internal clock is selected for UART1.

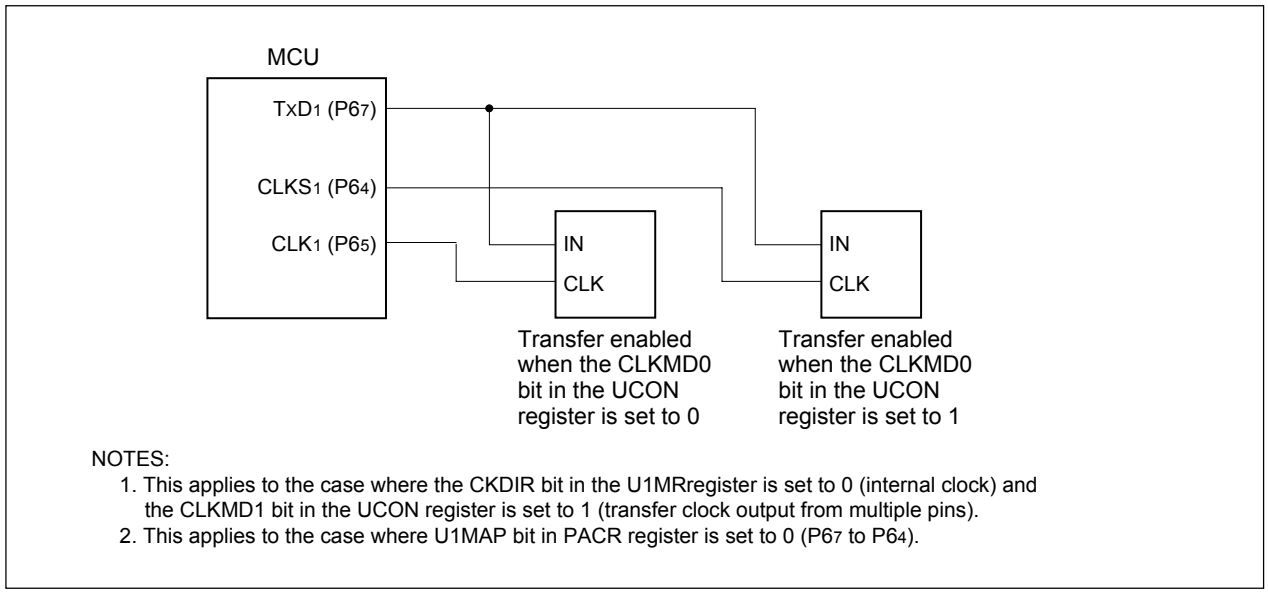


Figure 14.14 Transfer Clock Output From Multiple Pins

16.5.7 Bit 6: Communication Mode Select Bit (Transfer Direction Select Bit: TRX)

This TRX bit decides a transfer direction for data communication. When the TRX bit is set to 0, receive mode is entered and data is received from a transmit device. When the TRX bit is set to 1, transmit mode is entered, and address data and control data are output to the SDAMM, synchronized with a clock generated in the SCLMM.

The TRX bit is set to 1 automatically in the following condition:

- In slave mode, when the ALS in the S1D0 register to 0(addressing format), the AAS flag is set to 1 (address match) after the address data is received, and the received R/$\overline{W}$ bit is set to 1

The TRX bit is set to 0 in one of the following conditions:

- When an arbitration lost is detected
- When a STOP condition is detected
- When a START condition is detected
- When a START condition is disabled by the START condition duplicate protect function (1)
- When the MST bit in the S10 register is set to 0(slave mode) and a start condition is detected
- When the MST bit is set to 0 and the ACK non-return is detected
- When the ES0 bit is set to 0(I2C bus interface disabled)
- When the IHR bit in the S1D0 register is set to 1(reset)

16.5.8 Bit 7: Communication mode select bit (master/slave select bit: MST)

The MST bit selects either master mode or slave mode for data communication. When the MST bit is set to 0, slave mode is entered and the START/STOP condition generated by a master device are received. The data communication is synchronized with the clock generted by the master. When the MST bit is set to 1, master mode is entered and the START/STOP condition is generated.

Additionally, clocks required for the data communication are generated on the SCLMM.

The MST bit is set to 0 in one of the following conditions.

- After 1-byte data of a master whose arbtration is lost if arbitration lost is detected
- When a STOP condition is detected
- When a START condition is detected
- When a start condition is disabled by the START condition duplicate protect function (1)
- When the IHR bit in the S1D0 register is set to 1(reset)
- When the ES0 bit is set to 0(I2C bus interface disabled)

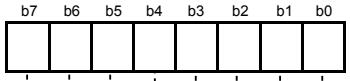
NOTE:

1. START condition duplicate protect function:
   When the START condition is generated, after confirming that the BB flag in the S1D0 register is set to 0 (bus free), all the MST, TRX and BB flags are set to 1 at the same time. However, if the BB flag is set to 1 immediately after the BB flag setting is confirmed because a START condition is generated by other master device, bits MST and TRX cannot be written. The duplicate protect function is valid from the rising edge of the BB flag until slave address is received. Refer to **16.9 START Condition Generation Method** for details.

17.1.3.7 C0CONR Register

Figure 17.12 shows the C0CONR register.

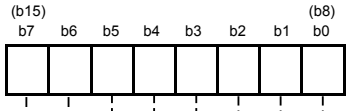
CAN0 Configuration Register(2)



Symbol: C0CONR — Address: 021A16 — After reset: Undefined

Bit symbol	Bit name	Function	RW
BRP	Prescaler division ratio select bits	b3 b2 b1 b0 0 0 0 0: Divide-by-1 of fCAN 0 0 0 1: Divide-by-2 of fCAN 0 0 1 0: Divide-by-3 of fCAN ⋮ 1 1 1 0: Divide-by-15 of fCAN 1 1 1 1: Divide-by-16 of fCAN (1)	RW
SAM	Sampling control bit	0: One time sampling 1: Three times sampling	RW
PTS	Propagation time segment control bits	b7 b6 b5 0 0 0: 1Tq 0 0 1: 2Tq 0 1 0: 2Tq ⋮ 1 1 0: 7Tq 1 1 1: 8Tq	RW

NOTES:
1. fCAN serves for the CAN clock. The period is decided by configuration of the CCLKi bits (i = 0 to 2) in the CCLKR register.
2. Set the C0CONR register only when the CAN module is in CAN reset / initialization mode.



Symbol: C0CONR — Address: 021B16 — After Reset: Undefined

Bit symbol	Bit name	Function	RW
PBS1	Phase buffer segment 1 control bits	b2 b1b0 0 0 0: Do not set 0 0 1: 2Tq 0 1 0: 3Tq ⋮ 1 1 0: 7Tq 1 1 1: 8Tq	RW
PBS2	Phase buffer segment 2 control bits	b5 b4 b3 0 0 0: Do not set 0 0 1: 2Tq 0 1 0: 3Tq ⋮ 1 1 0: 7Tq 1 1 1: 8Tq	RW
SJW	Resynchronization jump width control bits	b7 b6 0 0: 1Tq 0 1: 2Tq 1 0: 3Tq 1 1: 4Tq	RW

Figure 17.12 C0CONR Register

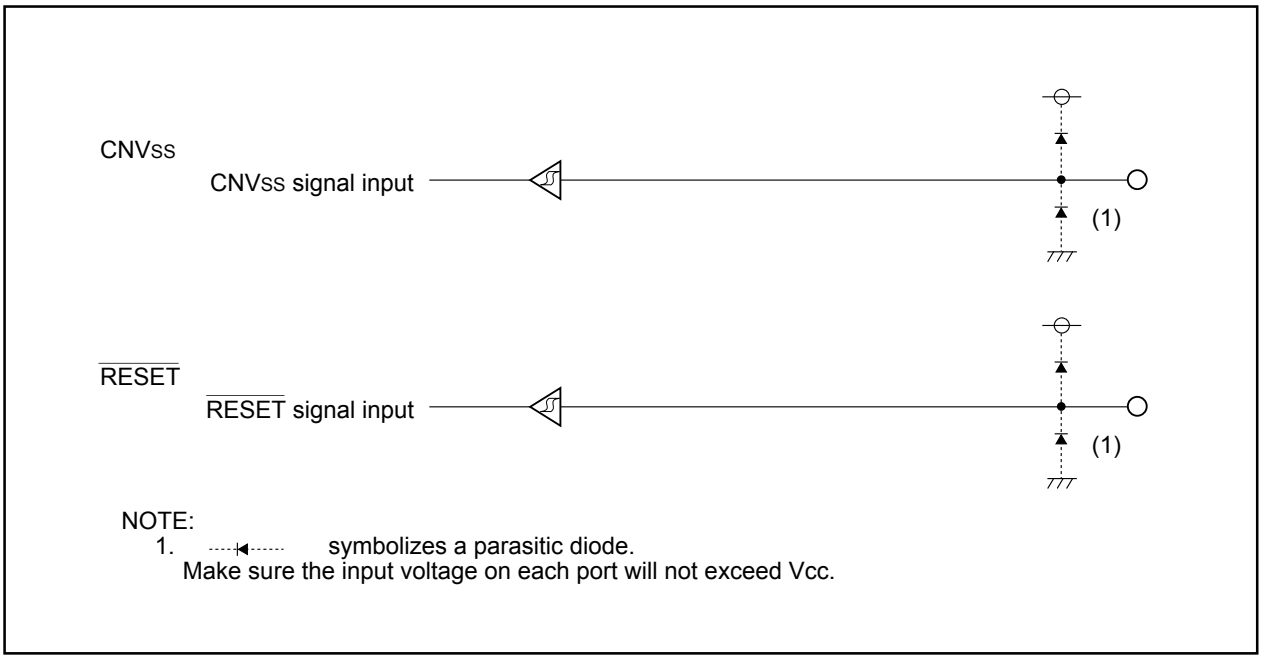


Figure 19.5 I/O Pins

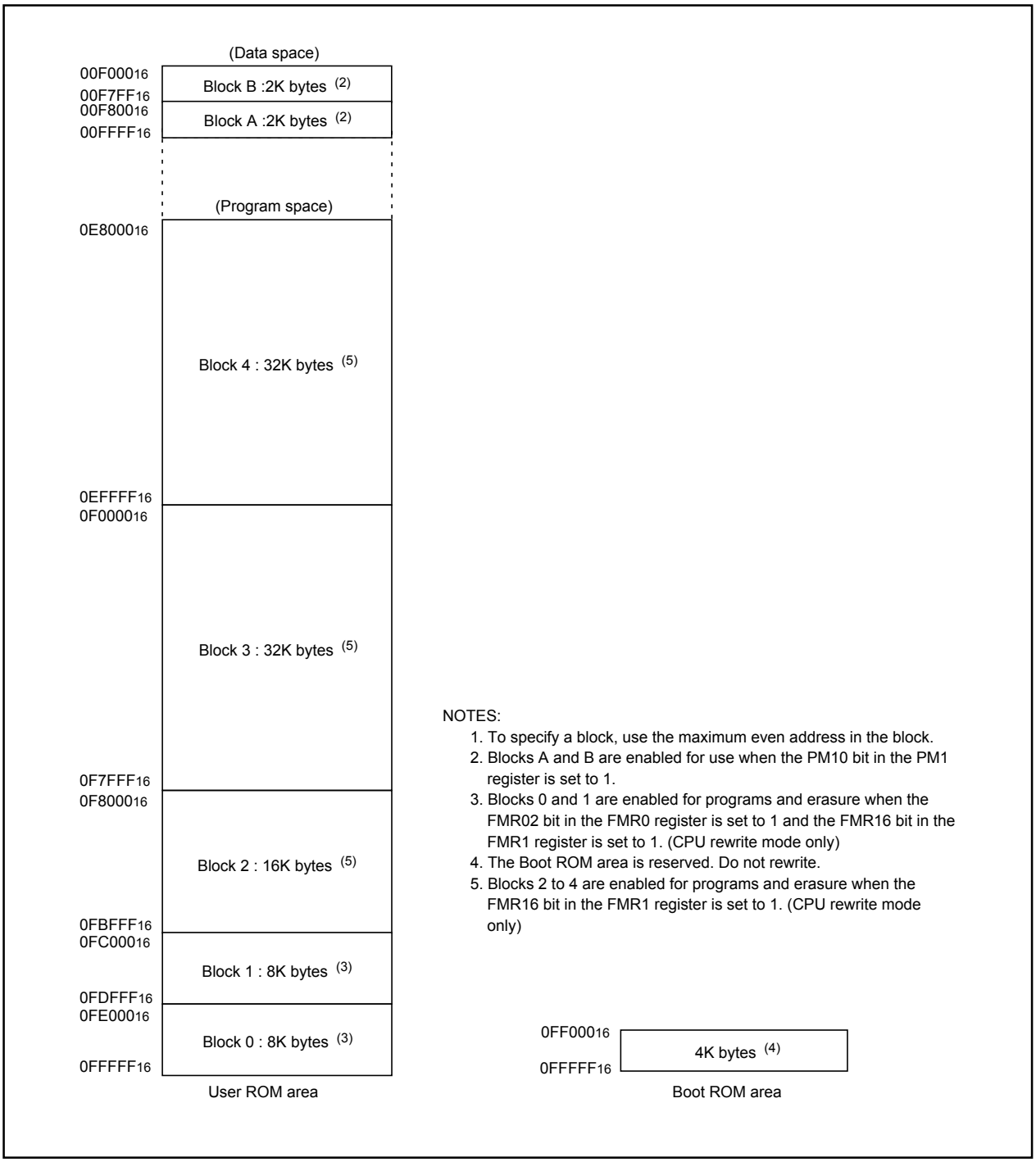


Figure 20.2 Flash Memory Block Diagram (ROM capacity 96 Kbytes)

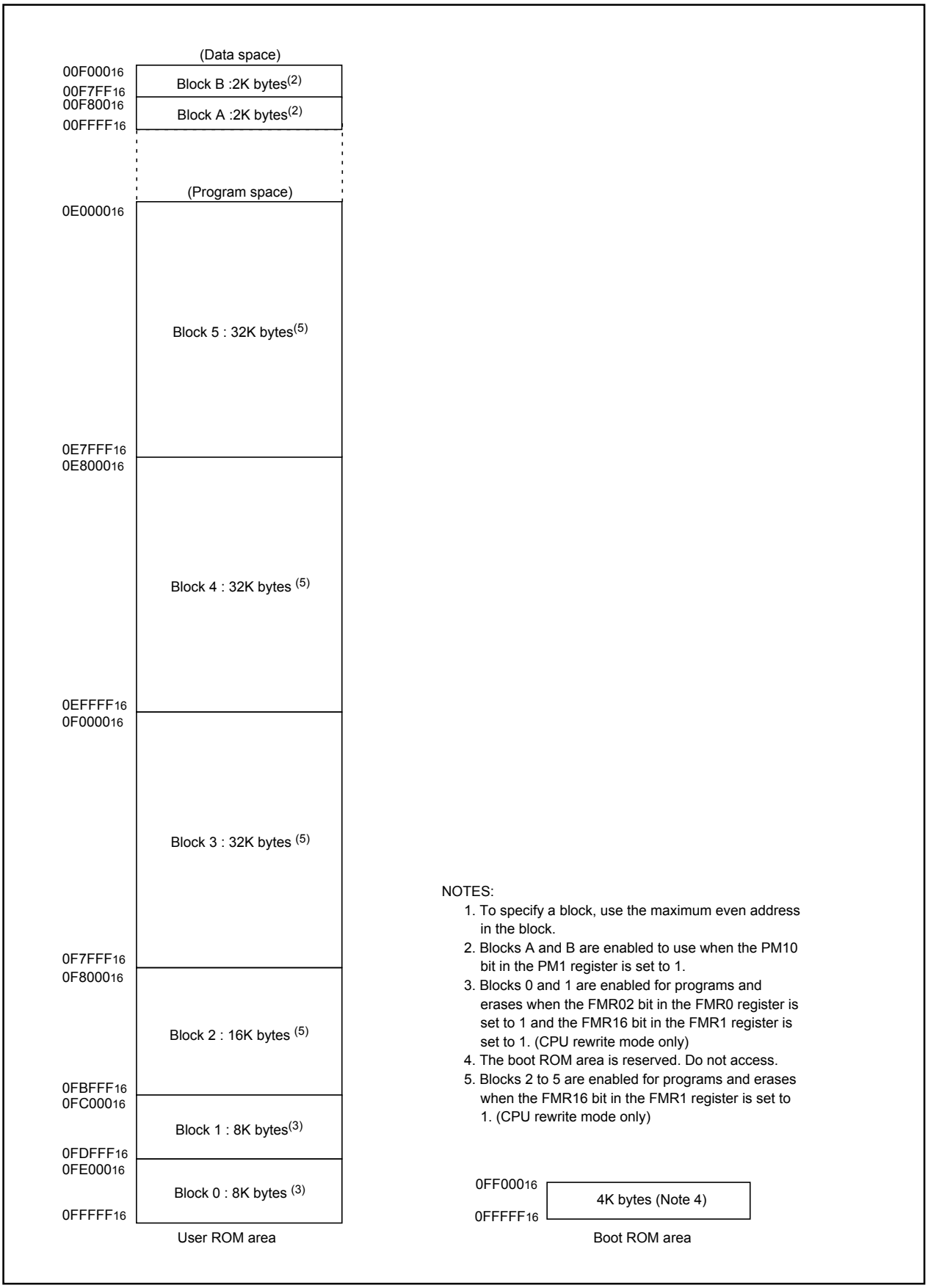


Figure 20.3 Flash Memory Block Diagram (ROM capacity 128 Kbytes)

Table 20.8 Pin Descriptions (Flash Memory Standard Serial I/O Mode)

Pin	Name		I/O	Descriptio n
VCC,VSS	Power input			Apply the voltage guaranteed for Program and Erase to Vcc pin and 0 V to Vss pin.
CNVSS	CNVSS		I	Connect to Vcc pin.
$\overline{\text{RESET}}$	Reset input		I	Reset input pin. While $\overline{\text{RESET}}$ pin is “L”, wait for td(ROC).
XIN	Clock input		I	Connect a ceramic resonator or crystal oscillator between XIN and XOUT pins. To input an externally generated clock, input it to XIN pin and open XOUT pin.
XOUT	Clock output		O	
AVCC, AVSS	Analog power supply input			Connect AVss to Vss and AVcc to Vcc, respectively.
VREF	Reference voltage input		I	Enter the reference voltage for AD conversion.
P00 to P07	Input port P0		I	Input “H” or “L” signal or leave open.
P10 to P15, P17	Input port P1		I	Input “H” or “L” signal or leave open.
P16	Input port P1		I	Connect this pin to Vcc while $\overline{\text{RESET}}$ pin is “L”. (2)
P20 to P27	Input port P2		I	Input "H" or “L” level signal or leave open.
P30 to P37	Input port P3		I	Input "H" or “L” level signal or leave open.
P60 to P63	Input port P6		I	Input "H" or “L” level signal or leave open.
P64	BUSY output		O	Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 2: Monitor signal output pin for boot program operation check
P65	SCLK input		I	Standard serial I/O mode 1: Serial clock input pin Standard serial I/O mode 2: Input “L”.
P66	RxD input		I	Serial data input pin
P67	TxD output		O	Serial data output pin (1)
P70 to P77	Input port P7		I	Input “H” or “L” signal or leave open.
P80 to P84, P87	Input port P8		I	Input “H” or “L” signal or leave open.
P85	$\overline{\text{RP}}$ input		I	Connect this pin to Vss while $\overline{\text{RESET}}$ pin is “L”. (2)
P86	$\overline{\text{CE}}$ input		I	Connect this pin to Vcc while $\overline{\text{RESET}}$ pin is “L”. (2)
P90 to P92, P95 to P97	Input port P9		I	Input “H” or “L” signal or leave open.
P93	Input port P93	Normal-ver.	I/O	“H” signal is output for specific time. Input “H” signal or leave open.
		T-ver./V-ver.	I	Input “H” or “L” signal or leave open.
P100 to P107	Input port P10		I	Input “H” or “L” signal or leave open.

NOTES:

1. When using standard serial I/O mode 1, to input “H” to the TxD pin is necessary while the $\overline{\text{RESET}}$ pin is held “L”. Therefore, connect this pin to VCC via a resistor. Adjust the pull-up resistor value on a system not to affect a data transfer after reset, because this pin changes to a data-output pin
2. Set the following, either or both.
   -Connect the $\overline{\text{CE}}$ pin to VCC.
   -Connect the $\overline{\text{RP}}$ pin to VSS and P16 pin to VCC.

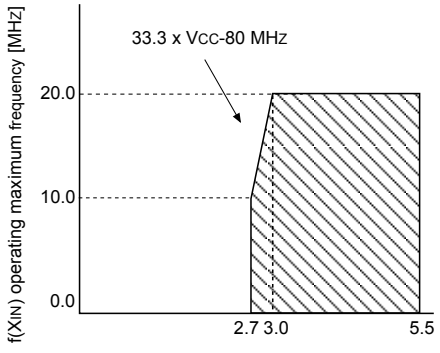
Table 21.2 Recommended Operating Conditions (Note 1)

Symbol	Parameter			Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply Voltage			2.7		5.5	V
AVcc	Analog Supply Voltage				Vcc		V
Vss	Supply Voltage				0		V
AVss	Analog Supply Voltage				0		V
V_{IH}	Input High ("H") Voltage	P0$_0$ to P0$_7$, P1$_0$ to P1$_7$, P2$_0$ to P2$_7$, P3$_0$ to P3$_7$, P6$_0$ to P6$_7$, P7$_0$ to P7$_7$, P8$_0$ to P8$_7$, P9$_0$ to P9$_3$, P9$_5$ to P9$_7$, P10$_0$ to P10$_7$		0.7Vcc		Vcc	V
		XIN, $\overline{\text{RESET}}$, CNVSS		0.8Vcc		Vcc	V
		SDAMM, SCLMM	When I^2C bus input level is selected	0.7Vcc		Vcc	V
			When SMBUS input level is selected	1.4		Vcc	V
V_{IL}	Input Low ("L") Voltage	P0$_0$ to P0$_7$, P1$_0$ to P1$_7$, P2$_0$ to P2$_7$, P3$_0$ to P3$_7$, P6$_0$ to P6$_7$, P7$_0$ to P7$_7$, P8$_0$ to P8$_7$, P9$_0$ to P9$_3$, P9$_5$ to P9$_7$, P10$_0$ to P10$_7$		0		0.3Vcc	V
		XIN, $\overline{\text{RESET}}$, CNVSS		0		0.2Vcc	V
		SDAMM, SCLMM	When I^2C bus input level is selected	0		0.3Vcc	V
			When SMBUS input level is selected	0		0.6	V
$I_{OH(peak)}$	Peak Output High ("H") Current	P0$_0$ to P0$_7$, P1$_0$ to P1$_7$, P2$_0$ to P2$_7$, P3$_0$ to P3$_7$, P6$_0$ to P6$_7$, P7$_0$ to P7$_7$, P8$_0$ to P8$_7$, P9$_0$ to P9$_3$, P9$_5$ to P9$_7$, P10$_0$ to P10$_7$				-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current	P0$_0$ to P0$_7$, P1$_0$ to P1$_7$, P2$_0$ to P2$_7$, P3$_0$ to P3$_7$, P6$_0$ to P6$_7$, P7$_0$ to P7$_7$, P8$_0$ to P8$_7$, P9$_0$ to P9$_3$, P9$_5$ to P9$_7$, P10$_0$ to P10$_7$				-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current	P0$_0$ to P0$_7$, P1$_0$ to P1$_7$, P2$_0$ to P2$_7$, P3$_0$ to P3$_7$, P6$_0$ to P6$_7$, P7$_0$ to P7$_7$, P8$_0$ to P8$_7$, P9$_0$ to P9$_3$, P9$_5$ to P9$_7$, P10$_0$ to P10$_7$				10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current	P0$_0$ to P0$_7$, P1$_0$ to P1$_7$, P2$_0$ to P2$_7$, P3$_0$ to P3$_7$, P6$_0$ to P6$_7$, P7$_0$ to P7$_7$, P8$_0$ to P8$_7$, P9$_0$ to P9$_3$, P9$_5$ to P9$_7$, P10$_0$ to P10$_7$				5.0	mA
f(XIN)	Main Clock Input Oscillation Frequency(4)		Vcc=3.0 to 5.5V	0		20	MHz
			Vcc=2.7 to 3.0V	0		33 X Vcc-80	MHz
f(XCIN)	Sub Clock Oscillation Frequency				32.768	50	kHz
f1(ROC)	On-chip Oscillator Frequency 1			0.5	1	2	MHz
f2(ROC)	On-chip Oscillator Frequency 2			1	2	4	MHz
f3(ROC)	On-chip Oscillator Frequency 3			8	16	26	MHz
f(PLL)	PLL Clock Oscillation Frequency(4)		Vcc=3.0 to 5.5V	10		20	MHz
			Vcc=2.7 to 3.0V	10		33 X Vcc-80	MHz
f(BCLK)	CPU Operation Clock Frequency			0		20	MHz
tsu(PLL)	Wait Time to Stabilize PLL Frequency Synthesizer		Vcc=5.0V			20	ms
			Vcc=3.0V			50	ms

NOTES:

1. Referenced to Vcc = 2.7 to 5.5V at Topr = -20 to 85 ° C / -40 to 85 ° C unless otherwise specified.
2. The mean output current is the mean value within 100ms.
3. The total $I_{OL(peak)}$ for all ports must be 80mA or less. The total $I_{OH(peak)}$ for all ports must be -80mA or less.
4. Relationship among main clock oscillation frequency, PLL clock oscillation frequency and supply voltage.

Main clock input oscillation frequency



PLL clock oscillation frequency

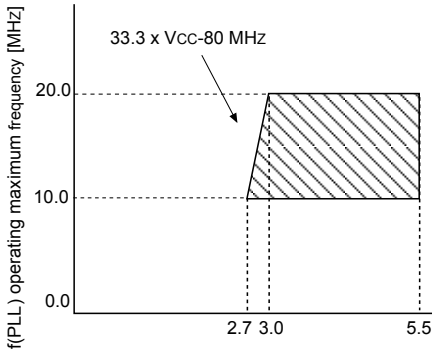


Table 21.4 Flash Memory Version Electrical Characteristics (1) for 100/1000 E/W cycle products

[Program Space and Data Space in U3 and U5: Program Space in U7 and U9]

Symbol	Parameter		Standard			Unit
			Min.	Typ.(2)	Max.	
-	Program and Erase Endurance(3)		100/1000(4, 11)			cycles
-	Word Program Time (Vcc=5.0V, Topr=25° C)			75	600	µs
-	Block Erase Time (Vcc=5.0V, Topr=25° C)	2-Kbyte Block		0.2	9	s
		8-Kbyte Block		0.4	9	s
		16-Kbyte Block		0.7	9	s
		32-Kbyte Block		1.2	9	s
td(SR-ES)	Duration between Suspend Request and Erase Suspend				8	ms
tPS	Wait Time to Stabilize Flash Memory Circuit				15	µs
-	Data Hold Time (5)		20			years

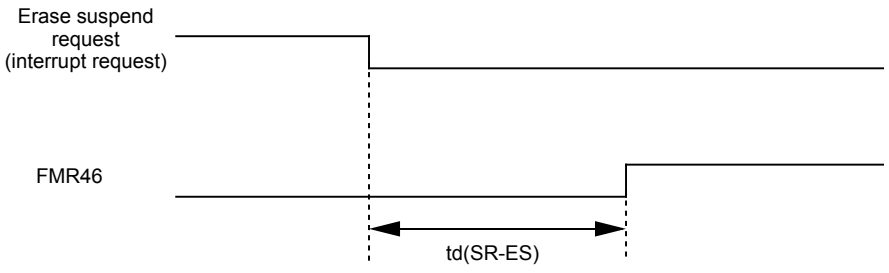
Table 21.5 Flash Memory Version Electrical Characteristics (6) 10000 E/W cycle products (Option)

[Data Space in U7 and U9(7)]

Symbol	Parameter	Standard			Unit
		Min.	Typ.(2)	Max.	
-	Program and Erase Endurance(3, 8, 9)	10000(4, 10)			cycles
-	Word Program Time (Vcc= 5.0 V, Topr = 25° C)		100		µs
-	Block Erase Time (Vcc= 5.0 V, Topr = 25° C) (2-Kbyte block)		0.3		s
td(SR-ES)	Duration between Suspend Request and Erase Suspend			8	ms
tPS	Wait Time to Stabilize Flash Memory Circuit			15	µs
-	Data Hold Time (5)	20			years

NOTES:

1. Referenced to Vcc= 2.7 to 5.5 V at Topr = 0 to 60° C (program space), unless otherwise specified.
2. Vcc= 5.0 V; Topr= 25° C
3. Program and erase endurance is defined as number of program-erase cycles per block.
   If program and erase endurance is *n* cycle (*n* = 100, 1000, 10000), each block can be erased and programmed *n* cycles.
   For example, if a 2-Kbyte block A is erased after programming one-word data to each address 1,024 times, this counts as one program and erase endurance. Data cannot be programmed to the same address more than once without erasing the block. (rewrite prohibited).
4. Number of E/W cycles for which operation is guranteed (1 to minimum value are guaranteed).
5. Topr= 55° C
6. Referenced to Vcc= 2.7 to 5.5 V at Topr= -40 to 85° C(U7) / -20 to 85° C (U9) unless otherwise specifie.
7. **Table 21.5** applies for data space in U7 and U9 when program and erase endurance is more than 1,000 cycles. Otherwise, use **Table 21.4**.
8. To reduce the number of program and erase endurance when working with systems requiring numerous rewrites, write to unused word addresses within the block instead of rewrite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 128 times maximum before erase becomes necessary. Maintaining an equal number of times erasure between block A and block B will also improve efficiency. It is recommended to track the total number of erasure performed per block and to limit the number of erasure.
9. If an erase error is generated during block erase, execute the clear status register command and block erase command at least 3 times until an erase error is not generated.
10. When executing more than 100 times rewrites, set one wait state per block access by setting the FMR17 bit in the FMR1 register 1 to 1 (wait state). When accessing to all other blocks and internal RAM, wait state can be set by the PM17 bit, regardless of the FMR17 bit setting value.
11. The program and erase endurance is 100 cycles for program space and data space in U3 and U5; 1,000 cycles for program space in U7 and U9.
12. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for further details on the E/W failure rate.



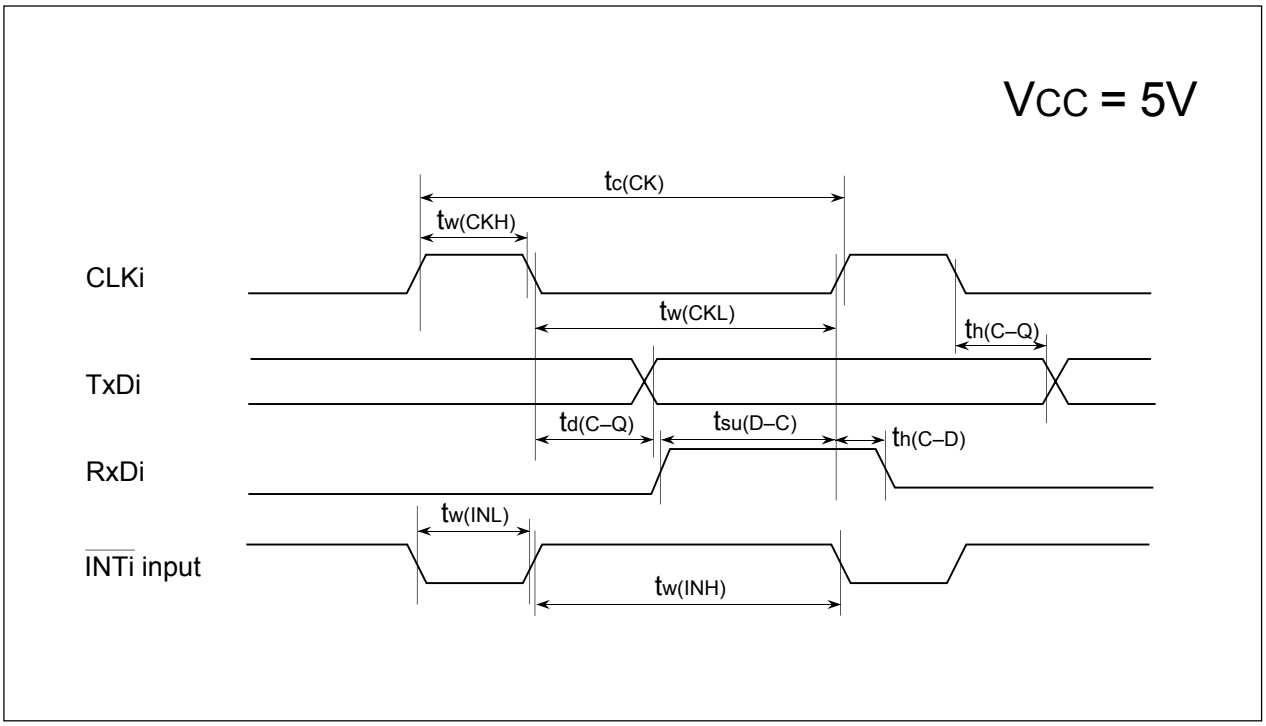


Figure 21.8 Timing Diagram (2)

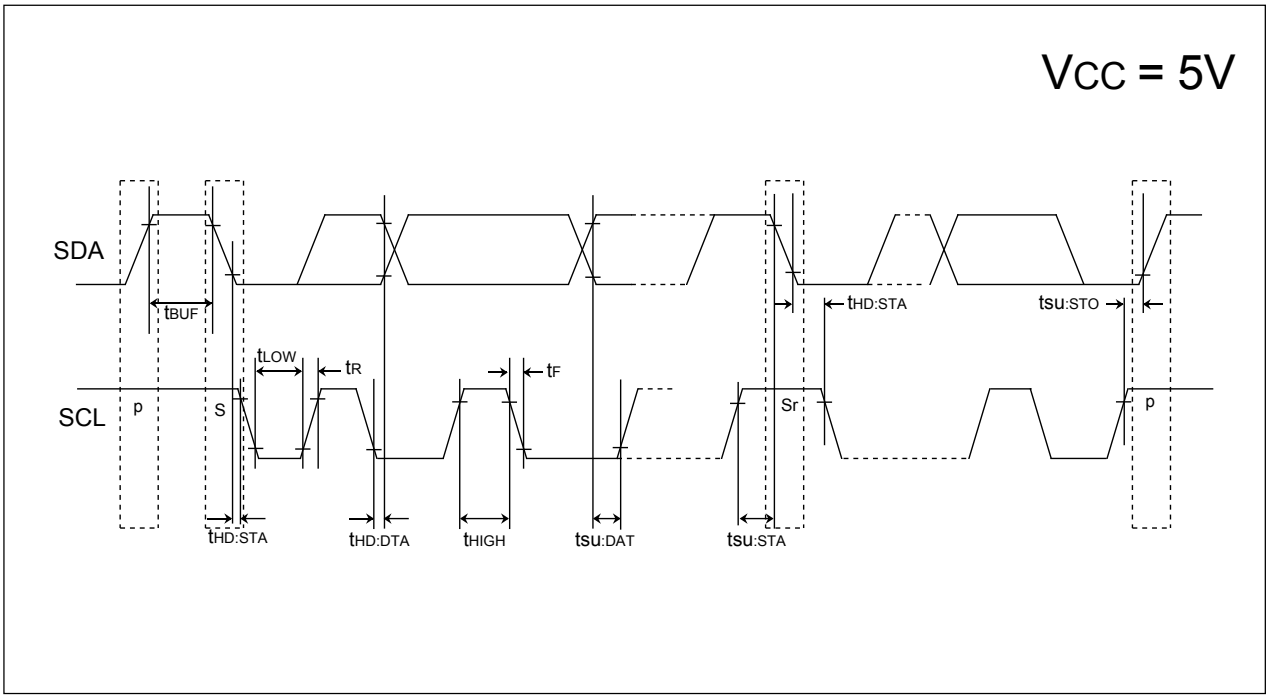


Figure 21.9 Timing Diagram (3)

22.11 CAN Module

22.11.1 Reading C0STR Register

The CAN module on the M16C/29 Group updates the status of the C0STR register in a certain period. When the CPU and the CAN module access to the C0STR register at the same time, the CPU has the access priority; the access from the CAN module is disabled. Consequently, when the updating period of the CAN module matches the access period from the CPU, the status of the CAN module cannot be updated. (See **Figure 22.5**)

Accordingly, be careful about the following points so that the access period from the CPU should not match the updating period of the CAN module:

(1) There should be a wait time of $3f_{CAN}$ or longer (see **Table 22.2**) before the CPU reads the C0STR register. (See **Figure 22.6**)

(2) When the CPU polls the C0STR register, the polling period must be $3f_{CAN}$ or longer. (See **Figure 22.7**)

Table 22.2 CAN Module Status Updating Period

$3f_{CAN}$ period = 3 × X_{IN} (Original oscillation period) × Division value of the CAN clock (CCLK)	
(Example 1) Condition X_{IN} 16 MHz CCLK: Divided by 1	$3f_{CAN}$ period = 3 × 62.5 ns × 1 = 187.5 ns
(Example 2) Condition X_{IN} 16 MHz CCLK: Divided by 2	$3f_{CAN}$ period = 3 × 62.5 ns × 2 = 375 ns
(Example 3) Condition X_{IN} 16 MHz CCLK: Divided by 4	$3f_{CAN}$ period = 3 × 62.5 ns × 4 = 750 ns
(Example 4) Condition X_{IN} 16 MHz CCLK: Divided by 8	$3f_{CAN}$ period = 3 × 62.5 ns × 8 = 1.5 µs
(Example 5) Condition X_{IN} 16 MHz CCLK: Divided by 16	$3f_{CAN}$ period = 3 × 62.5 ns × 16 = 3 µs

22.17 Instruction for a Device Use

When handling a device, extra attention is necessary to prevent it from crashing during the electrostatic discharge period.

Rev.	Date	Description	
		Page	Summary
		66	“9.3 Interrupt Control” is partly revised.
		76	“9.6 $\overline{\text{INT}}$ Interrupt” and “9.7 $\overline{\text{NMI}}$ Interrupt” are partly revised.
		77	“9.8 Key Input Interrupt” and “9.9 CAN0 Wake-up Interrupt” are partly revised.
		80	“10. Watchdog Timer” is partly revised.
		80, 81	“10.1 Count source protective mode” is partly revised.
		81	Note 2 in Figure 10.2 is revised.
		118	Figure 12.3.1 is partly revised.
		121	“Three-phase output buffer register” in Figure 12.3.4 is partly revised.
		133 to 138	Figure 13.1 to 13.6 are partly revised.
		141	“Function enable register” in Figure 13.9 is partly revised.
		150	Table 13.4.1 is partly revised.
		161	“13.6 I/O Port Function Select” is partly revised.
		198	Figure 14.1.4.1 is partly revised.
		209	Figure 14.2.1 is partly revised.
		210	Figure 14.2.2 is partly revised.
		214	“Integral Nonlinearity Error” in Table 15.1 is partly revised.
		253,254	Figure 16.6 and Figure 16.7 are partly revised.
		261	“16.5.4 Bit 3: Arbitration lost detection flag” is partly revised.
		266	“16.6.5 I2C system clock select bits” and Talbe 16.6 are partly revised.
		275	“9)” in “16.13.2 Example of Slave Receive” is revised.
		296	“17.3 Configuration of the CAN Module System Clock” is partly revised.
		306	“18.1 CRC snoop” is partly revised.
		337	Table 20.25 is partly revised.
		368	“21.1 Flash Memory Performance” is partly revised.
		367,368	“21.2 Memory Map” is partly revised.
		372	“21.4 CPU Rewrite Mode” is partly revised.
		373	“21.4.1 EW0 Mode” and “21.4.2 EW1 Mode” are partly revised.
		374	“FMR01 Bit” is partly revised.
		375	“FMR17 Bit” is partly revised.
		383	“21.7.4 Program Command (40_{16})” is partly revised.
		390	Table 21.9.1 and Note 2 are partly revised.
		391,392	Figure 21.9.1 and Figure 21.9.2 are partly revised.
		393,394	Figure 21.9.2.1 and Figure 21.9.2.2 are partly revised.
		396	Table 21.11.1 and Note 1 are partly revised.
		397,398	Figure 21.11.1 and Figure 21.11.2 are partly revised.
		399	Figure 21.11.3 is partly revised.
1.10	10/10/06	All Pages	Package code changed: 80P6Q-A to PLQP0080KB-A, 64P6Q-A to PLQP0064KB-A Words standardized: Low voltage detection, CPU clock, MCU, SDA_2, SCL_2