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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	55
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30291fchp-u5a

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9.3.1 I Flag

The I flag enables or disables the maskable interrupt. Setting the I flag to 1 (= enabled) enables the maskable interrupt. Setting the I flag to 0 (= disabled) disables all maskable interrupts.

9.3.2 IR Bit

The IR bit is set to 1 (= interrupt requested) when an interrupt request is generated. Then, when the interrupt request is accepted and the CPU branches to the corresponding interrupt vector, the IR bit is cleared to 0 (= interrupt not requested).
The IR bit can be cleared to 0 in a program. Note that do not write 1 to this bit.

9.3.3 ILVL2 to ILVL0 Bits and IPL

Interrupt priority levels can be set using bits ILVL2 to ILVL0.
Table 9.3 shows the settings of interrupt priority levels and **Table 9.4** shows the interrupt priority levels enabled by the IPL.

The following are conditions under which an interrupt is accepted:
· I flag = 1
· IR bit = 1
· interrupt priority level > IPL

The I flag, IR bit, bits ILVL2 to ILVL0, and IPL are independent of each other. In no case do they affect one another.

Table 9.3 Settings of Interrupt Priority Levels

ILVL2 to ILVL0 bits	Interrupt priority level	Priority order
000_2	Level 0 (interrupt disabled)	———
001_2	Level 1	Low ↓
010_2	Level 2	
011_2	Level 3	
100_2	Level 4	
101_2	Level 5	
110_2	Level 6	
111_2	Level 7	High

Table 9.4 Interrupt Priority Levels Enabled by IPL

IPL	Enabled interrupt priority levels
000_2	Interrupt levels 1 and above are enabled
001_2	Interrupt levels 2 and above are enabled
010_2	Interrupt levels 3 and above are enabled
011_2	Interrupt levels 4 and above are enabled
100_2	Interrupt levels 5 and above are enabled
101_2	Interrupt levels 6 and above are enabled
110_2	Interrupt levels 7 and above are enabled
111_2	All maskable interrupts are disabled

The operation of saving registers carried out in the interrupt sequence is dependent on whether the SP(1), at the time of acceptance of an interrupt request, is even or odd. If the stack pointer (1) is even, the FLG register and the PC are saved, 16 bits at a time. If odd, they are saved in two steps, 8 bits at a time. **Figure 9.8** shows the operation of the saving registers.

NOTE:
1. When any INT instruction in software numbers 32 to 63 has been executed, this is the SP indicated by the U flag. Otherwise, it is the ISP.

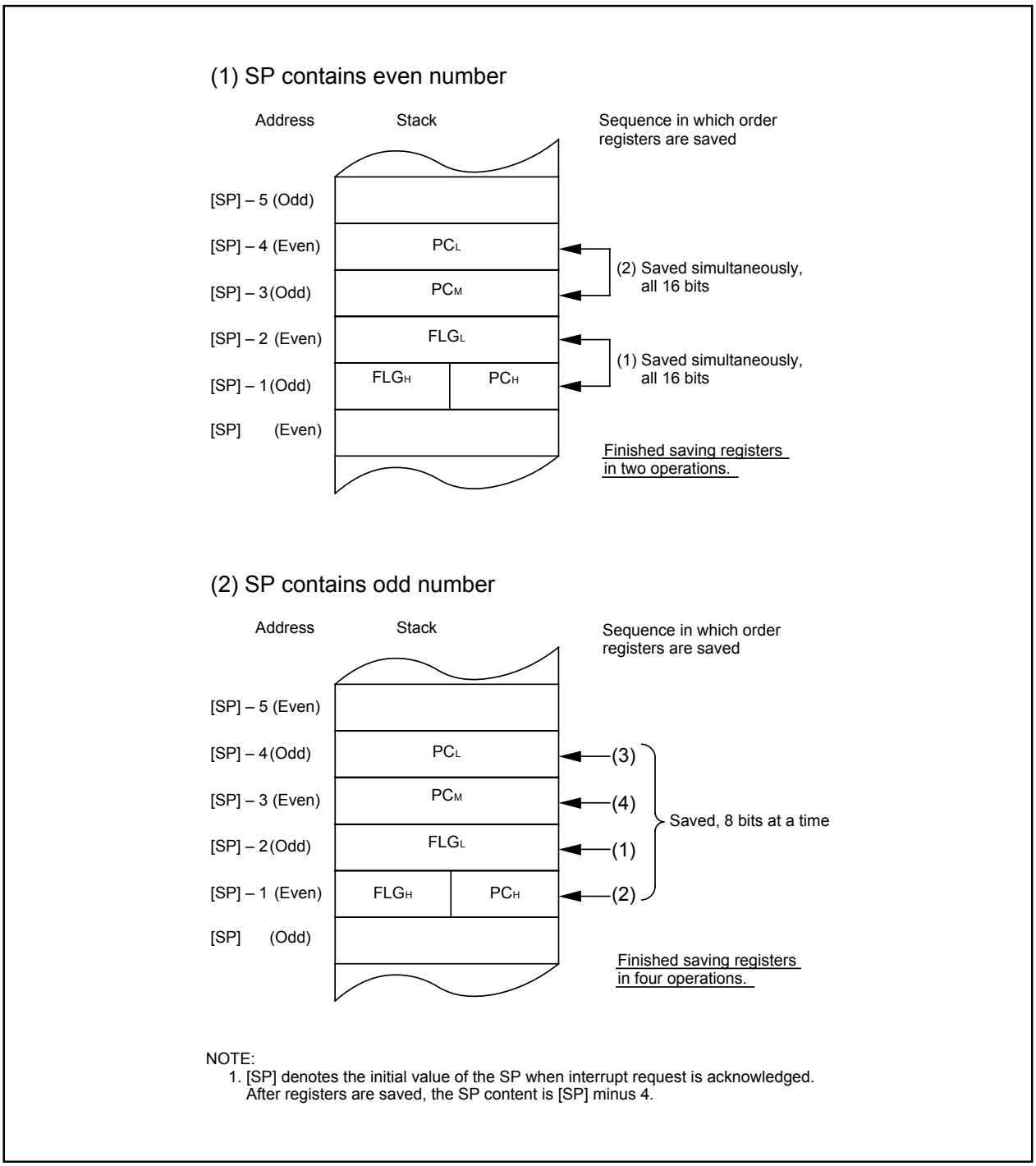


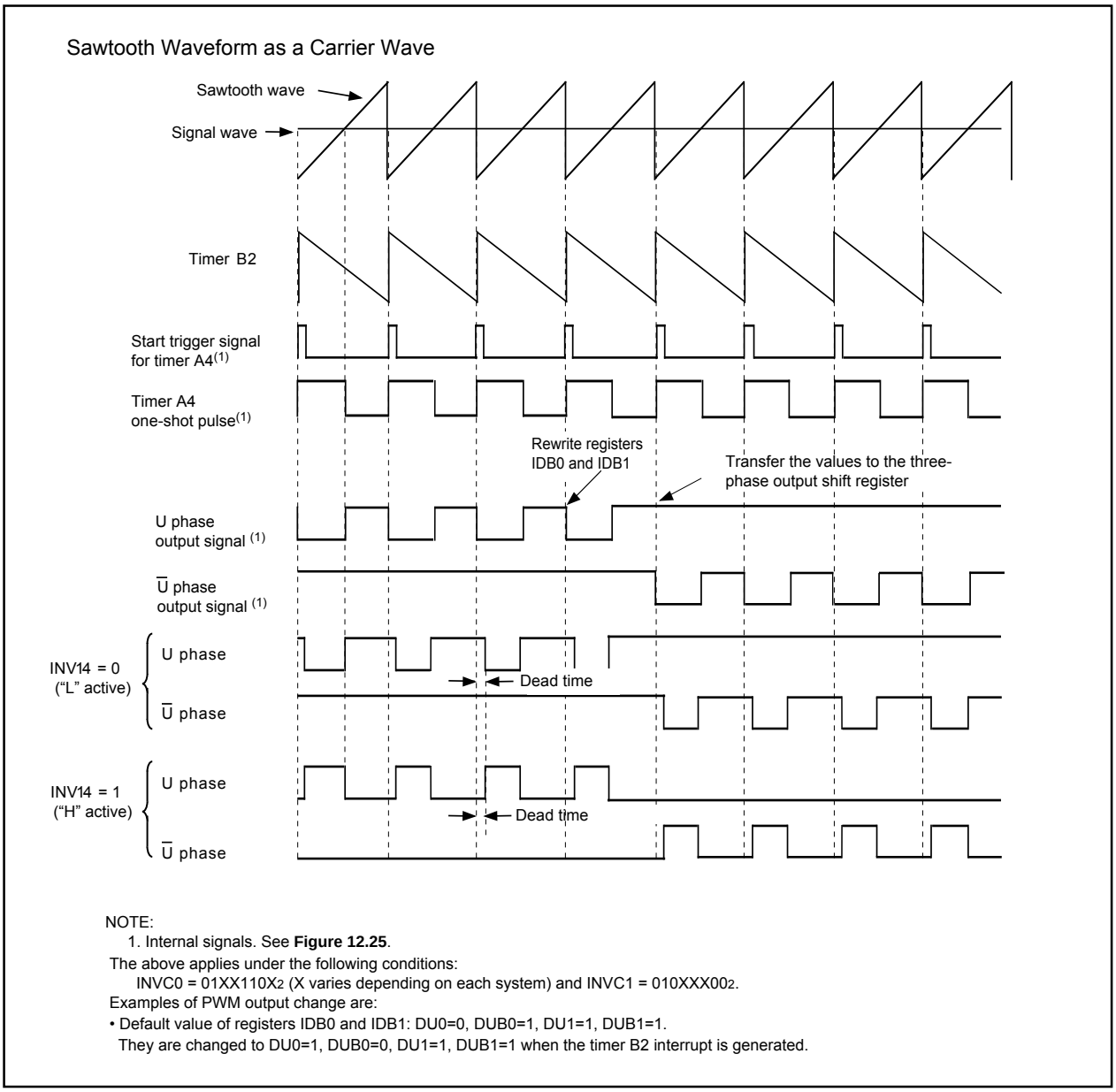
Figure 9.8 Operation of Saving Register

12.1.2 Event Counter Mode

In event counter mode, the timer counts pulses from an external device or overflows and underflows of other timers. Timers A2, A3, and A4 can count two-phase external signals. **Table 12.2** lists specifications in event counter mode (when not processing two-phase pulse signal). **Table 12.3** lists specifications in event counter mode (when processing two-phase pulse signal with the timers A2, A3 and A4). **Figure 12.8** shows TAiMR register in event counter mode (when not processing two-phase pulse signal). **Figure 12.9** shows TA2MR to TA4MR registers in event counter mode (when processing two-phase pulse signal with the timers A2, A3 and A4).

Table 12.2 Specifications in Event Counter Mode (when not processing two-phase pulse signal)

Item	Specification
Count source	• External signals input to TAiIN pin (i=0 to 4) (effective edge can be selected in program) • Timer B2 overflows or underflows, timer Aj (j=i-1, except j=4 if i=0) overflows or underflows, timer Ak (k=i+1, except k=0 if i=4) overflows or underflows
Count operation	• Increment or decrement can be selected by external signal or program • When the timer overflows or underflows, it reloads the reload register contents and continues counting. When operating in free-running mode, the timer continues counting without reloading.
Divided ratio	1/ (FFFF16 - n + 1) for increment 1/ (n + 1) for down-count n : set value of TAi register 000016 to FFFF16
Count start condition	Set TAiS bit in the TABSR register to 1 (start counting)
Count stop condition	Set TAiS bit to 0 (stop counting)
Interrupt request generation timing	Timer overflow or underflow
TAiIN pin function	I/O port or count source input
TAiOUT pin function	I/O port, pulse output, or up/down-count select input
Read from timer	Count value can be read by reading TAi register
Write to timer	• When not counting and until the 1st count source is input after counting start Value written to TAi register is written to both reload register and counter • When counting (after 1st count source input) Value written to TAi register is written to only reload register (Transferred to counter when reloaded next)
Select function	• Free-run count function Even when the timer overflows or underflows, the reload register content is not reloaded to it • Pulse output function Whenever the timer underflows or underflows, the output polarity of TAiOUT pin is inverted . When not counting, the pin outputs a low.



NOTE:
1. Internal signals. See **Figure 12.25**.

The above applies under the following conditions:
INVC0 = 01XX110X2 (X varies depending on each system) and INVC1 = 010XXX002.
Examples of PWM output change are:
• Default value of registers IDB0 and IDB1: DU0=0, DUB0=1, DU1=1, DUB1=1.
They are changed to DU0=1, DUB0=0, DU1=1, DUB1=1 when the timer B2 interrupt is generated.

Figure 12.34 Sawtooth Wave Modulation Operation

Table 14.3 lists pin functions for the case where the multiple transfer clock output pin select function is deselected. **Table 14.4** lists the P6$_4$ pin functions during clock synchronous serial I/O mode.
Note that for a period from when the UARTi operation mode is selected to when transfer starts, the TxDi pin outputs an “H”. (If the N-channel open-drain output is selected, this pin is in a high-impedance state.)

Table 14.3 Pin Functions (When Not Select Multiple Transfer Clock Output Pin Function)(1)

Pin Name	Function	Method of Selection
TxDi (i = 0 to 2) (P6$_3$, P6$_7$, P7$_0$)	Serial data output	(Outputs dummy data when performing reception only)
RxDi (P6$_2$, P6$_6$, P7$_1$)	Serial data input	Set the PD6_2 bit and PD6_6 bit in the PD6 register, and PD7_1 bit in the PD7 register to 0 (Can be used as an input port when performing transmission only)
CLKi (P6$_1$, P6$_5$, P7$_2$)	Transfer clock output	Set the CKDIR bit in the UiMR register to 0
	Transfer clock input	Set the CKDIR bit in the UiMR register to 1 Set the PD6_1 bit and PD6_5 bit in the PD6 register, and the PD7_2 bit in the PD7 register to 0
$\overline{\text{CTS}}$i/$\overline{\text{RTS}}$i (P6$_0$, P6$_4$, P7$_3$)	$\overline{\text{CTS}}$ input	Set the CRD bit in the UiC0 register to 0 Set the CRS bit in the UiC0 register to 0 Set the PD6_0 bit and PD6_4 bit in the PD6 register is set to 0, the PD7_3 bit in the PD7 register to 0
	$\overline{\text{RTS}}$ output	Set the CRD bit in the UiC0 register to 0 Set the CRS bit in the UiC0 register to 1
	I/O port	Set the CRD bit in the UiC0 register to 1

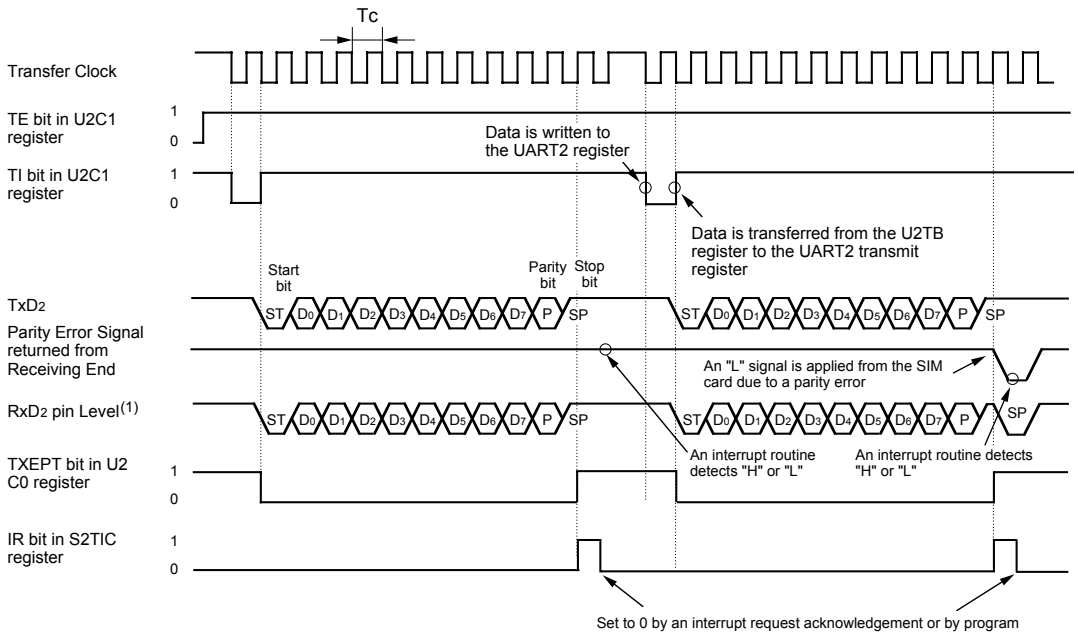
NOTE:
1: When the U1MAP bit in PACR register is 1 (P7$_3$ to P7$_0$), UART1 pin is assgined to P7$_3$ to P7$_0$.

Table 14.4 P6$_4$ Pin Functions(1)

Pin Function	Bit Set Value					
	U1C0 register		UCON register			PD6 register
	CRD	CRS	RCSP	CLKMD1	CLKMD0	PD6_4
P6$_4$	1	—	0	0	—	Input: 0, Output: 1
$\overline{\text{CTS}}_1$	0	0	0	0	—	0
$\overline{\text{RTS}}_1$	0	1	0	0	—	—
$\overline{\text{CTS}}_0$(2)	0	0	1	0	—	0
CLKS$_1$	—	—	—	1(3)	1	—

NOTES:
1. When the U1MAP bit in PACR register is 1 (P7$_3$ to P7$_0$), this table lists the P7$_0$ functions.
2. In addition to this, set the CRD bit in the U0C0 register to 0 ($\overline{\text{CT0}}_0$/$\overline{\text{RT0}}_0$ enabled) and the CRS bit in the U0C0 register to 1 ($\overline{\text{RTS}}_0$ selected).
3. When the CLKMD1 bit is set to 1 and the CLKMD0 bit is set to 0, the following logic levels are output:
   • High if the CLKPOL bit in the U1C0 register is set to 0
   • Low if the CLKPOL bit in the U1C0 register is set to 1

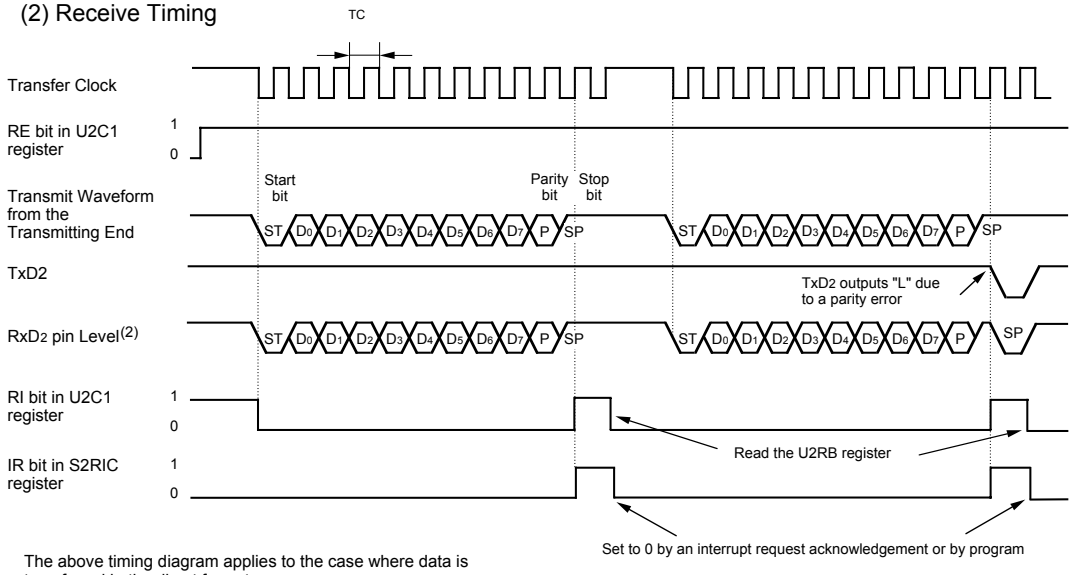
(1) Transmit Timing



The above timing diagram applies to the case where data is transferred in the direct format.
- U2MR register STPS bit = 0 (1 stop bit)
- U2MR register PRY bit = 1 (even)
- U2C0 register UFORM bit = 0 (LSB first)
- U2C1 register U2LCH bit = 0 (no reverse)
- U2C1 register U2IRSCH bit = 1 (transmit is completed)

$Tc = 16 (n + 1) / fi$ or $16 (n + 1) / f_{EXT}$
fi : frequency of U2BRG count source (f1SIO, f2SIO, f8SIO, f32SIO)
f_{EXT} : frequency of U2BRG count source (external clock)
n : value set to U2BRG

(2) Receive Timing



The above timing diagram applies to the case where data is transferred in the direct format.
- U2MR register STPS bit = 0 (1 stop bit)
- U2MR register PRY bit = 1 (even)
- U2C0 register UFORM bit = 0 (LSB first)
- U2C1 register U2LCH bit = 0 (no reverse)
- U2C1 register U2IRSCH bit = 1 (transmit is completed)

$Tc = 16 (n + 1) / fi$ or $16 (n + 1) / f_{EXT}$
fi : frequency of U2BRG count source (f1SIO, f2SIO, f8SIO, f32SIO)
f_{EXT} : frequency of U2BRG count source (external clock)
n : value set to U2BRG

NOTES:
1. Because TxD2 and RxD2 are connected, this is composite waveform consisting of the TxD2 output and the parity error signal sent back from receiver.
2. Because TxD2 and RxD2 are connected, this is composite waveform consisting of the transmitter's transmit waveform and the parity error signal received.

Figure 14.31 Transmit and Receive Timing in SIM Mode

15.1 Operating Modes

15.1.1 One-Shot Mode

In one-shot mode, analog voltage applied to a selected pin is once converted to a digital code. **Table 15.3** shows the one-shot mode specifications. **Figure 15.6** shows the operation example in one-shot mode. **Figure 15.7** shows registers ADCON0 to ADCON2 in one-shot mode.

Table 15.3 One-shot Mode Specifications

Item	Specification
Function	Bits CH2 to CH0 in the ADCON0 register and registers ADGSEL1 and ADGSEL0 in the ADCON2 register select pins. Analog voltage applied to a selected pin is once converted to a digital code
A/D Conversion Start Condition	• When the TRG bit in the ADCON0 register is 0 (software trigger) Set the ADST bit in the ADCON0 register to 1 (A/D conversion started) • When the TRG bit in the ADCON0 register is 1 (hardware trigger) The $\overline{\text{ADTRG}}$ pin input changes state from “H” to “L” after setting the ADST bit to 1 (A/D conversion started)
A/D Conversion Stop Condition	• A/D conversion completed (If a software trigger is selected, the ADST bit is set to 0 (A/D conversion halted)). • Set the ADST bit to 0
Interrupt Request Generation Timing	A/D conversion completed
Analog Input Pin	Select one pin from AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN3_0$ to $AN3_2$
Readout of A/D Conversion Result	Readout one of registers AD0 to AD7 that corresponds to the selected pin

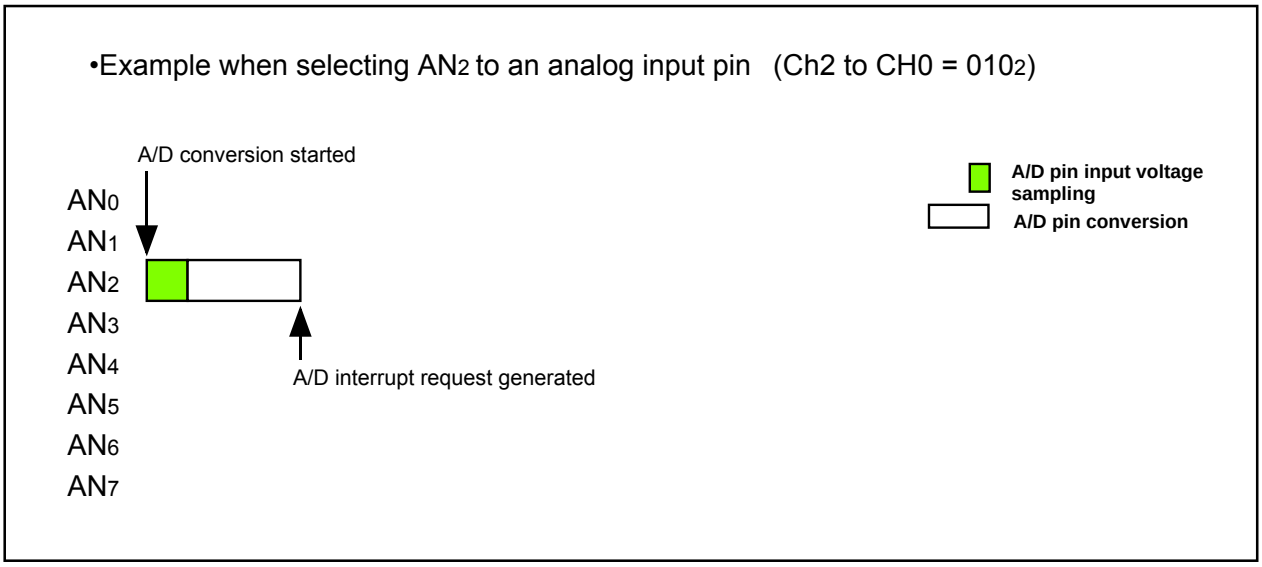
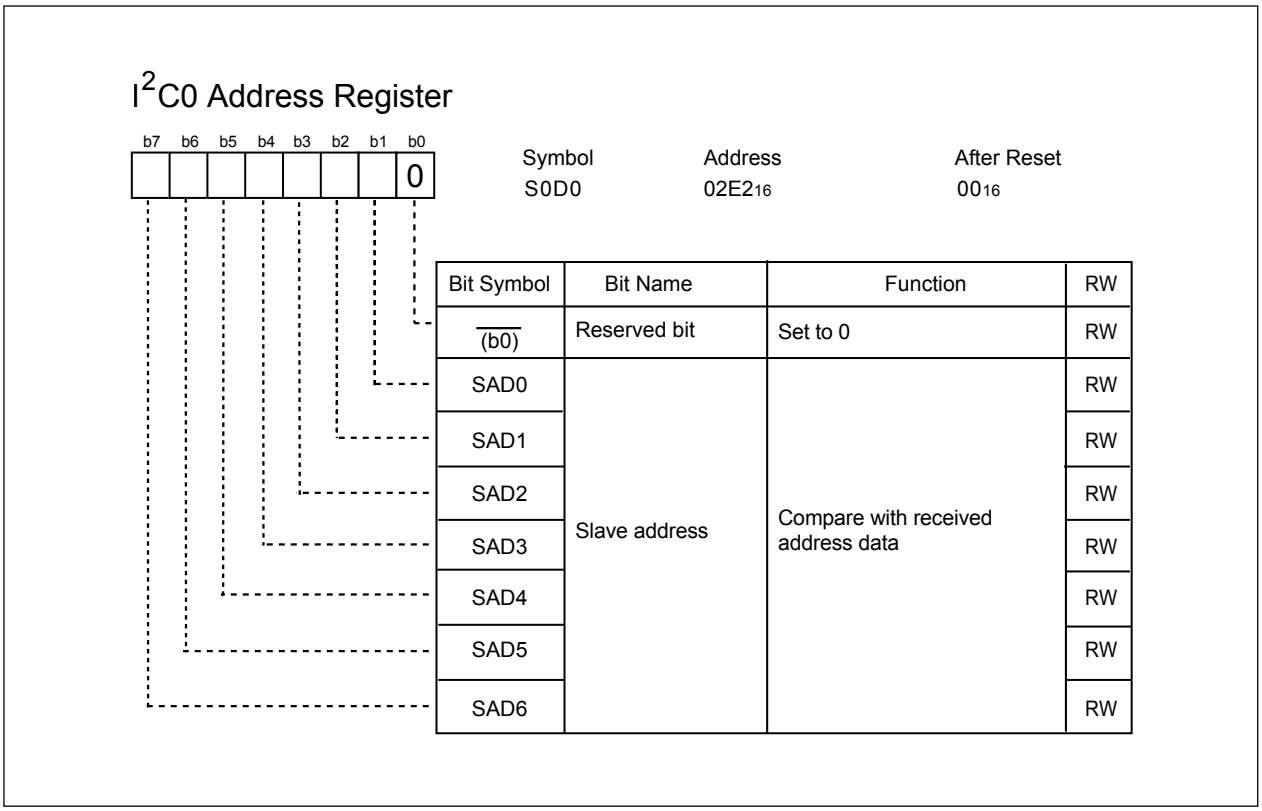


Figure 15.6 Operation Example in One-Shot Mode



Bit Symbol	Bit Name	Function	RW
$\overline{(b0)}$	Reserved bit	Set to 0	RW
SAD0	Slave address	Compare with received address data	RW
SAD1			RW
SAD2			RW
SAD3			RW
SAD4			RW
SAD5			RW
SAD6			RW

Figure 16.2 S0D0 Register

16.13 Address Data Communication

This section describes data transmit control when a master transferes data or a slave receives data in 7-bit address format. **Figure 16.20 (1)** shows a master transmit format.

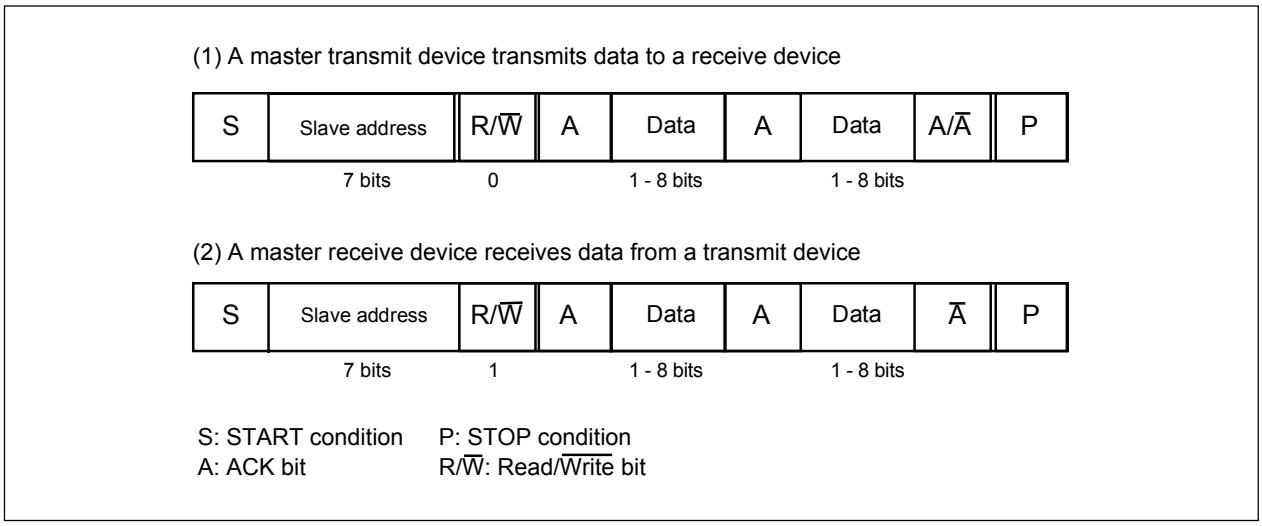


Figure 16.20 Address data communication format

16.13.1 Example of Master Transmit

For example, a master transmits data as shown below when following conditions are met: standard clock mode, SCL clock frequency of 100kHz and ACK clock added.

1) Set s slave address to the 7 high-order bits in the S0D0 register
2) Set 85_{16} to the S20 register, 000_2 to bits ICK4 to ICK2 in the S4D0 register and 00_{16} to the S3D0 registe to generate an ACK clock and set SCL clock frequency t 100 kHz (f_1=8MHz, f_{IIC}=f1)
3) Set 00_{16} to the S10 register to reset transmit/receive
4) Set 08_{16} to the S1D0 register to enable data communication
5) Confirm whether the bus is free by BB flag setting in the S10 register
6) Set $E0_{16}$ to the S10 register to enter START condition standby mode
7) Set the destination address in 7 high-order bits and 0 to a least significant bit in the S00 register to generate START condition. At this time, the first byte consisting of SCL and ACK clock are automatically generated
8) Set a transmit data to the S00 register. At this time, SCL and an ACK clock are automatically generated
9) When transmitting more than 1-byte control data, repeat the above step 8).
10) Set $C0_{16}$ in the S10 register to enter STOP condition standby mode if ACK is not returned from the slave receiver or if the transmit is completed
11) Write dummy data to the S00 regiser to generate STOP condition

17.7 Return from Bus off Function

When the protocol controller enters bus off state, it is possible to make it forced return from bus off state by setting the RetBusOff bit in the C0CTLR register to 1 (Force return from bus off). At this time, the error state changes from bus off state to error active state. If the RetBusOff bit is set to 1, registers C0RECR and C0TECR are initialized and the State_Reset bit in the C0STR register is set to 0 (The CAN module is not in error bus off state). However, registers of the CAN module such as C0CONR register and the content of each slot are not initialized.

17.8 Time Stamp Counter and Time Stamp Function

When the C0TSR register is read, the value of the time stamp counter at the moment is read. The period of the time stamp counter reference clock is the same as that of 1 bit time that is configured by the C0CONR register. The time stamp counter functions as a free run counter.

The 1 bit time period can be divided by 1 (undivided), 2, 4 or 8 to produce the time stamp counter reference clock. Use the TSPreScale bit in the C0CTLR register to select the divide-by-n value.

The time stamp counter is equipped with a register that captures the counter value when the protocol controller regards it as a successful reception. The captured value is stored when a time stamp value is stored in a reception slot.

17.9 Listen-Only Mode

When the RXOnly bit in the C0CTLR register is set to 1, the module enters listen-only mode.

In listen-only mode, no transmission -- data frames, error frames, and ACK response -- is performed to bus.

When listen-only mode is selected, do not request the transmission.

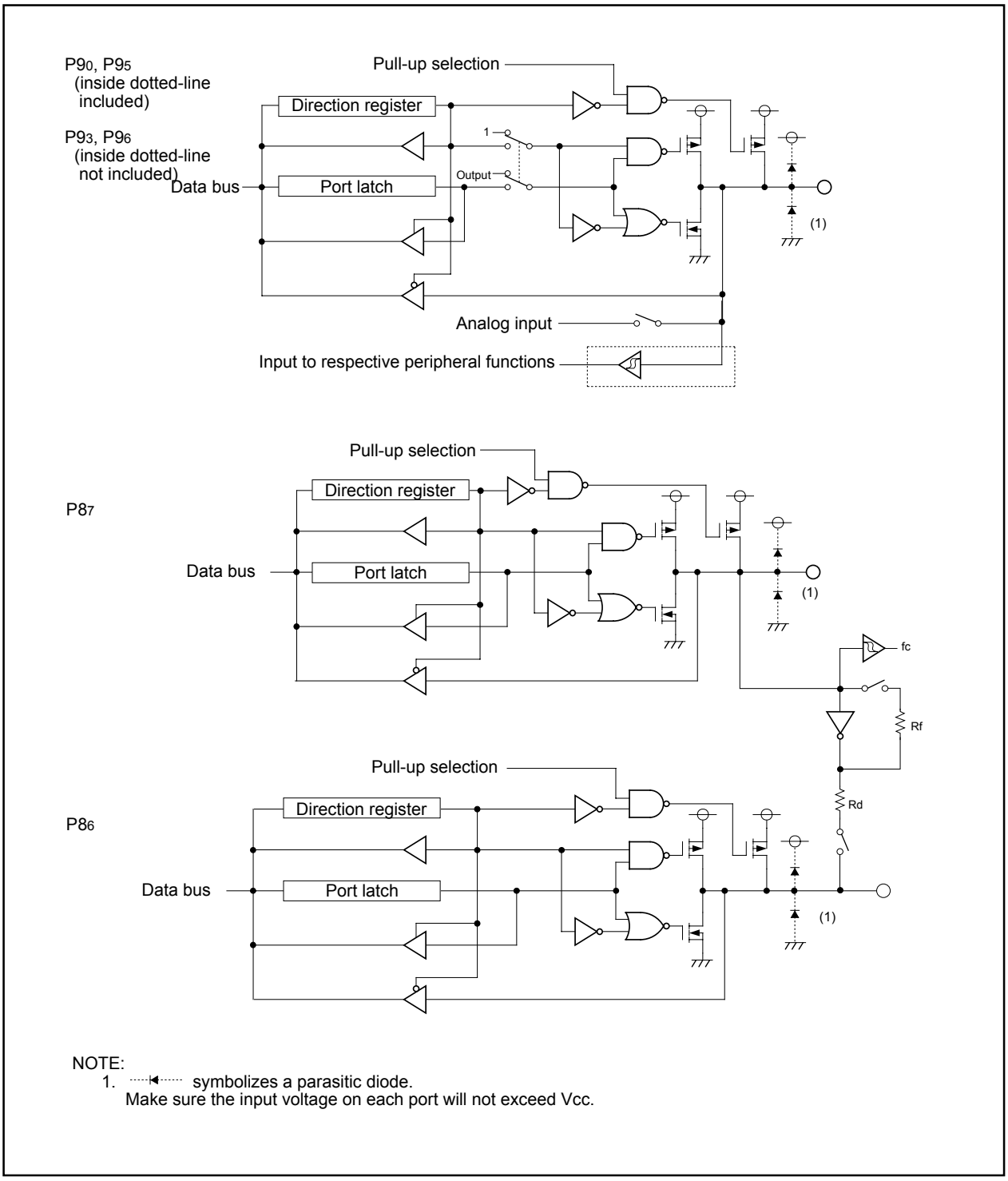
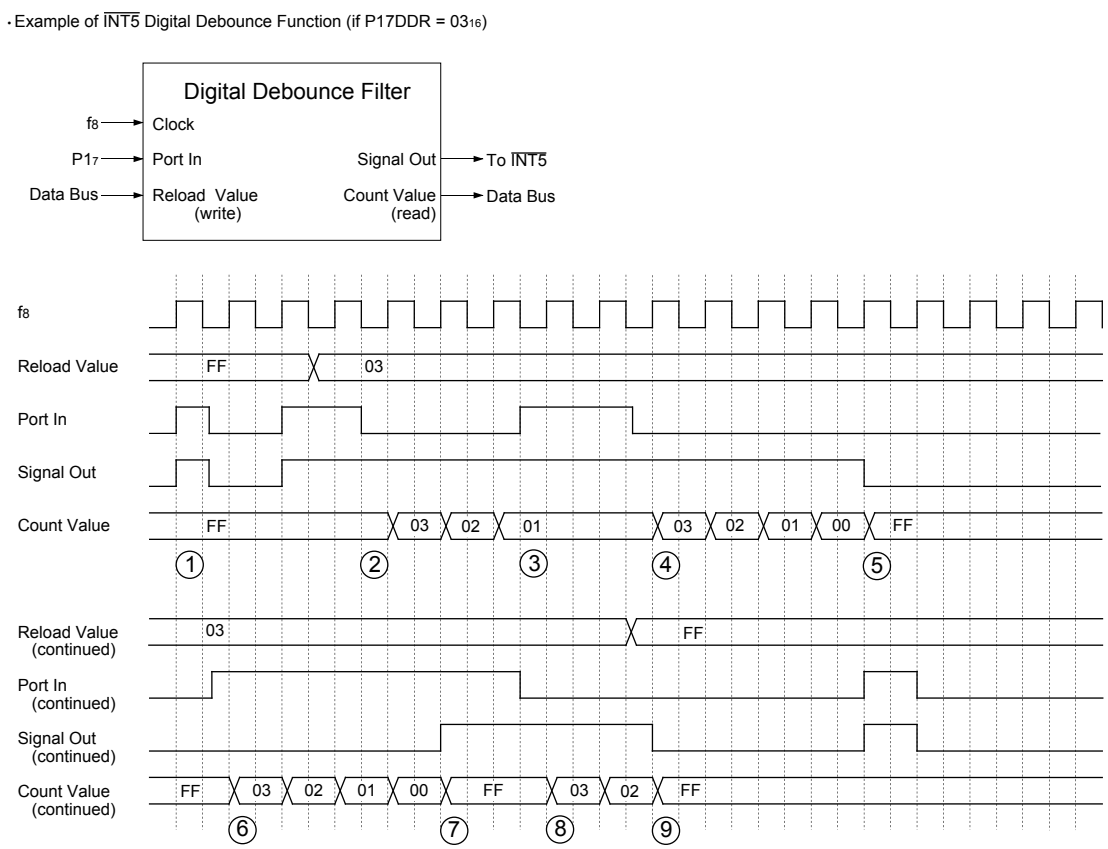


Figure 19.4 I/O Ports (4)



1. (Condition after reset). P17DDR=FF16. Pin input signal will be output directly.
2. Set the P17DDR register to 0316. The P17DDR register starts decrement along the f8 as a counter source, if the pin input level (e.g.,"L") and the signal output level (e.g.,"H") are not matched.
3. The P17DDR register will stops counting when the pin input level and the signal output level are matched (e.g., both levels are "H") while counting.
4. If the pin input level (e.g.,"L") and the signal output level (e.g.,"H") are not matched the P17DDR register will start decrement again after the setting value is reloaded.
5. When the P17DDR register is underflow, it stops counting and the signal output will output the same as pin input level (e.g."L").
6. If the pin input level (e.g.,"H") and the signal output level (e.g., "L") are not matched again, the P17DDR register will start decrement again after the setting value is reloaded.
7. When the P17DDR register is underflow, it stops counting and the signal output will output the same as pin input level (e.g."H").
8. If the pin input level (e.g.,"H") and the signal output level (e.g., "L") are not matched again, the P17DDR register will start decrement again after the setting value is reloaded.
9. Set the P17DDR register to FF16. The P17DDR register starts counting after the setting value is reloaded. Pin input signal will be output directly.

Figure 19.12 Functioning of Digital Debounce Filter

Flash Memory Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0
		0	0				

Symbol	Address	After Reset
FMR0	01B7$_{16}$	00000001$_2$

Bit Symbol	Bit Name	Function	RW
FMR00	RY/$\overline{BY}$ status flag	0: Busy (during writing or erasing) 1: Ready	RO
FMR01	CPU rewrite mode select bit (1)	0: Disables CPU rewrite mode (Disables software command) 1: Enables CPU rewrite mode (Enables software commands)	RW
FMR02	Block 0, 1 rewrite enable bit (2)	Set write protection for user ROM area (see **Table 20.4**)	RW
FMSTP	Flash memory stop bit (3, 5)	0: Starts flash memory operation 1: Stops flash memory operation (Enters low-power consumption state and flash memory reset)	RW
$\overline{(b5\text{-}b4)}$	Reserved bit	Set to 0	RW
FMR06	Program status flag (4)	0: Successfully completed 1: Completion error	RO
FMR07	Erase status flag (4)	0: Successfully completed 1: Completion error	RO

NOTES:
1. Set the FMR01 bit to 1 immediately after setting it first to 0. Do not generate an interrupt or a DMA transfer between setting the bit to 0 and setting it to 1. Set this bit while the P8$_5$/$\overline{NMI}$/$\overline{SD}$ pin is held “H” when selecting the $\overline{NMI}$ function. Set by program in a space other than the flash memory in EW mode 0. Set this bit to read alley mode and 0.
2. Set this bit to 1 immediately after setting it first to 0 while the FMR01 bit is set to 1. Do not generate an interrupt or a DMA transfer between setting this bit to 0 and setting it to 1.
3. Set this bit in a space other than the flash memory by program. When this bit is set to 1, access to flash memory will be denied. To set this bit to 0 after setting it to 1, wait for 10 usec. or more after setting it to 1. To read data from flash memory after setting this bit to 0, maintain tps wait time before accessing flash memory.
4. This bit is set to 0 by executing the clear status command.
5. This bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode). If the FMR01 bit is set to 0, this bit can be set to 1 by writing 1 to the FMR01 bit. However, the flash memory does not enter low-power consumption status and it is not initialized.

Flash Memory Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
		0	X	X	X		X

Symbol	Address	After Reset
FMR1	01B5$_{16}$	000XXX0X$_2$

Bit Symbol	Bit Name	Function	RW
$\overline{(b0)}$	Reserved bit	When read, the content is undefined	RO
FMR11	EW mode 1 select bit (1)	0: EW mode 0 1: EW mode 1	RW
$\overline{(b3\text{-}b2)}$	Reserved bit	When read, the content is undefined	RO
$\overline{(b4)}$	Nothing is assigned. If necessary, set to 0. When read, the content is undefined		—
$\overline{(b5)}$	Reserved bit	Set to 0	RW
FMR16	Block 0 to 5 rewrite enable bit (2)	Set write protection for user ROM space (see **Table 20.4**) 0: Disable 1: Enable	RW
FMR17	Block A, B access wait bit (3)	0: PM17 enabled 1: With wait state (1 wait)	RW

NOTES:
1. Set the FMR11 bit to 1 immediately after setting it first to 0 while the FMR01 bit is set to 1. Do not generate an interrupt or a DMA transfer between setting the bit to 0 and setting it to 1. Set this bit while the P8$_5$/$\overline{NMI}$/$\overline{SD}$ pin is held "H" when the $\overline{NMI}$ function is selected. If the FMR01 bit is set to 0, the FMR01 bit and FMR11 bit are both set to 0.
2. Set this bit to 1 immediately after setting it first to 0 while the FMR01 bit is set to 1. Do not generate an interrupt or a DMA transfer between setting this bit to 0 and setting it to 1.
3. When rewriting more than 100 times, set this bit to 1 (with wait state). When the FMR17 bit is set to1(with wait state), regardless of the PM17 bit setting, 1 wait state is inserted when accessing to blocks A and B. The PM17 bit setting is enabled, regardless of the FMR17 bit setting, as to the access to other block and the internal RAM.

Figure 20.6 FMR0 and FMR1 Registers

V_{CC} = 5V

Timing Requirements

(V_{CC} = 5V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 21.23 Multi-master I^2C bus Line

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
tBUF	Bus free time	4.7		1.3		µs
tHD;STA	The hold time in start condition	4.0		0.6		µs
tLOW	The hold time in SCL clock 0 status	4.7		1.3		µs
tR	SCL, SDA signals' rising time		1000	20+0.1Cb	300	ns
tHD;DAT	Data hold time	0		0	0.9	µs
tHIGH	The hold time in SCL clock 1 status	4.0		0.6		µs
tF	SCL, SDA signals' falling time		300	20+0.1Cb	300	ns
tSU;DAT	Data setup time	250		100		ns
tSU;STA	The setup time in restart condition	4.7		0.6		µs
tSU;STO	Stop condition setup time	4.0		0.6		µs

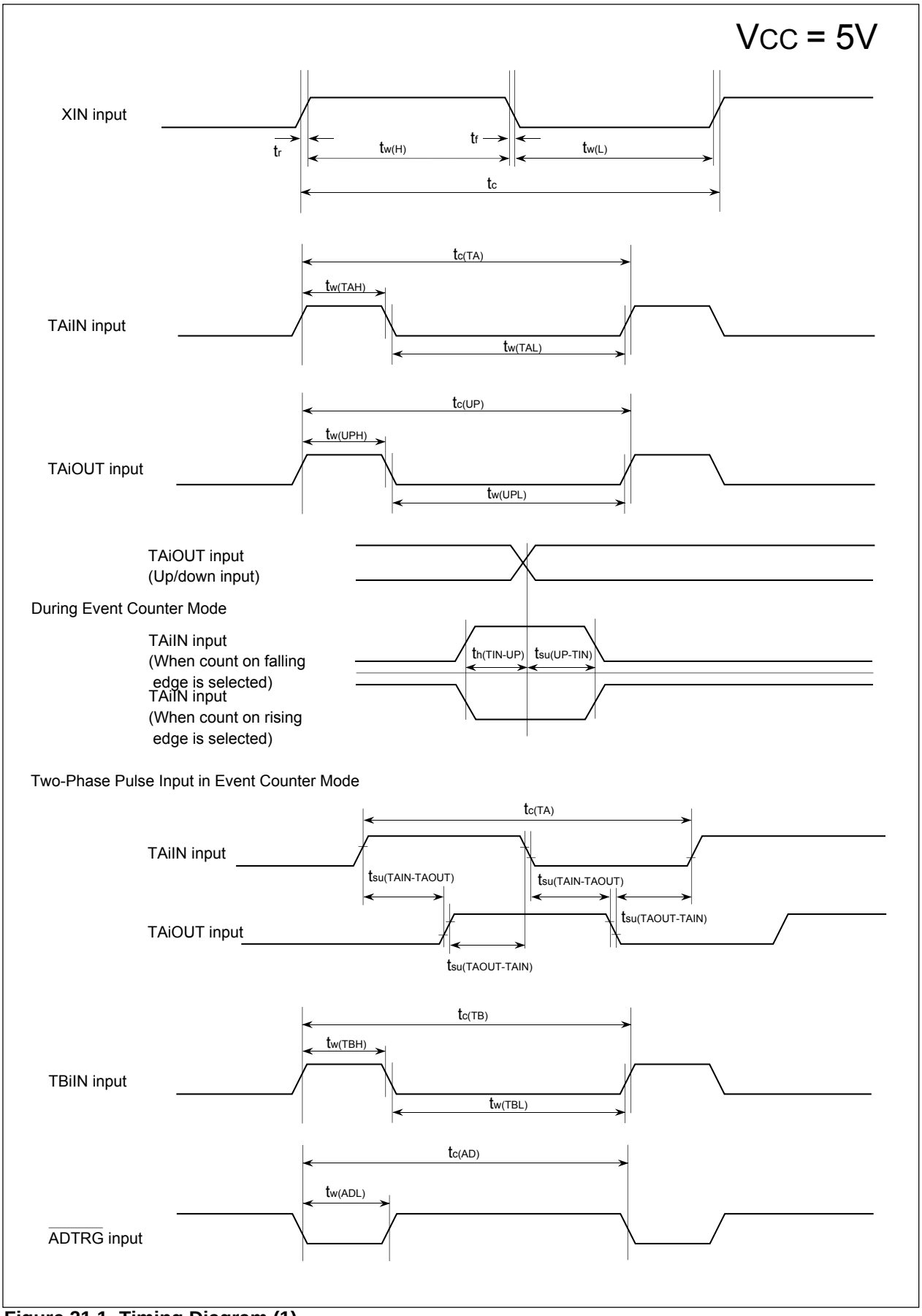


Figure 21.1 Timing Diagram (1)

Vcc = 5V

Timing Requirements

(Vcc=5V, Vss=0V, at Topr=-40 to 125°C unless otherwise specified)

Table 21.86 External Clock Input (XIN input)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
tc	External Clock Input Cycle Time	Topr=-40° C to 105° C	50		ns
		Topr=-40° C to 125° C	62.5		ns
$tw_{(H)}$	External Clock Input High ("H") Width	Topr=-40° C to 105° C	20		ns
		Topr=-40° C to 125° C	25		ns
$tw_{(L)}$	External Clock Input Low ("L") Width	Topr=-40° C to 105° C	20		ns
		Topr=-40° C to 125° C	25		ns
tr	External Clock Rise Time	Topr=-40° C to 105° C		9	ns
		Topr=-40° C to 125° C		15	ns
tf	External Clock Fall Time	Topr=-40° C to 105° C		9	ns
		Topr=-40° C to 125° C		15	ns

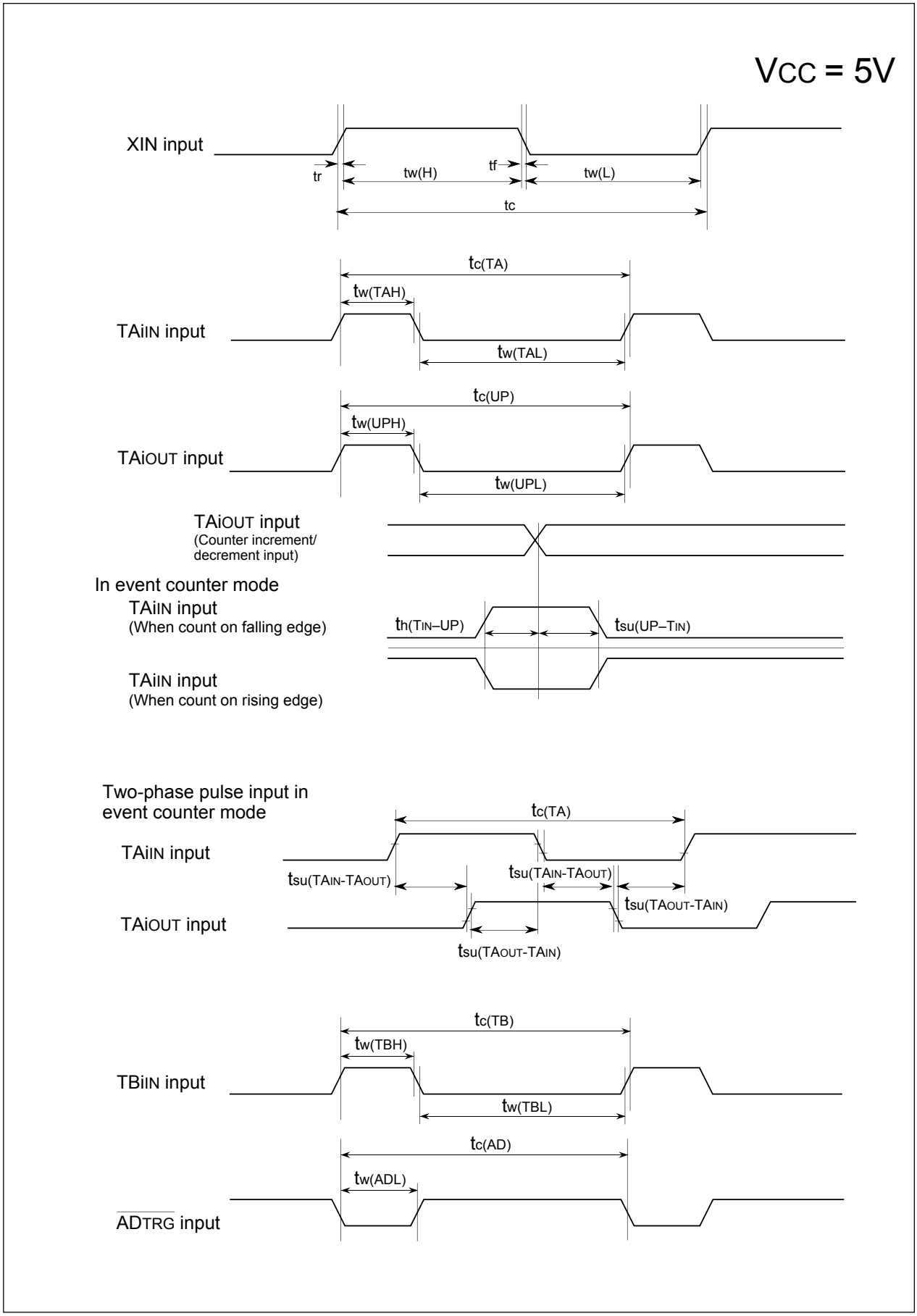


Figure 21.13 Timing Diagram (1)

Rev.	Date	Description	
		Page	Summary
			4 deleted
		401	• **Table 21.63 Elctrical Characteristics** measurement condition modified, note 4 deleted
		411	•**Tables 21.81 and 21.82 Flash Memory Version Electrical Characteristics** note 10 modified
		412	•Timing figure for td(P-R) and td(ROC) modified
		414	•**Table 21.85 Electrical Characteristics** measurment condition modified, note 4 deleted
			Usage Notes
		439	•**Figure 22.4 Use of Capacitors to Reduce Noise** note 1 modified
		449	•**22.15.10 How to Access** description modified
		450	•**22.15.15 Flash Memory Version Electrical Characteristics** 10,000 E/W Cycle Products description modified

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