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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	55
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30291fchp-u7a

1.3 Product List

Tables 1.3 to 1.5 list the M16C/29 Group products and **Figure 1.3** shows the type numbers, memory sizes and packages. **Tables 1.6 to 1.8** list the product code of flash memory version for M16C/29 Group. **Figure 1.4 to Figure 1.6** show the marking diagram of flash memory version for M16C/29 Group.

Table 1.3 Product List (1) -Normal Version **As of March, 2007**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30290FAHP	96 K + 4 K	8 K	PLQP0080KB-A (80P6Q-A)	Flash Memory	U3, U5, U7, U9
M30290FCHP	128 K + 4 K	12 K			
M30291FAHP	96 K + 4 K	8 K	PLQP0064KB-A (64P6Q-A)		
M30291FCHP	128 K + 4 K	12 K			
M30290M8-XXXHP	64 K	4 K	PLQP0080KB-A (80P6Q-A)	Mask ROM	U3, U5
M30290MA-XXXHP	96 K	8 K			
M30290MC-XXXHP	128 K	12 K			
M30291M8-XXXHP	64 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30291MA-XXXHP	96 K	8 K			
M30291MC-XXXHP	128 K	12 K			

Table 1.4 Product List (2) -T Version **As of March, 2007**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30290FATHP	96 K + 4 K	8 K	PLQP0080KB-A (80P6Q-A)	Flash Memory	U3, U5, U7, U9
M30290FCTHP	128 K + 4 K	12 K			
M30291FATHP	96 K + 4 K	8 K	PLQP0064KB-A (64P6Q-A)		
M30291FCTHP	128 K + 4 K	12 K			
M30290M8T-XXXHP	64 K	4 K	PLQP0080KB-A (80P6Q-A)	Mask ROM	U0
M30290MAT-XXXHP	96 K	8 K			
M30290MCT-XXXHP	128 K	12 K			
M30291M8T-XXXHP	64 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30291MAT-XXXHP	96 K	8 K			
M30291MCT-XXXHP	128 K	12 K			

Table 4.6 SFR Information (6)

Address	Register	Symbol	After reset
0140₁₆	CAN0 message box 14: Identifier/DLC		XX₁₆
0141₁₆			XX₁₆
0142₁₆			XX₁₆
0143₁₆			XX₁₆
0144₁₆			XX₁₆
0145₁₆			XX₁₆
0146₁₆	CAN0 message box 14 : Data field		XX₁₆
0147₁₆			XX₁₆
0148₁₆			XX₁₆
0149₁₆			XX₁₆
014A₁₆			XX₁₆
014B₁₆			XX₁₆
014C₁₆			XX₁₆
014D₁₆			XX₁₆
014E₁₆	CAN0 message box 14 : Time stamp		XX₁₆
014F₁₆			XX₁₆
0150₁₆	CAN0 message box 15 : Identifier/DLC		XX₁₆
0151₁₆			XX₁₆
0152₁₆			XX₁₆
0153₁₆			XX₁₆
0154₁₆			XX₁₆
0155₁₆			XX₁₆
0156₁₆	CAN0 message box 15 : Data field		XX₁₆
0157₁₆			XX₁₆
0158₁₆			XX₁₆
0159₁₆			XX₁₆
015A₁₆			XX₁₆
015B₁₆			XX₁₆
015C₁₆			XX₁₆
015D₁₆			XX₁₆
015E₁₆	CAN0 message box 15 : Time stamp		XX₁₆
015F₁₆			XX₁₆
0160₁₆	CAN0 global mask register	C0GMR	XX₁₆
0161₁₆			XX₁₆
0162₁₆			XX₁₆
0163₁₆			XX₁₆
0164₁₆			XX₁₆
0165₁₆			XX₁₆
0166₁₆	CAN0 local mask A register	C0LMAR	XX₁₆
0167₁₆			XX₁₆
0168₁₆			XX₁₆
0169₁₆			XX₁₆
016A₁₆			XX₁₆
016B₁₆			XX₁₆
016C₁₆	CAN0 local mask B register	C0LMBR	XX₁₆
016D₁₆			XX₁₆
016E₁₆			XX₁₆
016F₁₆			XX₁₆
0170₁₆			XX₁₆
0171₁₆			XX₁₆
≈			≈
01B3₁₆	Flash memory control register 4 (Note 2)	FMR4	0100000X₂
01B4₁₆			
01B5₁₆	Flash memory control register 1 (Note 2)	FMR1	000XXX0X₂
01B6₁₆			
01B7₁₆	Flash memory control register 0 (Note 2)	FMR0	01₁₆
≈			≈
01FD₁₆			
01FE₁₆			
01FF₁₆			

Note 1: The blank areas are reserved and cannot be used by users.
Note 2: This register is included in the flash memory version.

X : Undefined

9.7 $\overline{\text{NMI}}$ Interrupt

An $\overline{\text{NMI}}$ interrupt request is generated when input on the $\overline{\text{NMI}}$ pin changes state from high to low, after the $\overline{\text{NMI}}$ interrupt was enabled by writing a 1 to bit 4 in the register PM2. The $\overline{\text{NMI}}$ interrupt is a non-maskable interrupt, once it is enabled.

The input level of this $\overline{\text{NMI}}$ interrupt input pin can be read by accessing the P8_5 bit in the P8 register.

$\overline{\text{NMI}}$ is disabled by default after reset (the pin is a GPIO pin, $P8_5$) and can be enabled using bit 4 in the PM2 register. Once enabled, it can only be disabled by a reset signal.

The $\overline{\text{NMI}}$ input has a digital debounce function for noise rejection. Refer to "**19.6 Digital Debounce function**" for details. When using $\overline{\text{NMI}}$ interrupt to exit stop mode, set the NDDR register to FF_{16} before entering stop mode.

9.8 Key Input Interrupt

A key input interrupt is generated when input on any of the $P10_4$ to $P10_7$ pins which has had bits PD10_7 to PD10_4 in the PD10 register set to 0 (= input) goes low. Key input interrupts can be used for a key-on wakeup function to get the MCU to exit stop or wait modes. However, if you intend to use the key input interrupt, do not use $P10_4$ to $P10_7$ as analog input ports. **Figure 9.12** shows the block diagram of the key input interrupt. Note, however, that while input on any pin which has had bits PD10_7 to PD10_4 set to 0 (= input mode) is pulled low, inputs on all other pins of the port are not detected as interrupts.

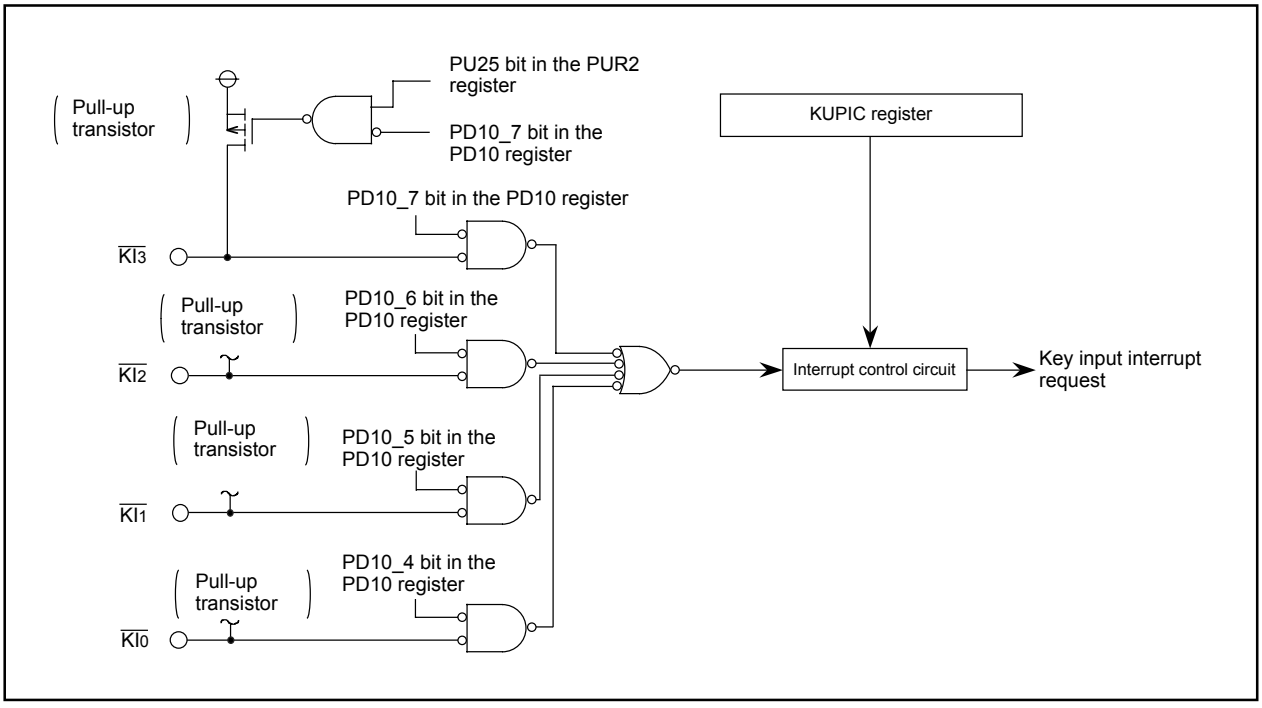


Figure 9.12 Key Input Interrupt

Divider Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
G1DV	$032A_{16}$	00_{16}

Function	Setting range	RW
Divide f_1, f_2 or two-phase pulse input by (n+1) for f_{BT1} clock cycles generation. n: the setting value of the G1DV register	00_{16} to FF_{16}	RW

Base Timer Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
0				0			0

Symbol	Address	After Reset
G1BCR1	0323_{16}	00_{16}

Bit Symbol	Bit Name	Function	RW
$\overline{\text{(b0)}}$	Reserved bit	Set to 0	RW
RST1	Base timer reset cause select bit 1	0: The base timer is not reset by matching the G1PO0 register 1: The base timer is reset by matching with the G1PO0 register (1)	RW
RST2	Base timer reset cause select bit 2	0: The base timer is not reset by applying "L" to the $\overline{\text{INT1}}$ pin 1: The base timer is reset by applying "L" to the $\overline{\text{INT1}}$ pin	RW
$\overline{\text{(b3)}}$	Reserved bit	Set to 0	RW
BTS	Base timer start bit	0: Base timer is reset 1: Base timer starts counting	RW
UD0	Counter increment/ decrement control bit	b6b5 0 0: Counter increment mode 0 1: Counter increment/decrement mode 1 0: Two-phase pulse signal processing mode 1 1: Do not set to this value	RW
UD1			RW
$\overline{\text{(b7)}}$	Reserved bit	Set to 0	RW

NOTS:
1. The base timer is reset two f_{BT1} clock cycles after the base timer matches the value set in the G1PO0 register. (See **Figure 13.7** for details on the G1PO0 register) When the RST1 bit is set to 1, the value of the G1POj register (j=1 to 7) for the waveform generating function must be set to a value smaller than that of the G1PO0 register.
When the RST1 bit is set to 1, set the RST4 bit in the G1BCR0 register to 0.

Figure 13.3 G1DV Register and G1BCR1 Register

13.6.1 INPC17 Alternate Input Pin Selection

The input capture pin for IC/OC channel 7 can be assigned to one of two package pins. The CH7INSEL bit in the G1BCR0 register selects IC/OC INPC17 from P27/OUTC17/INPC17 or P17/$\overline{\text{INT5}}$/INPC17/IDU.

13.6.2 Digital Debounce Function for Pin P17/$\overline{\text{INT5}}$/INPC17

The $\overline{\text{INT5}}$/INPC17 input from the P17/$\overline{\text{INT5}}$/INPC17/IDU pin has an effective digital debounce function against a noise rejection. Refer to **19.6 Digital Debounce function** for this detail.

Table 14.2 Registers to Be Used and Settings in Clock Synchronous Serial I/O Mode

Register	Bit	Function
UiTB(3)	0 to 7	Set transmission data
UiRB(3)	0 to 7	Reception data can be read
	OER	Overrun error flag
UiBRG	0 to 7	Set bit rate
UiMR(3)	SMD2 to SMD0	Set to 001_2
	CKDIR	Select the internal clock or external clock
	IOPOL(i=2) (4)	Set to 0
UiC0	CLK1 to CLK0	Select the count source for the UiBRG register
	CRS	Select $\overline{CTS}$ or $\overline{RTS}$ to use
	TXEPT	Transmit register empty flag
	CRD	Enable or disable the $\overline{CTS}$ or $\overline{RTS}$ function
	NCH	Select TxDi pin output mode
	CKPOL	Select the transfer clock polarity
	UFORM	Select the LSB first or MSB first
UiC1	TE	Set this bit to 1 to enable transmission/reception
	TI	Transmit buffer empty flag
	RE	Set this bit to 1 to enable reception
	RI	Reception complete flag
	U2IRS (1)	Select the source of UART2 transmit interrupt
	U2RRM (1)	Set this bit to 1 to use UART2 continuous receive mode
	U2LCH (3)	Set this bit to 1 to use UART2 inverted data logic
	U2ERE (3)	Set to 0
U2SMR	0 to 7	Set to 0
U2SMR2	0 to 7	Set to 0
U2SMR3	0 to 2	Set to 0
	NODC	Select clock output mode
	4 to 7	Set to 0
U2SMR4	0 to 7	Set to 0
UCON	U0IRS, U1IRS	Select the source of UART0/UART1 transmit interrupt
	U0RRM, U1RRM	Set this bit to 1 to use continuous receive mode
	CLKMD0	Select the transfer clock output pin when CLKMD1 is set to 1
	CLKMD1	Set this bit to 1 to output UART1 transfer clock from two pins
	RCSP	Set this bit to 1 to accept as input the UART0 $\overline{CTS_0}$ signal from the $P6_4$ pin
	7	Set to 0

NOTES:

1. Set bits 5 and 4 in registers U0C1 and U1C1 to 0. Bits U0IRS, U1IRS, U0RRM, and U1RRM are in the UCON register.
2. Not all register bits are described above. Set those bits to 0 when writing to the registers in clock synchronous serial I/O mode.
3. Set bits 7 and 6 in registers U0C1 and U1C1 to 0.
4. Set the bit 7 in registers U0MR and U1MR to 0.

i=0 to 2

15. A/D Converter

Note

Ports P04 to P07(AN04 to AN07), P10 to P13(AN20 to AN23) and P95 to P97(AN25 to AN27) are not available in 64-pin package. Do not use port P04 to P07(AN04 to AN07), P10 to P13(AN20 to AN23) and P95 to P97(AN25 to AN27) as analog input pins in 64-pin package.

The MCU contains one A/D converter circuit based on 10-bit successive approximation method configured with a capacitive-coupling amplifier. The analog inputs share the pins with P100 to P107 (AN0 to AN7), P00 to P07 (AN00 to AN07), and P10 to P13, P93, P95 to P97 (AN20 to AN27), and P90 to P92 (AN30 to AN32). Similarly, $\overline{\text{ADTRG}}$ input shares the pin with P15. Therefore, when using these inputs, make sure the corresponding port direction bits are set to 0 (input mode).

When not using the A/D converter, set the VCUT bit to 0 (Vref unconnected), so that no current will flow from the Vref pin into the resistor ladder, helping to reduce the power consumption of the chip.

The A/D conversion result is stored in the ADi register bits for ANi, AN0i, AN2i (i = 0 to 7), and AN3i pins (i = 0 to 2). **Table 15.1** shows the A/D converter performance. **Figure 15.1** shows the A/D converter block diagram and **Figures 15.2** to **15.4** show the A/D converter associated with registers.

Table 15.1 A/D Converter Performance

Item	Performance
A/D Conversion Method	Successive approximation (capacitive coupling amplifier)
Analog Input Voltage (1)	0V to AVCC (VCC)
Operating Clock ϕAD (2)	fAD/divided-by-2 or fAD/divided-by-3 or fAD/divided-by-4 or fAD/divided-by-6 or fAD/divided-by-12 or fAD
Resolution	8-bit or 10-bit (selectable)
Integral Nonlinearity Error	When AVCC = Vref = 5V • With 8-bit resolution: ±2LSB • With 10-bit resolution: ±3LSB When AVCC = Vref = 3.3V • With 8-bit resolution: ±2LSB • With 10-bit resolution: ±5LSB
Operating Modes	One-shot mode, repeat mode, single sweep mode, repeat sweep mode 0, repeat sweep mode 1, simultaneous sample sweep mode and delayed trigger mode 0,1
Analog Input Pins	8 pins (AN0 to AN7) + 8 pins (AN00 to AN07) + 8 pins (AN20 to AN27) + 3 pins (AN30 to AN32) (80-pin package) 8 pins (AN0 to AN7) + 4 pins (AN00 to AN03) + 1 pin (AN24) + 3 pins (AN30 to AN32) (64-pin package)
Conversion Speed Per Pin	• Without sample and hold function 8-bit resolution: 49 ϕAD cycles, 10-bit resolution: 59 ϕAD cycles • With sample and hold function 8-bit resolution: 28 ϕAD cycles, 10-bit resolution: 33 ϕAD cycles

NOTES:

1. Not dependent on use of sample and hold function.
2. Set the ϕAD frequency to 10 MHz or less.
   Without sample-and-hold function, set the ϕAD frequency to 250kHz or more.
   With the sample and hold function, set the ϕAD frequency to 1MHz or more.

A/D Trigger Control Register (1)

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	0	0	1	1

Symbol	Address	After Reset
ADTRGCON	$03D2_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
SSE	A/D operation mode select bit 2	Simultaneous sample sweep mode or delayed trigger mode 0, 1	RW
DTE	A/D operation mode select bit 3	Delayed trigger mode 0, 1	RW
HPTRG0	AN0 trigger select bit	See **Table 15.13**	RW
HPTRG1	AN1 trigger select bit	See **Table 15.13**	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—

NOTE:
1. If ADTRGCON is rewritten during A/D conversion, the conversion result will be undefined.

Figure 15.28 ADTRGCON Register in Delayed Trigger Mode 1

Table 15.13 Trigger Select Bit Setting in Delayed Trigger Mode 1

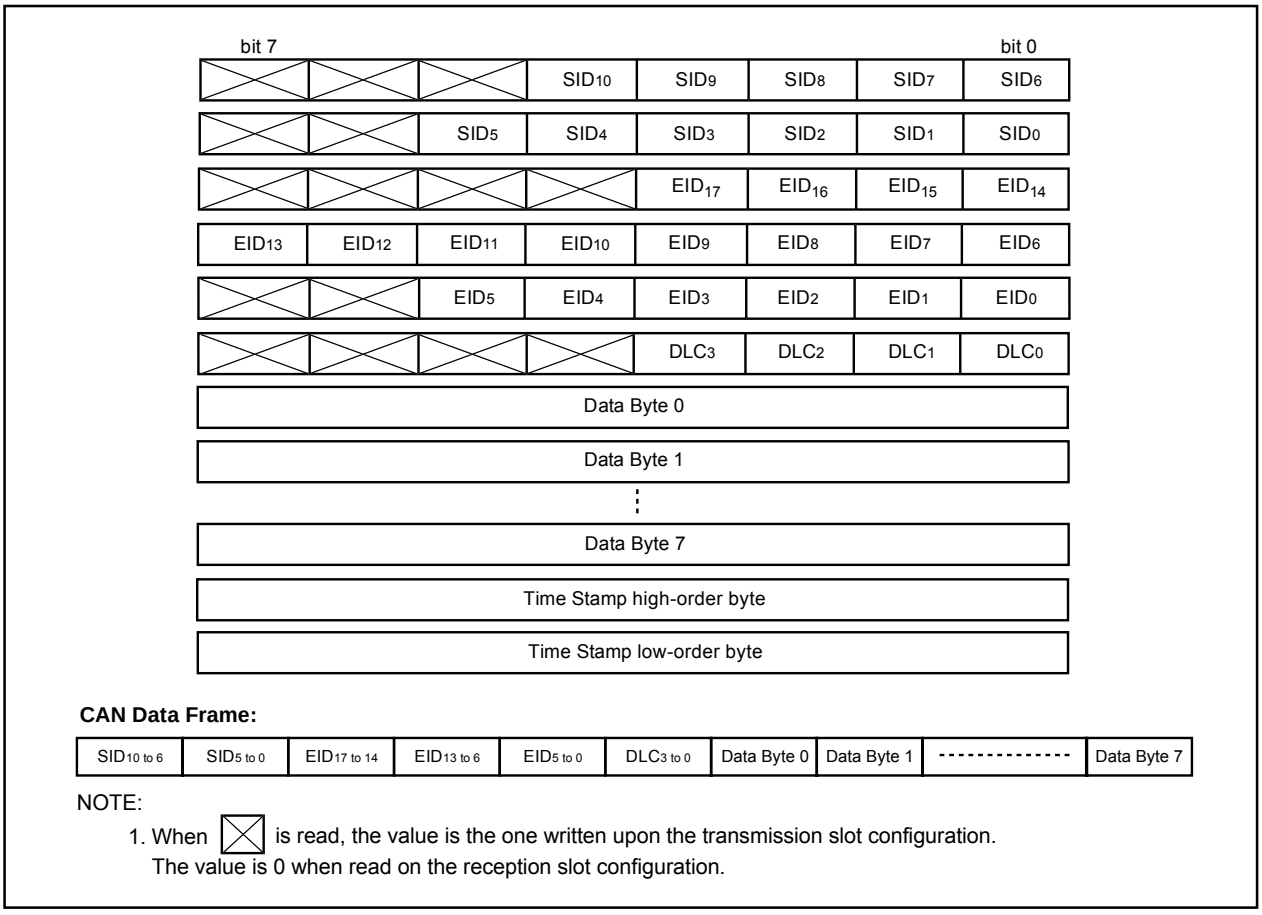
TRG	TRG1	HPTRG0	HPTRG1	Trigger
0	1	0	0	$\overline{\text{AD}}_{\text{TRG}}$

16.13.2 Example of Slave Receive

For example, a slave receives data as shown below when following conditions are met: high-speed clock mode, SCL frequency of 400 kHz, ACK clock added and addressing format.

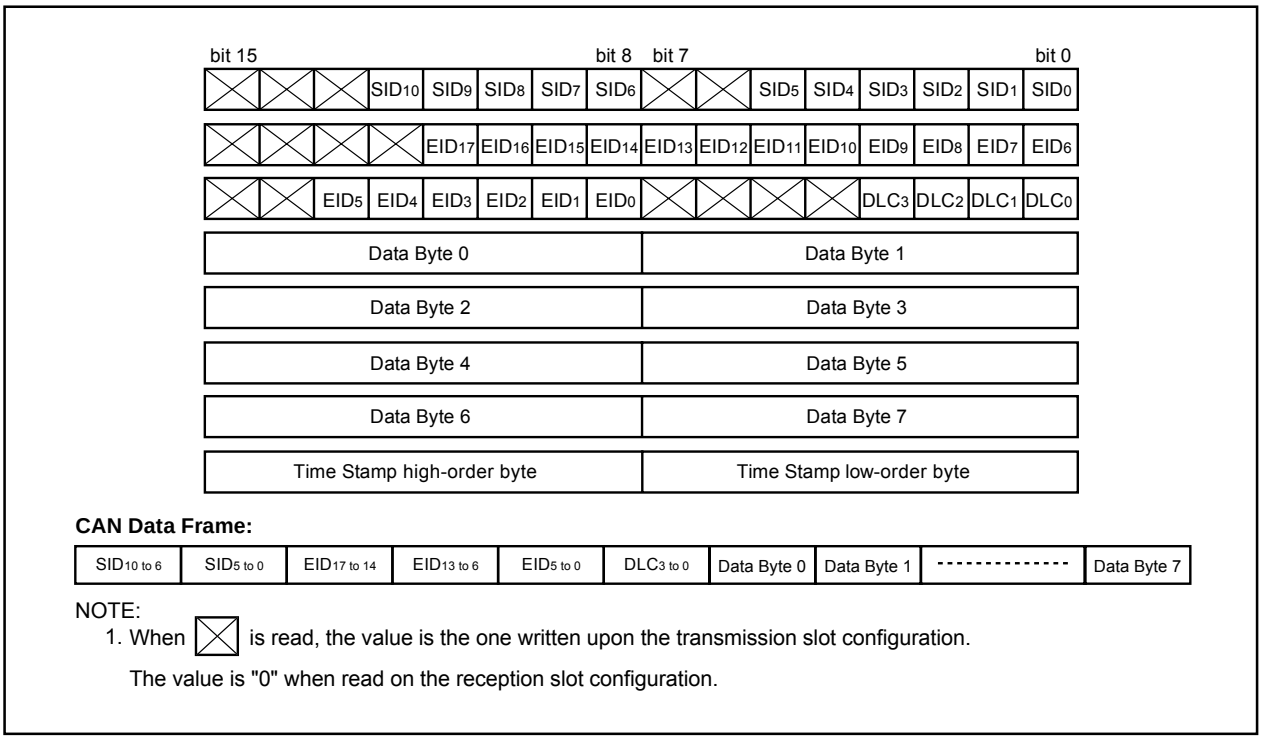
1) Set a slave address in the 7 high-order bits in the S0D0 register
2) Set $A5_{16}$ to the S20 register, 000_2 to bits ICK4 to ICK2 in the S4D0 register, and 00_{16} to the S3D0 register to generate an ACK clock and set SCL clock frequency at 400kHz (f_1 = 8 MHz, $f_{IIC} = f_1$)
3) Set 00_{16} to the S10 register to reset transmit/receive mode
4) Set 08_{16} to the S1D0 register to enable data communication
5) When a START condition is received, addresses are compared
6) •When the transmitted addresses are all 0 (general call), the ADR0 bit in the S10 register is set to 1 and an I2C bus interface interrupt request signal is generated.
   •When the transmitted addresses match with the address set in 1), the ASS bit in the S10 register is set to 1 and an I2C bus interface interrupt request signal is generated.
   •In other cases, bits ADR0 and AAS are set to 0 and I2C bus interface interrupt request signal is not generated.
7) Write dummy data to the S00 register.
8) After receiving 1-byte data, an ACK-CLK bit is automatically returned and an I2C bus interface interrupt request signal is generated.
9) To determine whether the ACK should be returned depending on contents in the received data, set dummy data to the S00 register to receive data after setting the WIT bit in te S3D0 register to 1 (enable the I2C bus interface interrupt of data receive completion). Because the I2C bus interface interrupt is generated when the 1-byte data is received, set the ACKBIT bit to 1 or 0 to output a signal from the ACKBIT bit.
10) When receiving more than 1-byte control data, repeat steps 7) and 8) or 7) and 9).
11) When a STOP condition is detected, the communication is ended.

Figures 17.2 and **17.3** show the bit mapping in each slot in byte access and word access. The content of each slot remains unchanged unless transmission or reception of a new message is performed.



NOTE:
1. When ☒ is read, the value is the one written upon the transmission slot configuration.
The value is 0 when read on the reception slot configuration.

Figure 17.2 Bit Mapping in Byte Access



NOTE:
1. When ☒ is read, the value is the one written upon the transmission slot configuration.
The value is "0" when read on the reception slot configuration.

Figure 17.3 Bit Mapping in Word Access

Port Control Register

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	X	X	X

Symbpl	Address	After Reset
PCR	$03FF_{16}$	00_{16}

Bit symbol	Bit Name	Function	RW
PCR0	Port P1 control bit	Operation performed when the P1 register is read 0: When the port is set for input, the input levels of $P1_0$ to $P1_7$ pins are read. When set for output, the port latch is read. 1: The port latch is read regardless of whether the port is set for input or output.	RW
—— (b7-b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—

Figure 19.9 PCR Register

Pin Assignment Control Register (1)

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X				

Symbpl	Address	After Reset
PACR	$025D_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
PACR0	Pin enabling bit	010 : 64 pin 011 : 80 pin All other values are reserved. Do not use.	RW
PACR1			RW
PACR2			RW
—— (b6-b3)	Reserved bits	Nothing is assigned. If necessary, set to 0. When read, the content is 0	—
U1MAP	UART1 pin remapping bit	UART1 pins assigned to 0 : $P6_7$ to $P6_4$ 1 : $P7_3$ to $P7_0$	RW

NOTE:
1. Set the PACR register by the next instruction after setting the PRC2 bit in the PRCR register to 1 (write enable).

Figure 19.10 PACR Register

ROM Code Protect Control Address(5)

b7	b6	b5	b4	b3	b2	b1	b0
				1	1	1	1

Symbol: ROMCP
Address: 0FFFFF16
Factory Setting: FF16 (4)

Bit Symbol	Bit Name	Function	RW
$\overline{(b5\text{-}b0)}$	Reserved Bit	Set to 1	RW
ROMCP1	ROM Code Protect Level 1 Set Bit (1, 2, 3, 4)	b7 b6 00: } Enables protect 01: } 10: 11: Disables protect	RW RW

NOTES:
1. When the ROM code protect is active by the ROMCP1 bit setting, the flash memory is protected against reading or rewriting in parallel I/O mode.
2. Set the bit 5 to bit 0 to 1111112 when the ROMCP1 bit is set to a value other than 112. When the bit 5 to bit 0 are set to values other than 1111112, the ROM code protection may not become active by setting the ROMCP1 bit to a value other than 112.
3. To make the ROM code protection inactive, erase a block including the ROMCP address in standard serial I/O mode or CPU rewrite mode.
4. The ROMCP address is set to FF16 when a block, including the ROMCP address, is erased.
5. When a value of the ROMCP address is 0016 or FF16, the ROM code protect function is disabled.

Figure 20.4 ROMCP Address

Address		
0FFFDF16 to 0FFFDC16	ID1	Undefined instruction vector
0FFFE316 to 0FFFE016	ID2	Overflow vector
0FFFE716 to 0FFFE416		BRK instruction vector
0FFFEB16 to 0FFFE816	ID3	Address match vector
0FFFEF16 to 0FFFEC16	ID4	Single step vector
0FFFF316 to 0FFFF016	ID5	Watchdog timer vector
0FFFF716 to 0FFFF416	ID6	$\overline{\text{DBC}}$ vector
0FFFFB16 to 0FFFF816	ID7	$\overline{\text{NMI}}$ vector
0FFFFF16 to 0FFFFC16	ROMCP	Reset vector

4 bytes

Figure 20.5 Address for ID Code Stored

20.11 CAN I/O Mode

Note

The CAN I/O mode is not available in M16C/29 T-ver./V-ver.

In CAN I/O mode, the user ROM area can be rewritten while the MCU is mounted on-board by using a CAN programmer which is applicable for the M16C/29 group. For more information about CAN programmers, contact the manufacturer of your CAN programmer. For details on how to use, refer to the user's manual included with your CAN programmer.
Table 20.9 lists pin functions for CAN I/O mode. Figures 20.19 and 20.20 show pin connections for CAN I/O mode.

20.11.1 ID code check function

This function determines whether the ID codes sent from the CAN programmer and those written in the flash memory match.(Refer to **20.3 Functions To Prevent Flash Memory from Rewriting**.)

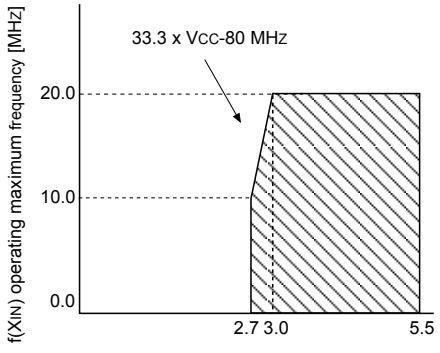
Table 21.2 Recommended Operating Conditions (Note 1)

Symbol	Parameter			Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply Voltage			2.7		5.5	V
AVcc	Analog Supply Voltage				Vcc		V
Vss	Supply Voltage				0		V
AVss	Analog Supply Voltage				0		V
V_{IH}	Input High ("H") Voltage	P0$_0$ to P0$_7$, P1$_0$ to P1$_7$, P2$_0$ to P2$_7$, P3$_0$ to P3$_7$, P6$_0$ to P6$_7$, P7$_0$ to P7$_7$, P8$_0$ to P8$_7$, P9$_0$ to P9$_3$, P9$_5$ to P9$_7$, P10$_0$ to P10$_7$		0.7Vcc		Vcc	V
		XIN, $\overline{\text{RESET}}$, CNVSS		0.8Vcc		Vcc	V
		SDAMM, SCLMM	When I^2C bus input level is selected	0.7Vcc		Vcc	V
			When SMBUS input level is selected	1.4		Vcc	V
V_{IL}	Input Low ("L") Voltage	P0$_0$ to P0$_7$, P1$_0$ to P1$_7$, P2$_0$ to P2$_7$, P3$_0$ to P3$_7$, P6$_0$ to P6$_7$, P7$_0$ to P7$_7$, P8$_0$ to P8$_7$, P9$_0$ to P9$_3$, P9$_5$ to P9$_7$, P10$_0$ to P10$_7$		0		0.3Vcc	V
		XIN, $\overline{\text{RESET}}$, CNVSS		0		0.2Vcc	V
		SDAMM, SCLMM	When I^2C bus input level is selected	0		0.3Vcc	V
			When SMBUS input level is selected	0		0.6	V
$I_{OH(peak)}$	Peak Output High ("H") Current	P0$_0$ to P0$_7$, P1$_0$ to P1$_7$, P2$_0$ to P2$_7$, P3$_0$ to P3$_7$, P6$_0$ to P6$_7$, P7$_0$ to P7$_7$, P8$_0$ to P8$_7$, P9$_0$ to P9$_3$, P9$_5$ to P9$_7$, P10$_0$ to P10$_7$				-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current	P0$_0$ to P0$_7$, P1$_0$ to P1$_7$, P2$_0$ to P2$_7$, P3$_0$ to P3$_7$, P6$_0$ to P6$_7$, P7$_0$ to P7$_7$, P8$_0$ to P8$_7$, P9$_0$ to P9$_3$, P9$_5$ to P9$_7$, P10$_0$ to P10$_7$				-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current	P0$_0$ to P0$_7$, P1$_0$ to P1$_7$, P2$_0$ to P2$_7$, P3$_0$ to P3$_7$, P6$_0$ to P6$_7$, P7$_0$ to P7$_7$, P8$_0$ to P8$_7$, P9$_0$ to P9$_3$, P9$_5$ to P9$_7$, P10$_0$ to P10$_7$				10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current	P0$_0$ to P0$_7$, P1$_0$ to P1$_7$, P2$_0$ to P2$_7$, P3$_0$ to P3$_7$, P6$_0$ to P6$_7$, P7$_0$ to P7$_7$, P8$_0$ to P8$_7$, P9$_0$ to P9$_3$, P9$_5$ to P9$_7$, P10$_0$ to P10$_7$				5.0	mA
f(XIN)	Main Clock Input Oscillation Frequency(4)		Vcc=3.0 to 5.5V	0		20	MHz
			Vcc=2.7 to 3.0V	0		33 X Vcc-80	MHz
f(XCIN)	Sub Clock Oscillation Frequency				32.768	50	kHz
f1(ROC)	On-chip Oscillator Frequency 1			0.5	1	2	MHz
f2(ROC)	On-chip Oscillator Frequency 2			1	2	4	MHz
f3(ROC)	On-chip Oscillator Frequency 3			8	16	26	MHz
f(PLL)	PLL Clock Oscillation Frequency(4)		Vcc=3.0 to 5.5V	10		20	MHz
			Vcc=2.7 to 3.0V	10		33 X Vcc-80	MHz
f(BCLK)	CPU Operation Clock Frequency			0		20	MHz
tsu(PLL)	Wait Time to Stabilize PLL Frequency Synthesizer		Vcc=5.0V			20	ms
			Vcc=3.0V			50	ms

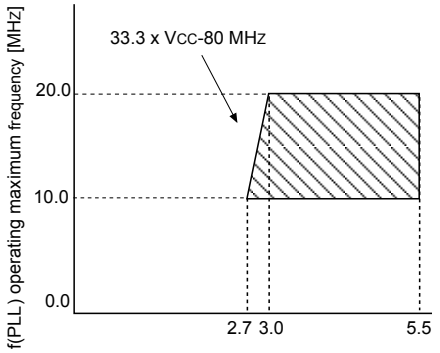
NOTES:

1. Referenced to Vcc = 2.7 to 5.5V at Topr = -20 to 85 ° C / -40 to 85 ° C unless otherwise specified.
2. The mean output current is the mean value within 100ms.
3. The total $I_{OL(peak)}$ for all ports must be 80mA or less. The total $I_{OH(peak)}$ for all ports must be -80mA or less.
4. Relationship among main clock oscillation frequency, PLL clock oscillation frequency and supply voltage.

Main clock input oscillation frequency



PLL clock oscillation frequency



VCC = 5V

Timing Requirements

(VCC = 5V, VSS = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 21.10 External Clock Input (XIN input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	50		ns
$t_{w(H)}$	External Clock Input High ("H") Width	20		ns
$t_{w(L)}$	External Clock Input Low ("L") Width	20		ns
tr	External Clock Rise Time		9	ns
tf	External Clock Fall Time		9	ns

V_{CC} = 3V

Timing Requirements

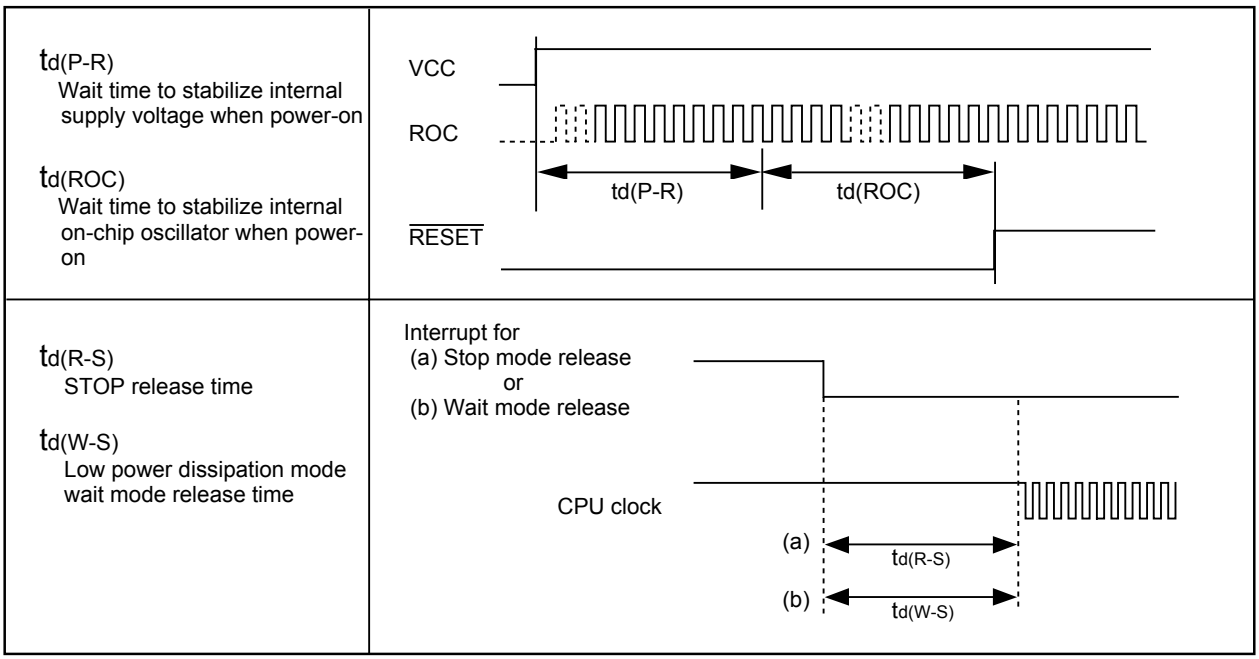
(V_{CC} = 3V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 21.39 Multi-master I²C bus Line

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
tBUF	Bus free time	4.7		1.3		µs
tHD;STA	The hold time in start condition	4.0		0.6		µs
tLOW	The hold time in SCL clock 0 status	4.7		1.3		µs
tR	SCL, SDA signals' rising time		1000	20+0.1Cb	300	ns
tHD;DAT	Data hold time	0		0	0.9	µs
tHIGH	The hold time in SCL clock 1 status	4.0		0.6		µs
tF	SCL, SDA signals' falling time		300	20+0.1Cb	300	ns
tsu;DAT	Data setup time	250		100		ns
tsu;STA	The setup time in restart condition	4.7		0.6		µs
tsu;STO	Stop condition setup time	4.0		0.6		µs

Table 21.45 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait Time to Stabilize Internal Supply Voltage when Power-on	V_{CC} = 3.0 to 5.5V			2	ms
td(ROC)	Wait Time to Stabilize Internal On-chip Oscillator when Power-on				40	µs
td(R-S)	STOP Release Time(1)				150	µs
td(W-S)	Low Power Dissipation Mode Wait Mode Release Time				150	µs



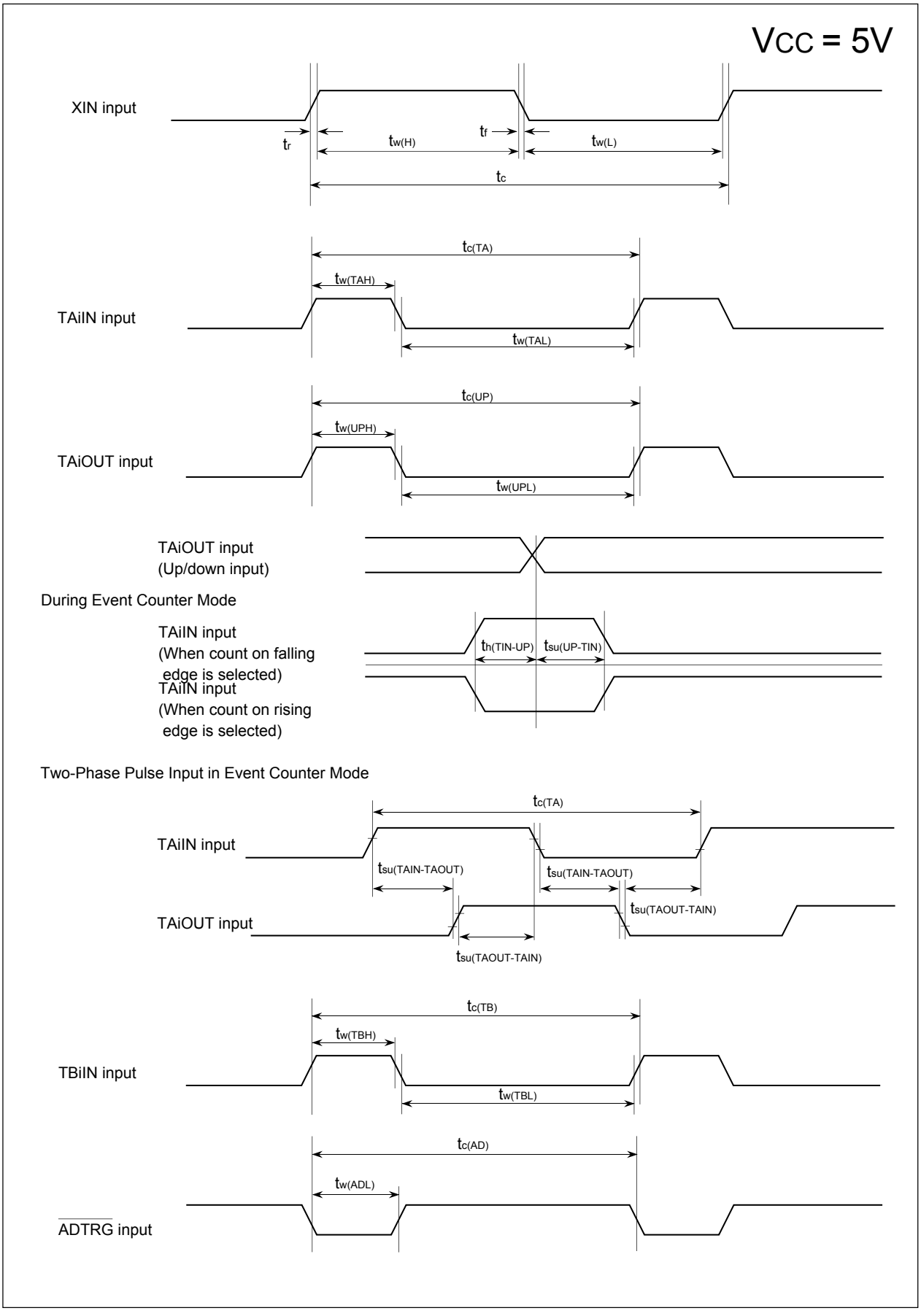


Figure 21.7 Timing Diagram (1)

Rev.	Date	Description	
		Page	Summary
		360	Table 21.1 is partly revised.
		368	Section “21.4.2 EW1 Mode” is partly revised.
0.80	Sep/03/Y04	2,3	Table 1.2.1 and Table 1.2.2 are partly revised.
		6,7	Table 1.4.1 to Table 1.4.3 are partly revised.
		7	Figure 1.4.1 is partly revised.
		8,9	Figure 1.5.1 and Figure 1.5.2 are partly revised.
		21	Figure 4.7 is partly revised.
		24	Figure 4.10 is partly revised.
		26	Section “5.1.2 Hardware Reset 2” is partly revised.
		29 to 34	Section “5.5 Voltage Detection Circuit” is revised.
		80	Section “10.2 Cold start / Warm start” is added.
		322	Table 20.2 is partly revised.
		323	Table 20.3 is partly revised.
		325	Table 20.6 and Table 20.7 are partly revised.
		327	Table 20.9 is partly revised.
		331	Title of Table 20.23 is partly revised.
		335	Table 20.25 is partly revised.
		339	Title of Table 20.39 is partly revised.
		343	Table 20.41 is partly revised.
		344	Table 20.42 is partly revised.
		346	“Low Voltage Detection Circuit Electrical Characteristics” is deleted.
			Talbe 20.45 is partly revised.
		348	Table 20.47 is partly revised.
		352	Title of Table 20.61 is partly revised.
		356	Talbe 20.63 is partly revised.
		360	Title of Table 20.77 is partly revised.
		398	64P6Q-A package is revised.
1.00	Nov/01/Y04	All pages	Words standardized (on-chip oscillator, A/D)
		2, 3	Table1.2.1 and Table 1.2.2 are partly revised.
		8, 9	Table 1.4.4 to 1.4.6 and figure1.4.2 to 1.4.6 are added.
		28	“5.1.2 Hardware Reset 2” is partly revised.
		29	“5.4 Oscillation Stop Detection Reset” is partly revised.
		38	Table 7.1 is partly revised.
		41	Note 6 in Figure 7.3 is partly revised. b7 to b4 bit in Figure 7.4 is revised.
		42	Figure 7.5 is partly revised.
		43	“PCLKR register” in Figure 7.6 is partly revised.
		50	“7.6.1 Normal Operation Mode” is partly revised.
		51	Note 1 in Table 7.6.1.1 is partly revised.
		57	“7.8 Oscillation Stop and Re-oscillation Detect Function” is partly revised.

Rev.	Date	Description	
		Page	Summary
		9	• **Tables 1.6** to **1.8** Product Codes modified
		19, 20	• **Table 1.14 Pin Description** pin description on I/O ports modified
			Reset
		37	• **Figure 5.2 Reset Sequence** Vcc and ROC timings modified
			Processor Mode
		45	• **Figure 6.2 PM2 Register** Description on notes 5 and 6 modified
			Clock Generation Circuit
		52	• **Figure 7.6 PM2 Register** Description on notes 5 and 6 modified
		64	• **Figure 7.12 State Transition in Normal Mode** note 2 modified
			Protection
		69	• Description on protection modified
			• **Figure 8.1 PRCR Register** note 1 modified
			Interrupts
		88	• **Table 9.6 PC Value Saved in Stack Area When Address Match Interrupt Request I Acknowledged** instruction modified
			Watchdog Timer
		90	• **Figure10.2 WDTS Register** modified
			• **10.1 Count Source Protective Mode** description modified
			Timer
		129	• **Figure 12.28 ICTB2 Register** modified
			Multi-Master I^2C bus Interface
		256	• **Figure 16.1 Block Diagram of Multi-Master I^2C bus Interface** modified
			Flash Memory Version
		335	• **20.3.1 ROM Code Protect Function** register name modified
		340	• **20.5.2 Flash Memory Control Register 1** description on FMR17 bit modified
		341	• **Figure 20.6 FMR1 Register** note 2 modified
		343	• **Figure 20.9 Setting and Resetting of EW Mode 1** modified
			Electrical Characteristics
		369	• **Table 21.5 Flash Memory Version Electrical Characteristics** note 10 modified
		370	• Timing figure for td(P-R) and td(ROC) modified
		372	• **Table 21.9 Electrical Characteristics** parameter and measurement condition modified, note 5 deleted
		380	• **Table 21.25 Electrical Characteristics** measurement condition modified, note 5 deleted
		390	• **Tables 21.43 and 44 Flash Memory Version Electrical Characteristics** note 10 modified
		391	• Timing figure for td(P-R) and td(ROC) modified
		393	• **Table 21.47 Electrical Characteristics** parameter and condition modified, note