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Applications of "Embedded - Microcontrollers"

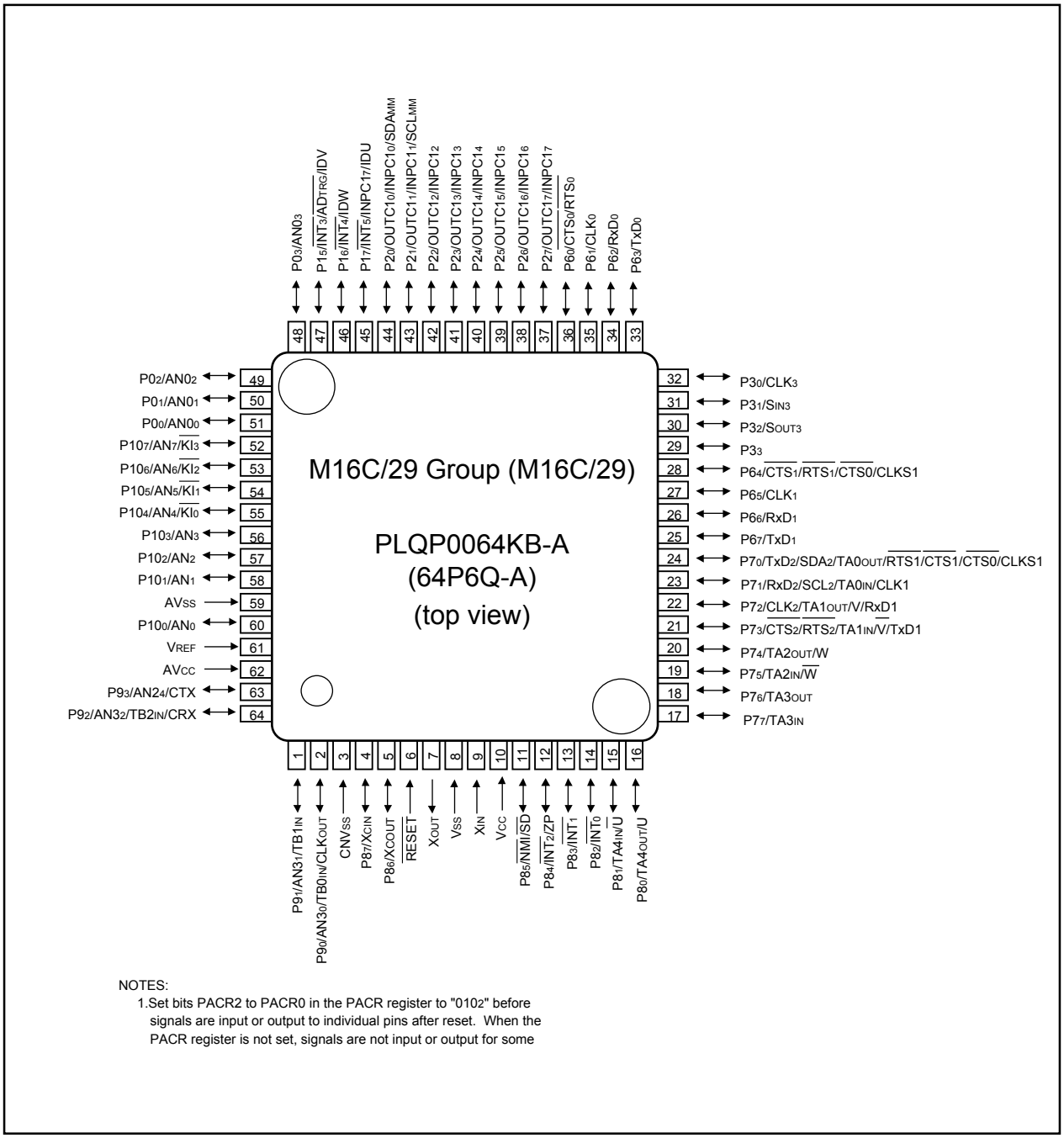
Details	
Product Status	Active
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	55
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30291fchp-u9a

Quick Reference to Pages Classified by Address

Address	Register	Symbol	Page
0080₁₆ 0081₁₆ 0082₁₆ 0083₁₆ 0084₁₆ 0085₁₆	CAN0 message box 2: Identifier/DLC		289
0086₁₆ 0087₁₆ 0088₁₆ 0089₁₆ 008A₁₆ 008B₁₆ 008C₁₆ 008D₁₆	CAN0 message box 2: Data field		289
008E₁₆ 008F₁₆	CAN0 message box 2: time stamp		289
0090₁₆ 0091₁₆ 0092₁₆ 0093₁₆ 0094₁₆ 0095₁₆	CAN0 message box 3: Identifier/DLC		289
0096₁₆ 0097₁₆ 0098₁₆ 0099₁₆ 009A₁₆ 009B₁₆ 009C₁₆ 009D₁₆	CAN0 message box 3: Data field		289
009E₁₆ 009F₁₆	CAN0 message box 3: time stamp		289
00A0₁₆ 00A1₁₆ 00A2₁₆ 00A3₁₆ 00A4₁₆ 00A5₁₆	CAN0 message box 4: Identifier/DLC		289
00A6₁₆ 00A7₁₆ 00A8₁₆ 00A9₁₆ 00AA₁₆ 00AB₁₆ 00AC₁₆ 00AD₁₆	CAN0 message box 4: Data field		289
00AE₁₆ 00AF₁₆	CAN0 message box 4: time stamp		289
00B0₁₆ 00B1₁₆ 00B2₁₆ 00B3₁₆ 00B4₁₆ 00B5₁₆	CAN0 message box 5: Identifier/DLC		289
00B6₁₆ 00B7₁₆ 00B8₁₆ 00B9₁₆ 00BA₁₆ 00BB₁₆ 00BC₁₆ 00BD₁₆	CAN0 message box 5: Data field		289
00BE₁₆ 00BF₁₆	CAN0 message box 5: time stamp		289

Address	Register	Symbol	Page
00C0₁₆ 00C1₁₆ 00C2₁₆ 00C3₁₆ 00C4₁₆ 00C5₁₆	CAN0 message box 6: Identifier/DLC		289
00C6₁₆ 00C7₁₆ 00C8₁₆ 00C9₁₆ 00CA₁₆ 00CB₁₆ 00CC₁₆ 00CD₁₆	CAN0 message box 6: Data field		289
00CE₁₆ 00CF₁₆	CAN0 message box 6: time stamp		289
00D0₁₆ 00D1₁₆ 00D2₁₆ 00D3₁₆ 00D4₁₆ 00D5₁₆	CAN0 message box 7: Identifier/DLC		289
00D6₁₆ 00D7₁₆ 00D8₁₆ 00D9₁₆ 00DA₁₆ 00DB₁₆ 00DC₁₆ 00DD₁₆	CAN0 message box 7: Data field		289
00DE₁₆ 00DF₁₆	CAN0 message box 7: time stamp		289
00E0₁₆ 00E1₁₆ 00E2₁₆ 00E3₁₆ 00E4₁₆ 00E5₁₆	CAN0 message box 8: Identifier/DLC		289
00E6₁₆ 00E7₁₆ 00E8₁₆ 00E9₁₆ 00EA₁₆ 00EB₁₆ 00EC₁₆ 00ED₁₆	CAN0 message box 8: Data field		289
00EE₁₆ 00EF₁₆	CAN0 message box 8: time stamp		289
00F0₁₆ 00F1₁₆ 00F2₁₆ 00F3₁₆ 00F4₁₆ 00F5₁₆	CAN0 message box 9: Identifier/DLC		289
00F6₁₆ 00F7₁₆ 00F8₁₆ 00F9₁₆ 00FA₁₆ 00FB₁₆ 00FC₁₆ 00FD₁₆	CAN0 message box 9: Data field		289
00FE₁₆ 00FF₁₆	CAN0 message box 9: time stamp		289

Note: The blank areas are reserved and cannot be accessed by users.



NOTES:
1.Set bits PACR2 to PACR0 in the PACR register to "010₂" before signals are input or output to individual pins after reset. When the PACR register is not set, signals are not input or output for some

Figure 1.9 Pin Assignment (Top View) of 64-Pin Package

Table 4.9 SFR Information (9)

Address	Register	Symbol	After reset
0340₁₆			
0341₁₆			
0342₁₆	Timer A1-1 register	TA11	XX₁₆
0343₁₆			XX₁₆
0344₁₆	Timer A2-1 register	TA21	XX₁₆
0345₁₆			XX₁₆
0346₁₆	Timer A4-1 register	TA41	XX₁₆
0347₁₆			XX₁₆
0348₁₆	Three phase PWM control register 0	INVC0	00₁₆
0349₁₆	Three phase PWM control register 1	INVC1	00₁₆
034A₁₆	Three phase output buffer register 0	IDB0	00₁₆
034B₁₆	Three phase output buffer register 1	IDB1	00₁₆
034C₁₆	Dead time timer	DTT	XX₁₆
034D₁₆	Timer B2 Interrupt occurrence frequency set counter	ICTB2	XX₁₆
034E₁₆	Position - data - retain function control register	PDRF	XXXX0000₂
034F₁₆			
0350₁₆			
0351₁₆			
0352₁₆			
0353₁₆			
0354₁₆			
0355₁₆			
0356₁₆			
0357₁₆			
0358₁₆	Port function control register	PFCR	00111111₂
0359₁₆			
035A₁₆			
035B₁₆			
035C₁₆			
035D₁₆			
035E₁₆	Interrupt cause select register 2(2)	IFSR2A	00XXX000₂
035F₁₆	Interrupt cause select register	IFSR	00₁₆
0360₁₆	SI/O3 transmit/receive register	S3TRR	XX₁₆
0361₁₆			
0362₁₆	SI/O3 control register	S3C	01000000₂
0363₁₆	SI/O3 bit rate register	S3BRG	XX₁₆
0364₁₆	SI/O4 transmit/receive register	S4TRR	XX₁₆
0365₁₆			
0366₁₆	SI/O4 control register	S4C	01000000₂
0367₁₆	SI/O4 bit rate register	S4BRG	XX₁₆
0368₁₆			
0369₁₆			
036A₁₆			
036B₁₆			
036C₁₆			
036D₁₆			
036E₁₆			
036F₁₆			
0370₁₆			
0371₁₆			
0372₁₆			
0373₁₆			
0374₁₆	UART2 special mode register 4	U2SMR4	00₁₆
0375₁₆	UART2 special mode register 3	U2SMR3	000X0X0X₂
0376₁₆	UART2 special mode register 2	U2SMR2	X0000000₂
0377₁₆	UART2 special mode register	U2SMR	X0000000₂
0378₁₆	UART2 transmit/receive mode register	U2MR	00₁₆
0379₁₆	UART2 bit rate register	U2BRG	XX₁₆
037A₁₆	UART2 transmit buffer register	U2TB	XX₁₆
037B₁₆			XX₁₆
037C₁₆	UART2 transmit/receive control register 0	U2C0	00001000₂
037D₁₆	UART2 transmit/receive control register 1	U2C1	00000010₂
037E₁₆	UART2 receive buffer register	U2RB	XX₁₆
037F₁₆			XX₁₆

Note 1: The blank areas are reserved and cannot be used by users.
Note 2: Write 0 to the bit 0 after reset.

X : Undefined

The operation of saving registers carried out in the interrupt sequence is dependent on whether the SP(1), at the time of acceptance of an interrupt request, is even or odd. If the stack pointer (1) is even, the FLG register and the PC are saved, 16 bits at a time. If odd, they are saved in two steps, 8 bits at a time. **Figure 9.8** shows the operation of the saving registers.

NOTE:
1. When any INT instruction in software numbers 32 to 63 has been executed, this is the SP indicated by the U flag. Otherwise, it is the ISP.

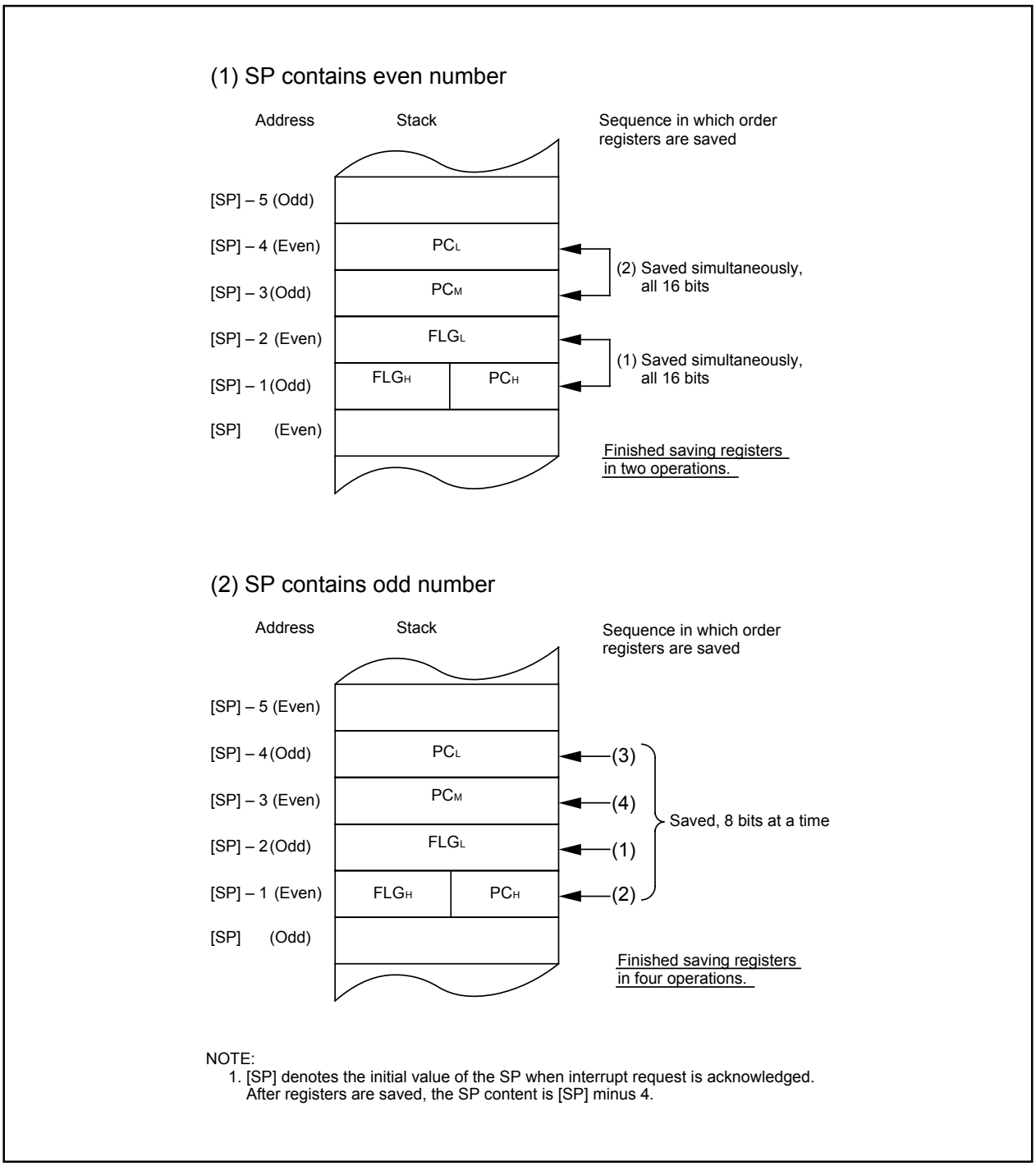
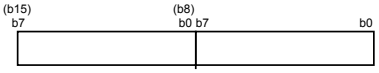


Figure 9.8 Operation of Saving Register

Timer Ai Register (i= 0 to 4) (1)

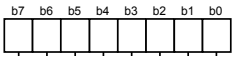


Symbol	Address	After Reset
TA0	038716, 038616	Undefined
TA1	038916, 038816	Undefined
TA2	038B16, 038A16	Undefined
TA3	038D16, 038C16	Undefined
TA4	038F16, 038E16	Undefined

Mode	Function	Setting Range	RW
Timer mode	Divide the count source by n + 1 where n = set value	000016 to FFFF16	RW
Event counter mode	Divide the count source by FFFF16 – n + 1 where n = set value when counting up or by n + 1 when counting down(5)	000016 to FFFF16	RW
One-shot timer mode	Divide the count source by n where n = set value and cause the timer to stop	000016 to FFFF16 (2, 4)	WO
Pulse width modulation mode (16-bit PWM)	Modify the pulse width as follows: PWM period: (216 – 1) / fj High level PWM pulse width: n / fj where n = set value, fj = count source frequency	000016 to FFFE16 (3, 4)	WO
Pulse width modulation mode (8-bit PWM)	Modify the pulse width as follows: PWM period: (28 – 1) x (m + 1)/ fj High level PWM pulse width: (m + 1)n / fj where n = high-order address set value, m = low-order address set value, fj = count source frequency	0016 to FE16 (High-order address) 0016 to FF16 (Low-order address) (3, 4)	WO

NOTES:
1. The register must be accessed in 16 bit units.
2. If the TAi register is set to 000016, the counter does not work and timer Ai interrupt requests are not generated either. Furthermore, if “pulse output” is selected, no pulses are output from the TAiOUT pin.
3. If the TAi register is set to 000016, the pulse width modulator does not work, the output level on the TAiOUT pin remains low, and timer Ai interrupt requests are not generated either. The same applies when the 8 high-order bits of the timer TAi register are set to 000016 while operating as an 8-bit pulse width modulator.
4. Use the MOV instruction to write to the TAi register.
5. The timer counts pulses from an external device or overflows or underflows in other timers.

Count Start Flag



Symbol	Address	After Reset
TABSR	038016	0016

Bit Symbol	Bit Name	Function	RW
TA0S	Timer A0 count start flag	0 : Stops counting 1 : Starts counting	RW
TA1S	Timer A1 count start flag		RW
TA2S	Timer A2 count start flag		RW
TA3S	Timer A3 count start flag		RW
TA4S	Timer A4 count start flag		RW
TB0S	Timer B0 count start flag		RW
TB1S	Timer B1 count start flag		RW
TB2S	Timer B2 count start flag		RW

Up/Down Flag (1)

Symbol	Address	After Reset
UDF	038416	0016

Bit Symbol	Bit Name	Function	RW
TA0UD	Timer A0 up/down flag	0: Down count 1: Up count Enabled by setting the MR2 bit in the TAiMR register to 0 (= switching source in UDF register) during event counter mode	RW
TA1UD	Timer A1 up/down flag		RW
TA2UD	Timer A2 up/down flag		RW
TA3UD	Timer A3 up/down flag		RW
TA4UD	Timer A4 up/down flag		RW
TA2P	Timer A2 two-phase pulse signal processing select bit	0: two-phase pulse signal processing disabled 1: two-phase pulse signal processing enabled (2, 3)	WO
TA3P	Timer A3 two-phase pulse signal processing select bit		WO
TA4P	Timer A4 two-phase pulse signal processing select bit		WO

NOTES:
1. Use MOV instruction to write to this register.
2. Make sure the port direction bits for the TA2IN to TA4IN and TA2OUT to TA4OUT pins are set to 0 input mode.
3. When the two-phase pulse signal processing function is not used, set the corresponding bit to 0.

Figure 12.5 TA0 to TA4 Registers, TABSR Register, and UDF Register

12.2.2 Event Counter Mode

In event counter mode, the timer counts pulses from an external device or overflows and underflows of other timers (see **Table 12.7**). **Figure 12.19** shows the TBiMR register in event counter mode.

Table 12.7 Specifications in Event Counter Mode

Item	Specification
Count source	• External signals input to TBiIN pin (i=0 to 2) (effective edge can be selected in program) • Timer Bj overflow or underflow (j=i-1, except j=2 if i=0)
Count operation	• Decrement • When the timer underflows, it reloads the reload register contents and continues counting
Divide ratio	1/(n+1) n: set value of TBi register 0000$_{16}$ to FFFF$_{16}$
Count start condition	Set TBiS bit(1) to 1 (start counting)
Count stop condition	Set TBiS bit to 0 (stop counting)
Interrupt request generation timing	Timer underflow
TBiIN pin function	Count source input
Read from timer	Count value can be read by reading TBi register
Write to timer	• When not counting and until the 1st count source is input after counting start Value written to TBi register is written to both reload register and counter • When counting (after 1st count source input) Value written to TBi register is written to only reload register (Transferred to counter when reloaded next)

NOTE:
1. Bits TB2S to TB0S are assigned to the bit 7 to bit 5 in the TABSR register.

Timer Bi Mode Register (i=0 to 2)

b7	b6	b5	b4	b3	b2	b1	b0
						0	1

Symbol	Address	After Reset
TB0MR to TB2MR	039B$_{16}$ to 039D$_{16}$	00XX0000$_2$

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 1: Event counter mode	RW
TMOD1			RW
MR0	Count polarity select bit (1)	b3 b2 0 0: Counts external signal's falling edges 0 1: Counts external signal's rising edges 1 0: Counts external signal's falling and rising edges 1 1: Do not set	RW
MR1			RW
MR2	TB0MR register Set to 0 in timer mode		RW
	TB1MR, TB2MR registers Nothing is assigned. If necessary, set to 0. When read, the content is undefined		—
MR3	When write in event counter mode, set to 0. When read in event counter mode, its content is undefined		RO
TCK0	No effect in event counter mode Can be set to 0 or 1		RW
TCK1	Event clock select	0 : Input from TBiIN pin (2) 1 : TBj overflow or underflow (j = i – 1, except j = 2 if i = 0)	RW

NOTES:
1. Effective when the TCK1 bit is set to 0 (input from TBiIN pin). If the TCK1 bit is set to 1 (TBj overflow or underflow), these bits can be set to 0 or 1.
2. The port direction bit for the TBiIN pin must be set to 0 (= input mode).

Figure 12.19 TBiMR Register in Event Counter Mode

12.3.1 Position-Data-Retain Function

This function is used to retain the position data synchronously with the three-phase waveform output.There are three position-data input pins for U, V, and W phases.

A trigger to retain the position data (hereafter, this trigger is referred to as "retain trigger") can be selected by the PDRT bit in the PDRF register. This bit selects the retain trigger to be the falling edge of each positive phase, or the rising edge of each positive phase.

12.3.1.1 Operation of the Position-data-retain Function

Figure 12.35 shows a usage example of the position-data-retain function (U phase) when the retain trigger is selected as the falling edge of the positive signal.

(1) At the falling edge of the U-phase waveform ouput, the state at pin IDU is transferred to the PDRU bit in the PDRF register.

(2) Until the next falling edge of the Uphase waveform output,the above value is retained.

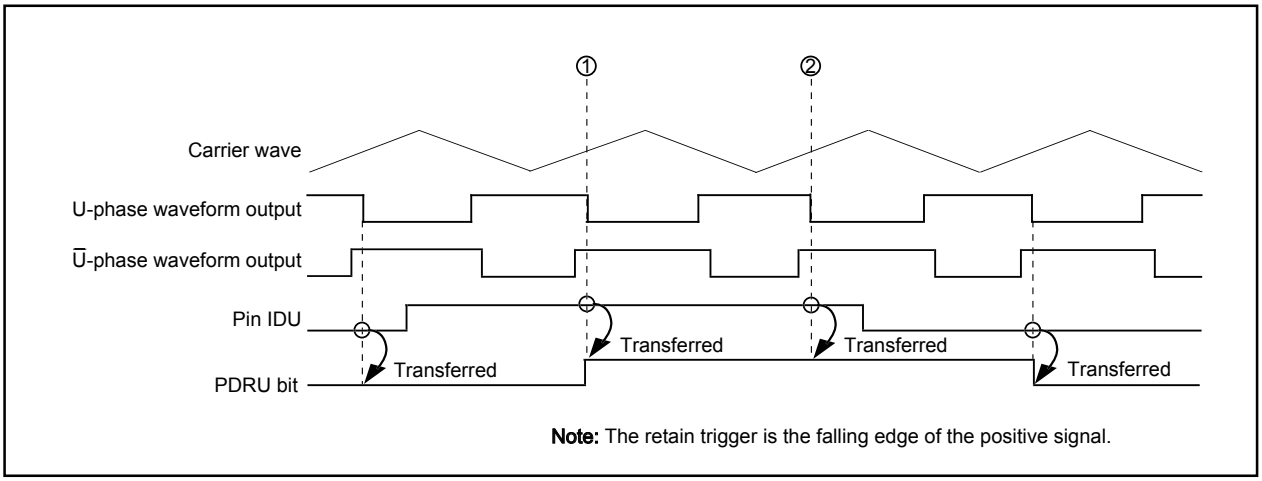
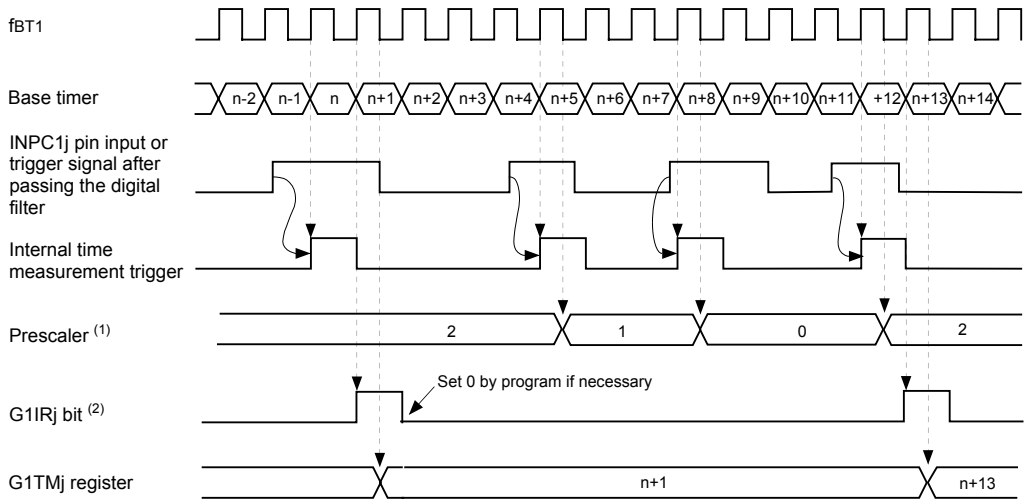


Figure 12.35 Usage Example of Position-data-retain Function (U phase)

(a) With the prescaler function

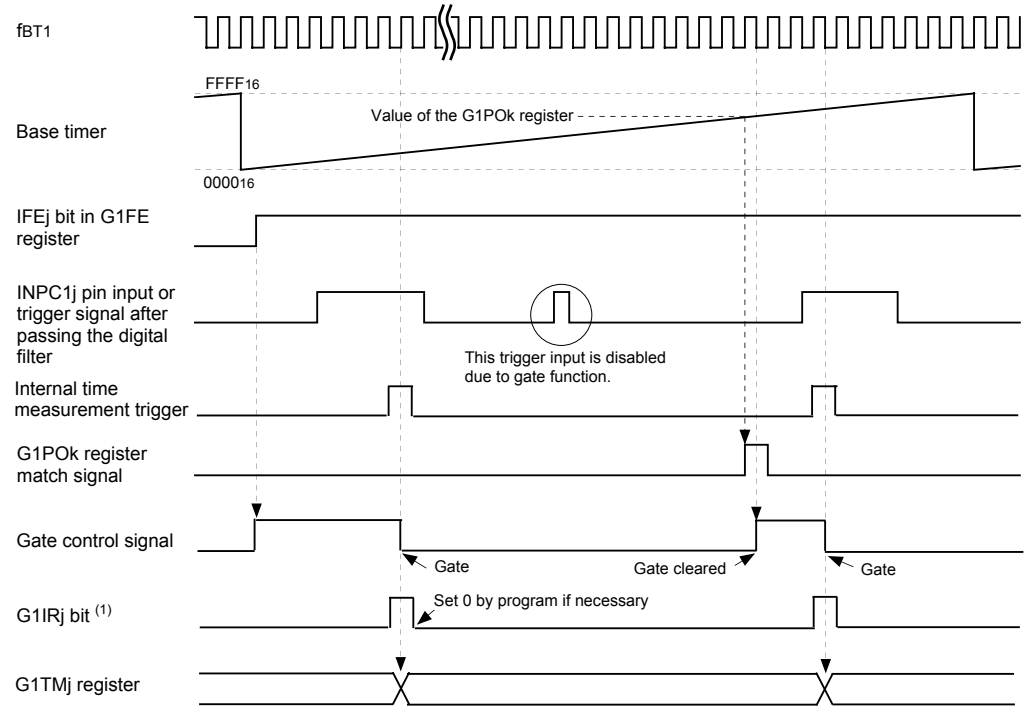
(When the G1TPRj register (j = 6, 7) is set to 02_{16}, the PR bit in the G1TMCRj register (j = 6, 7) is set to 1)



NOTES:
1. This applies to 2nd or later prescaler cycle after the PR bit in the G1TMCRj register is set to 1 (prescaler used).
2. Bits in the G1IR register.

(b) With the gate function

(The gate function is cleared by matching the base timer with the G1POk register(k = 4, 5), the GT bit in the G1TMCRj register is set to 1, the GOC bit is set to 1)



NOTE:
1. Bits in the G1IR register.

Figure 13.21 Prescaler Function and Gate Function

13.5.3 Set/Reset Waveform Output (SR Waveform Output) Mode

Output signal level of the OUTC1j pin becomes high ("H") when the INV bit in the G1POCRi (i=0 to 7) is set to 0 (output is not reversed) and the base timer value matches the G1POj register value (j=0, 2, 4, 6). The "H" signal switches to a low-level ("L") signal when the base timer value matches the G1POk (k=j+1) register value. **Table 13.10** lists specifications of SR waveform mode. **Figure 13.24** shows an example of the SR waveform mode operation.

Table 13.10 SR Waveform Output Mode Specifications

Item	Specification
Output waveform	• Free-running operation (the RST1, RTS2, and RST4 bits of the G1BCR1 and G1BCR0 registers are set to 0 (no reset)) Cycle : $\frac{65536}{f_{BT1}}$ Inverse level width(1) : $\frac{n-m}{f_{BT1}}$ • The base timer is cleared to 0000_{16} by matching the base timer with either following register (a) G1PO0 register (enabled by setting RST1 bit to 1, and bits RST4 and RST2 to 0)(2), or (b) G1BTRR register (enabled by setting RST4 bit to 1, and bits RST2 and RST1 to 0) Cycle : $\frac{p+2}{f_{BT1}}$ Inverse level width(1) : $\frac{n-m}{f_{BT1}}$ m : setting value of the G1POj register (j=0, 2, 4, 6) n : setting value of the G1POk register (k=j+1) p : setting value of the G1PO0 register or G1BTRR register value range of m, n, p: 0001_{16} to $FFFD_{16}$
Waveform output start condition	Bits IFEj and IFEk in the G1FE register is set to 1 (channel j function enabled)
Waveform output stop condition	Bits IFEj and IFEk are set to 0 (channel j function disabled)
Interrupt request	The G1IRj bit in the G1IR register is set to 1 when the base timer value matches the G1POj register value. The G1IRk bit in the interrupt request register is set to 1 when the base timer value matches the G1POk register value (See **Figure 13.24**)
OUTC1j pin (3)	Pulse signal output pin
Selectable function	• Default value set function : Set starting waveform output level • Inverse output function: Waveform output signal is inversed and provided from the OUTC1j pin

NOTES:
1. The odd channel's waveform generating register must have greater value than the even channel's.
2. When the G1PO0 register resets the base timer, the channel 0 and channel 1 SR waveform generating functions are not available.
3. Pins $OUTC1_0$, $OUTC1_2$, OUTC14, $OUTC1_6$.

UARTi Transmit/receive Mode Register (i=0, 1)

b7	b6	b5	b4	b3	b2	b1	b0
0							

Symbol	Address	After Reset
U0MR, U1MR	$03A0_{16}$, $03A8_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
SMD0	Serial I/O mode select bit (2)	b2 b1 b0 0 0 0 : Serial I/O disabled 0 0 1 : Clock synchronous serial I/O mode 1 0 0 : UART mode transfer data 7 bit long 1 0 1 : UART mode transfer data 8 bit long 1 1 0 : UART mode transfer data 9 bit long Do not set the value other than the above	RW
SMD1			RW
SMD2			RW
CKDIR	Internal/external clock select bit	0 : Internal clock 1 : External clock (1)	RW
STPS	Stop bit length select bit	0 : One stop bit 1 : Two stop bits	RW
PRY	Odd/even parity select bit	Effective when PRYE = 1 0 : Odd parity 1 : Even parity	RW
PRYE	Parity enable bit	0 : Parity disabled 1 : Parity enabled	RW
$\overline{\text{(b7)}}$	Reserve bit	Set to 0	RW

NOTES:
1. Set the corresponding port direction bit for each CLKi pin to 0 (input mode).
2. To receive data, set the corresponding port direction bit for each RxDi pin to 0.

UART2 Transmit/receive Mode Register

b7	b6	b5	b4	b3	b2	b1	b0

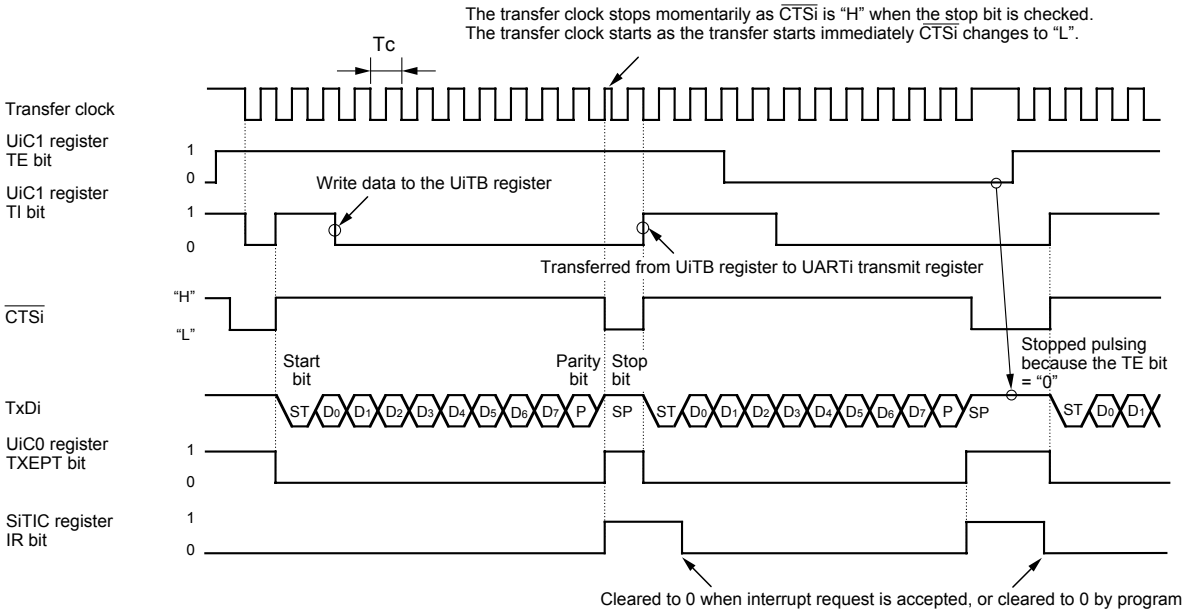
Symbol	Address	After Reset
U2MR	0378_{16}	00_{16}

Bit Symbol	Bit Name	Function	RW
SMD0	Serial I/O mode select bit (2)	b2 b1 b0 0 0 0 : Serial I/O disabled 0 0 1 : Clock synchronous serial I/O mode 0 1 0 : I^2C bus mode(3) 1 0 0 : UART mode transfer data 7 bit long 1 0 1 : UART mode transfer data 8 bit long 1 1 0 : UART mode transfer data 9 bits long Do not set the value other than the above	RW
SMD1			RW
SMD2			RW
CKDIR	Internal/external clock select bit	0 : Internal clock 1 : External clock (1)	RW
STPS	Stop bit length select bit	0 : One stop bit 1 : Two stop bits	RW
PRY	Odd/even parity select bit	Effective when PRYE = 1 0 : Odd parity 1 : Even parity	RW
PRYE	Parity enable bit	0 : Parity disabled 1 : Parity enabled	RW
IOPOL	TxD, RxD I/O polarity reverse bit	0 : No reverse 1 : Reverse	RW

NOTES:
1. Set the corresponding port direction bit for each CLK2 pin to 0 (input mode).
2. To receive data, set the corresponding port direction bit for each RxD2 pin to 0 (input mode).
3. Set the corresponding port direction bit for SCL_2 and SDA_2 pins to 0 (input mode).

Figure 14.5 U0MR to U2MR Registers

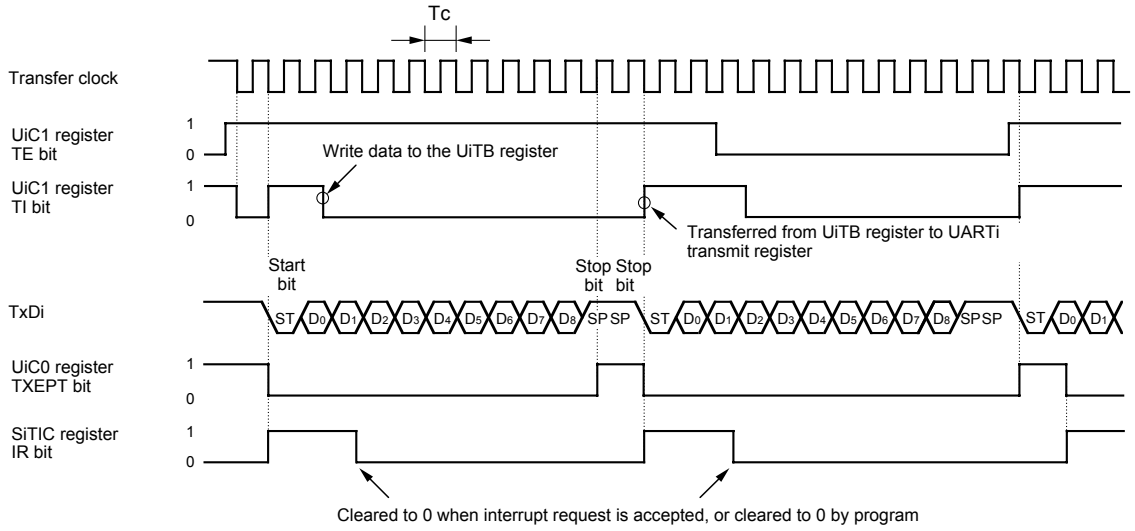
• Example of transmit timing when transfer data is 8-bit long (parity enabled, one stop bit)



The above timing diagram applies to the case where the register bits are set as follows:
- Set the PRYE bit in the UiMR register to 1 (parity enabled)
- Set the STPS bit in the UiMR register to 0 (1 stop bit)
- Set the CRD bit in the UiC0 register to 0 (CTS/RTS enabled), the CRS bit to 0 (CTS selected).
- Set the UiIRS bit to 1 (an interrupt request occurs when transmit completed):
  U0IRS bit is the UCON register bit 0, U1IRS bit is the UCON register bit 1, and U2IRS bit is the U2C1 register bit 4

Tc = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: frequency of UiBRG count source (f1SIO, f2SIO, f8SIO, f32SIO)
fEXT: frequency of UiBRG count source (external clock)
n: value set to UiBRG
i = 0 to 2

• Example of transmit timing when transfer data is 9-bit long (parity disabled, two stop bits)



The above timing diagram applies to the case where the register bits are set as follows:
- Set the PRYE bit in the UiMR register to 0 (parity disabled)
- Set the STPS bit in the UiMR register to 1 (2 stop bits)
- Set the CRD bit in the UiC0 register to 1 (CTS/RTS disabled)
- Set the UiIRS bit to 0 (an interrupt request occurs when transmit buffer becomes empty):
  U0IRS bit is the UCON register bit 0, U1IRS bit is the UCON register bit 1, and U2IRS bit is the U2C1 register bit 4

Tc = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: frequency of UiBRG count source (f1SIO, f2SIO, f8SIO, f32SIO)
fEXT: frequency of UiBRG count source (external clock)
n: value set to UiBRG
i = 0 to 2

Figure 14.16 Typical transmit timing in UART mode (UART0, UART1)

A/D Trigger Control Register (1)

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	0	0	1	1

Symbol	Address	After Reset
ADTRGCON	$03D2_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
SSE	A/D operation mode select bit 2	Simultaneous sample sweep mode or delayed trigger mode 0, 1	RW
DTE	A/D operation mode select bit 3	Delayed trigger mode 0, 1	RW
HPTRG0	AN0 trigger select bit	See **Table 15.13**	RW
HPTRG1	AN1 trigger select bit	See **Table 15.13**	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—

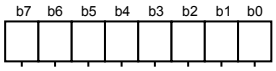
NOTE:
1. If ADTRGCON is rewritten during A/D conversion, the conversion result will be undefined.

Figure 15.28 ADTRGCON Register in Delayed Trigger Mode 1

Table 15.13 Trigger Select Bit Setting in Delayed Trigger Mode 1

TRG	TRG1	HPTRG0	HPTRG1	Trigger
0	1	0	0	$\overline{\text{AD}}_{\text{TRG}}$

Pull-up Control Register 0 (1)

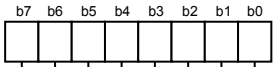


Symbol	Address	After Reset
PUR0	03FC16	0016

Bit Symbol	Bit Name	Function	RW
PU00	P00 to P03 pull-up	0: Not pulled up 1: Pulled up (1)	RW
PU01	P04 to P07 pull-up		RW
PU02	P10 to P13 pull-up		RW
PU03	P14 to P17 pull-up		RW
PU04	P20 to P23 pull-up		RW
PU05	P24 to P27 pull-up		RW
PU06	P30 to P33 pull-up		RW
PU07	P34 to P37 pull-up		RW

NOTE:
1. The pin for which this bit is 1 (pulled up) and the direction bit is 0 (input mode) is pulled up.

Pull-up Control Register 1

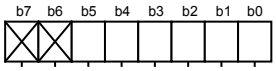


Symbol	Address	After Reset
PUR1	03FD16	0016

Bit Symbol	Bit Name	Function	RW
—— (b3-b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—
PU14	P60 to P63 pull-up	0: Not pulled high 1: Pulled high (1)	RW
PU15	P64 to P67 pull-up		RW
PU16	P70 to P73 pull-up		RW
PU17	P74 to P77 pull-up		RW

NOTE:
1. The pin for which this bit is 1 (pulled up) and the direction bit is 0 (input mode) is pulled up.

Pull-up Control Register 2

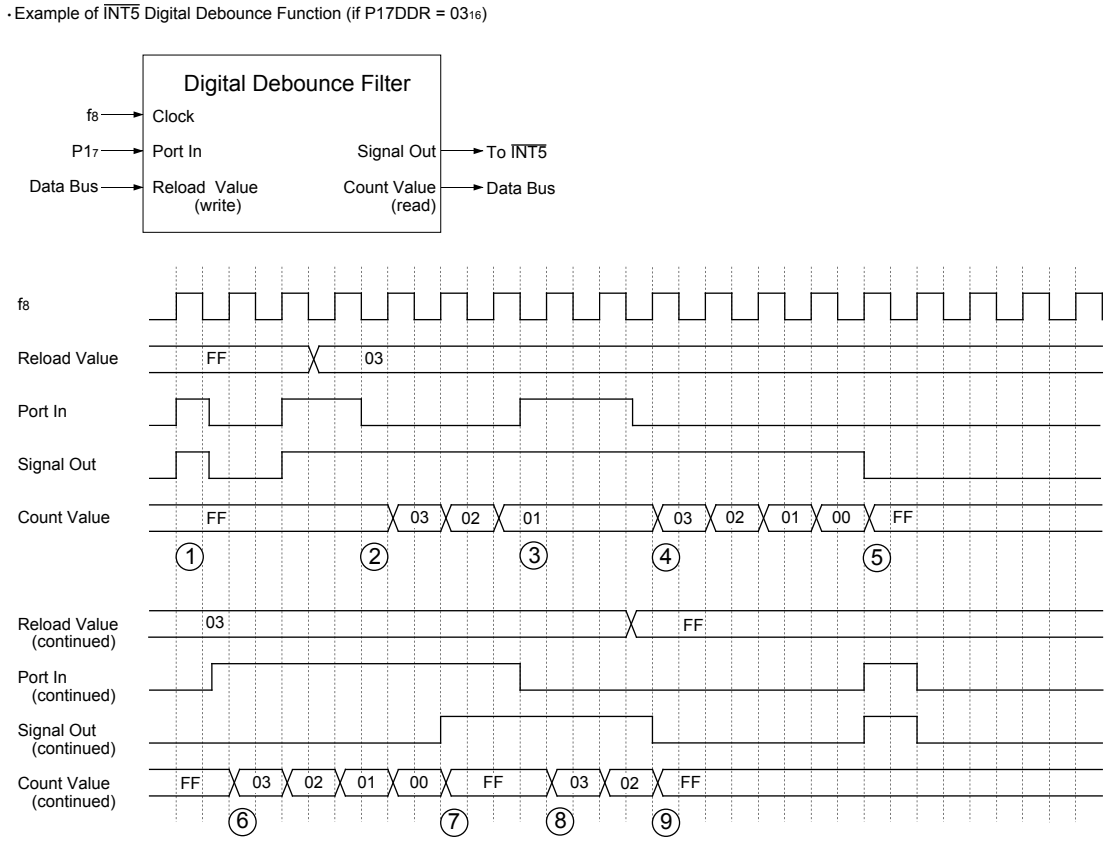


Symbol	Address	After Reset
PUR2	03FE16	0016

Bit Symbol	Bit Name	Function	RW
PU20	P80 to P83 pull-up	0: Not pulled up 1: Pulled up (1)	RW
PU21	P84 to P87 pull-up		RW
PU22	P90 to P93 pull-up		RW
PU23	P95 to P97 pull-up		RW
PU24	P100 to P103 pull-up		RW
PU25	P104 to P107 pull-up		RW
—— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—

NOTE:
1. The pin for which this bit is 1 (pulled up) and the direction bit is 0 (input mode) is pulled up.

Figure 19.8 PUR0 to PUR2 Registers



1. (Condition after reset). P17DDR=FF16. Pin input signal will be output directly.
2. Set the P17DDR register to 0316. The P17DDR register starts decrement along the f8 as a counter source, if the pin input level (e.g.,"L") and the signal output level (e.g.,"H") are not matched.
3. The P17DDR register will stops counting when the pin input level and the signal output level are matched (e.g., both levels are "H") while counting.
4. If the pin input level (e.g.,"L") and the signal output level (e.g.,"H") are not matched the P17DDR register will start decrement again after the setting value is reloaded.
5. When the P17DDR register is underflow, it stops counting and the signal output will output the same as pin input level (e.g."L").
6. If the pin input level (e.g.,"H") and the signal output level (e.g., "L") are not matched again, the P17DDR register will start decrement again after the setting value is reloaded.
7. When the P17DDR register is underflow, it stops counting and the signal output will output the same as pin input level (e.g."H").
8. If the pin input level (e.g.,"H") and the signal output level (e.g., "L") are not matched again, the P17DDR register will start decrement again after the setting value is reloaded.
9. Set the P17DDR register to FF16. The P17DDR register starts counting after the setting value is reloaded. Pin input signal will be output directly.

Figure 19.12 Functioning of Digital Debounce Filter

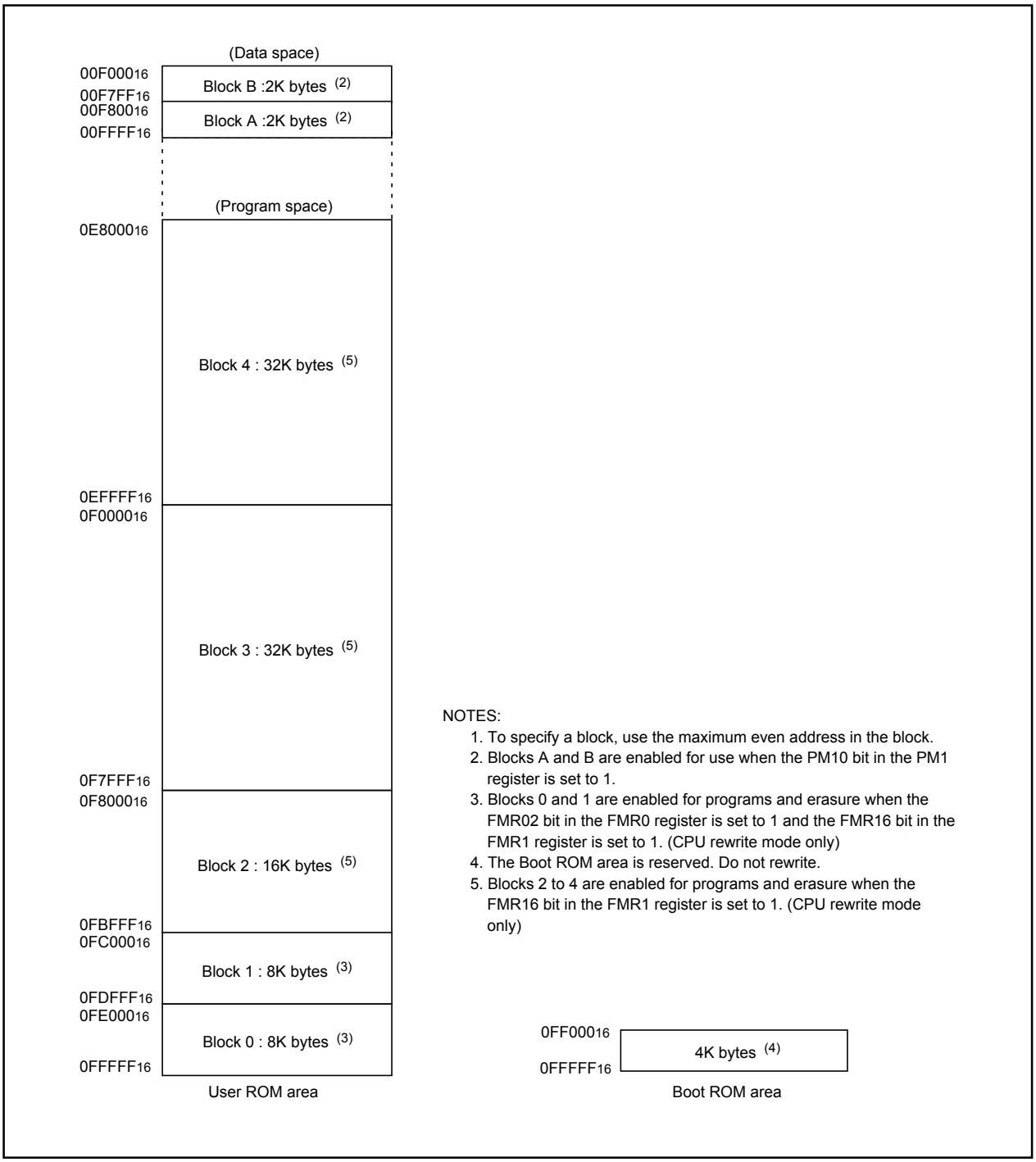
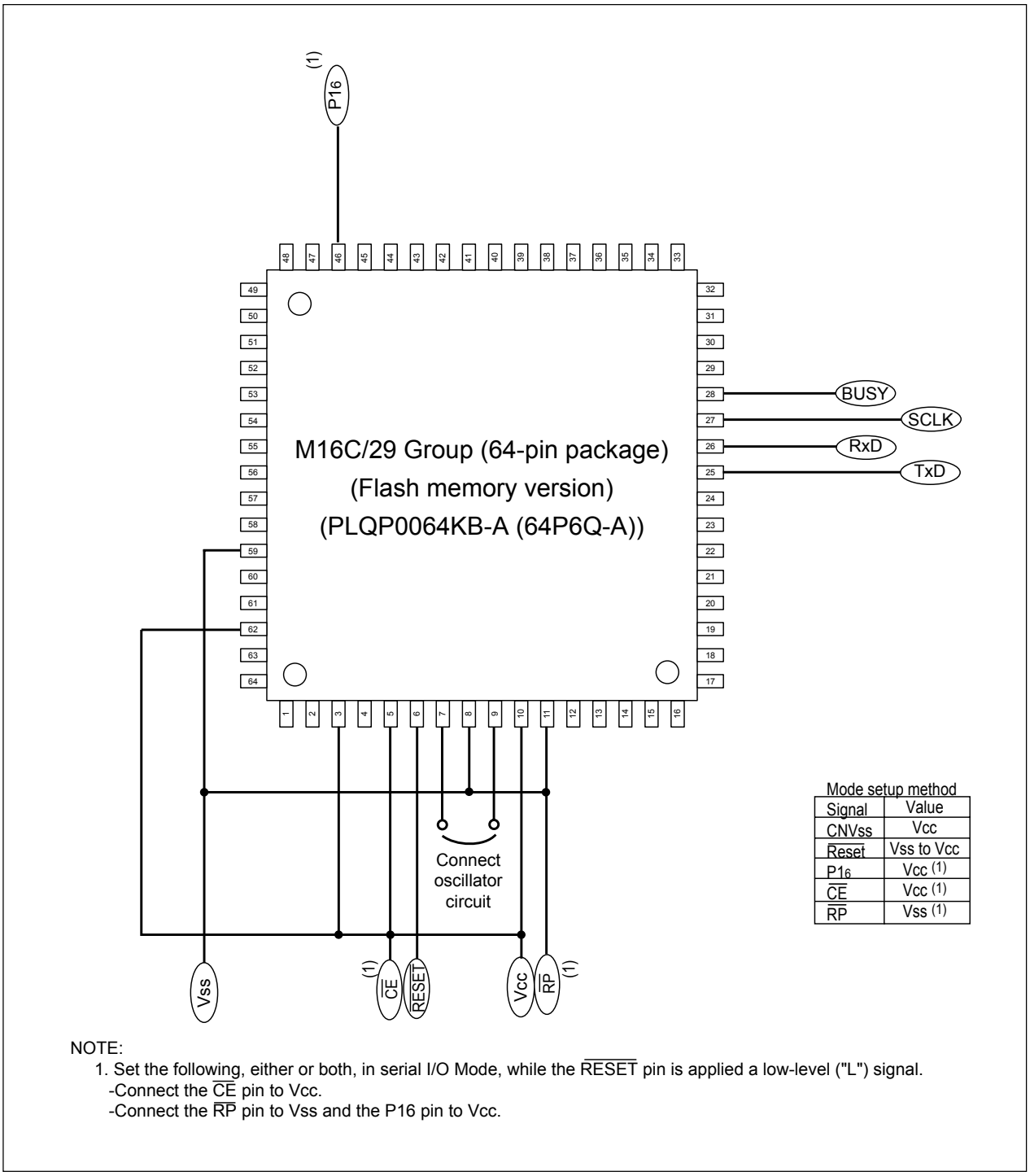


Figure 20.2 Flash Memory Block Diagram (ROM capacity 96 Kbytes)



NOTE:
1. Set the following, either or both, in serial I/O Mode, while the RESET pin is applied a low-level ("L") signal.
-Connect the CE pin to Vcc.
-Connect the RP pin to Vss and the P16 pin to Vcc.

Figure 20.15 Pin Connections for Serial I/O Mode (1)

V_{CC} = 5V

Timing Requirements

(V_{CC} = 5V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 21.11 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	100		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	40		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	40		ns

Table 21.12 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	400		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	200		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	200		ns

Table 21.13 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	200		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	100		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	100		ns

Table 21.14 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input HIGH pulse width	100		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	100		ns

Table 21.15 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input cycle time	2000		ns
$t_{w(UPH)}$	TAiOUT input HIGH pulse width	1000		ns
$t_{w(UPL)}$	TAiOUT input LOW pulse width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	400		ns

Table 21.16 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	200		ns

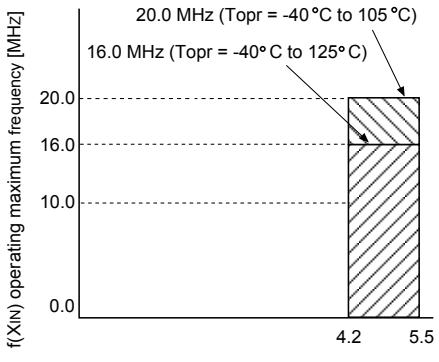
Table 21.79 Recommended Operating Conditions (1)

Symbol	Parameter			Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply Voltage			4.2		5.5	V
AVcc	Analog Supply Voltage				Vcc		V
V_{SS}	Supply Voltage				0		V
AVss	Analog Supply Voltage				0		V
V_{IH}	Input High ("H") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$		0.7 Vcc		Vcc	V
		XIN, $\overline{RESET}$, CNVSS		0.8 Vcc		Vcc	V
		SDAMM, SCLMM	When I^2C bus input level is selected	0.7 Vcc		Vcc	V
			When SMBUS input level is selected	1.4		Vcc	V
V_{IL}	Input Low ("L") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$		0		0.3Vcc	V
		XIN, $\overline{RESET}$, CNVSS		0		0.2Vcc	V
		SDAMM, SCLMM	When I^2C bus input level is selected	0		0.3Vcc	V
			When SMBUS input level is selected	0		0.6	V
$I_{OH(peak)}$	Peak Output High ("H") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$				-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$				-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$				10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$				5.0	mA
f(X_{IN})	Main Clock Input Oscillation Frequency(4)		Topr = -40 to 105 ° C	0		20	MHz
			Topr = -40 to 125 ° C	0		16	MHz
f(X_{CIN})	Sub Clock Oscillation Frequency				32.768	50	kHz
f_1(ROC)	On-chip Oscillator Frequency 1			0.5	1	2	MHz
f2(ROC)	On-chip Oscillator Frequency 2			1	2	4	MHz
f3(ROC)	On-chip Oscillator Frequency 3			8	16	26	MHz
f(PLL)	PLL Clock Oscillation Frequency(4)		Topr = -40 to 105 ° C	10		20	MHz
			Topr = -40 to 125 ° C	10		16	MHz
f(BCLK)	CPU Operation Clock Frequency		Topr = -40 to 105 ° C	0		20	MHz
			Topr = -40 to 125 ° C	0		16	MHz
t_{SU}(PLL)	Wait Time to Stabilize PLL Frequency Synthesizer		Vcc = 5.0 V			20	MHz

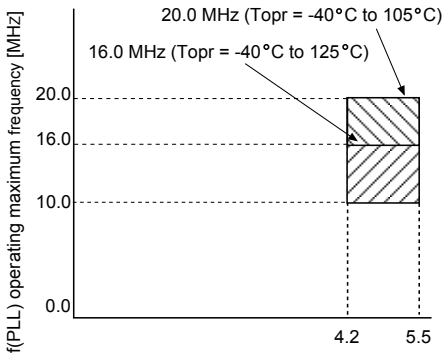
NOTES:

1. Referenced to Vcc = 4.2 to 5.5 V at Topr = -40 to 125 ° C unless otherwise specified.
2. The mean output current is the mean value within 100ms.
3. The total $I_{OL(peak)}$ for all ports must be 80 mA or less. The total $I_{OH(peak)}$ for all ports must be -80 mA or less.
4. Relationship among main clock oscillation frequency, PLL clock oscillation frequency and supply voltage.

Main clock input oscillation frequency



PLL clock oscillation frequency



22.15.14 Definition of Programming/Erasure Times

"Number of programs and erasure" refers to the number of erasure per block.
If the number of program and erasure is n (n=100 1,000 10,000) each block can be erased n times.
For example, if a 2K byte block A is erased after writing 1 word data 1024 times, each to a different address, this is counted as one program and erasure. However, data cannot be written to the same adrress more than once without erasing the block. (Rewrite prohibited)

22.15.15 Flash Memory Version Electrical Characteristics 10,000 E/W cycle products (Normal: U7, U9; T-ver./V-ver.: U7)

When Block A or B E/W cycles exceed 100, set the FMR17 bit in the FMR1 register to 1 (1 wait) to select one wait state per block access for products U7 and U9. When the FMR17 bit is set to 1, one wait state is inserted per access to Block A or B - regardless of the value of the PM17 bit. Wait state insertion during access to all other blocks, as well as to internal RAM, is controlled by the PM17 bit - regardless of the setting of the FMR17 bit.
To use the limited number of erasure efficiently, write to unused address within the block instead of rewite. Erase block only after all possible address are used. For example, an 8-word program can be written 128 times before erase becomes necessary.
Maintaining an equal number of erasure between Block A and B will also improve efficiency.
We recommend keeping track of the number of times erasure is used.

22.15.16 Boot Mode

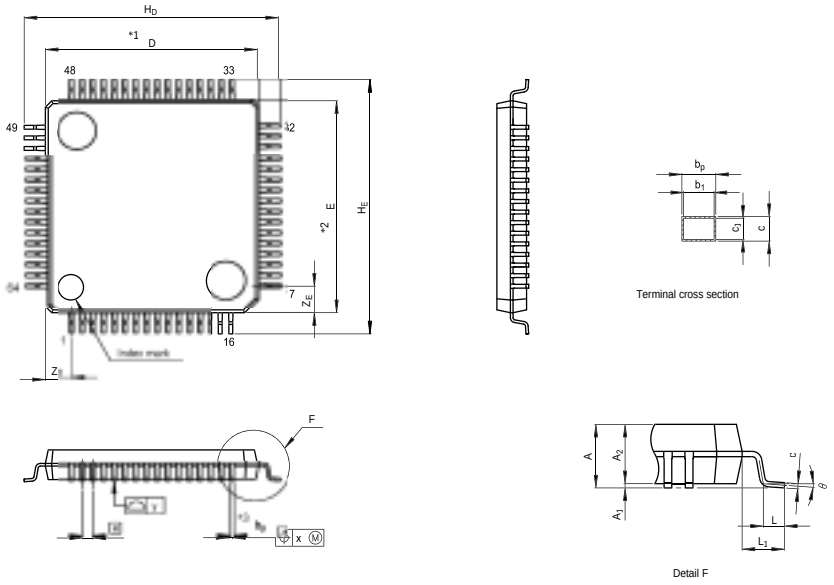
An undefined value is sometimes output in the I/O port until the internal power supply becomes stable when "H" is applied to the CNVSS pin and "L" is applied to the $\overline{\text{RESET}}$ pin.
When setting the CNVSS pin to "H", the following procedure is required:

(1) Apply an "L" signal to the $\overline{\text{RESET}}$ pin and the CNVSS pin.
(2) Bring VCC to more than 2.7V, and wait at least 2 msec. (Internal power supply stable waiting time)
(3) Apply an "H" signal to the CNVSS pin.
(4) Apply an "H" signal to the $\overline{\text{RESET}}$ pin.

When the CNVSS pin is “H” and RESET pin is “L”, P67 pin is connected to the pull-up resister.

Appendix 1. Package Dimensions

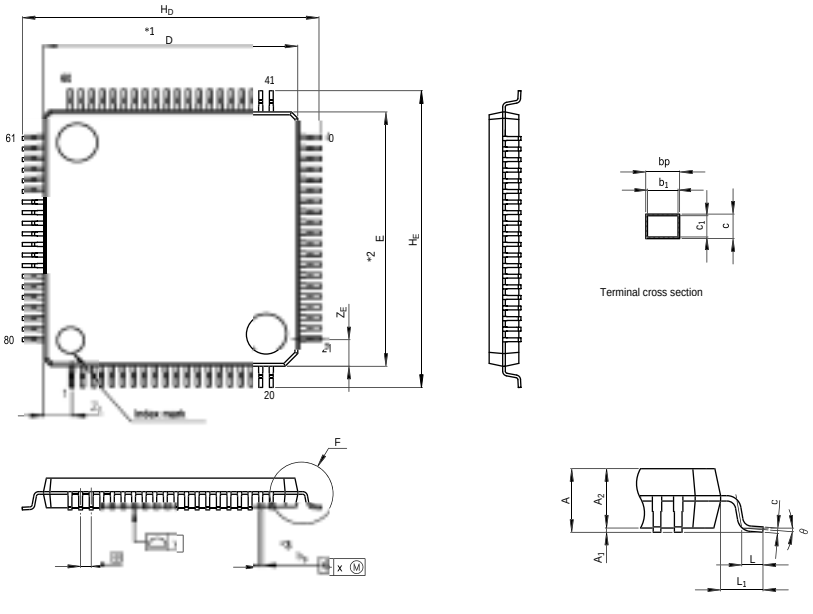
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—