Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	-
Core Size	-
Speed	-
Connectivity	-
Peripherals	-
Number of I/O	-
Program Memory Size	-
Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30291fcthp-u7a

Table 4.8 SFR Information (8)

Address	Register	Symbol	After reset
0300₁₆	Time measurement, Pulse generation register 0	G1TM0,G1PO0	XX₁₆
0301₁₆			XX₁₆
0302₁₆	Time measurement, Pulse generation register 1	G1TM1,G1PO1	XX₁₆
0303₁₆			XX₁₆
0304₁₆	Time measurement, Pulse generation register 2	G1TM2,G1PO2	XX₁₆
0305₁₆			XX₁₆
0306₁₆	Time measurement, Pulse generation register 3	G1TM3,G1PO3	XX₁₆
0307₁₆			XX₁₆
0308₁₆	Time measurement, Pulse generation register 4	G1TM4,G1PO4	XX₁₆
0309₁₆			XX₁₆
030A₁₆	Time measurement, Pulse generation register 5	G1TM5,G1PO5	XX₁₆
030B₁₆			XX₁₆
030C₁₆	Time measurement, Pulse generation register 6	G1TM6,G1PO6	XX₁₆
030D₁₆			XX₁₆
030E₁₆	Time measurement, Pulse generation register 7	G1TM7,G1PO7	XX₁₆
030F₁₆			XX₁₆
0310₁₆	Pulse generation control register 0	G1POCR0	0X00XX00₂
0311₁₆	Pulse generation control register 1	G1POCR1	0X00XX00₂
0312₁₆	Pulse generation control register 2	G1POCR2	0X00XX00₂
0313₁₆	Pulse generation control register 3	G1POCR3	0X00XX00₂
0314₁₆	Pulse generation control register 4	G1POCR4	0X00XX00₂
0315₁₆	Pulse generation control register 5	G1POCR5	0X00XX00₂
0316₁₆	Pulse generation control register 6	G1POCR6	0X00XX00₂
0317₁₆	Pulse generation control register 7	G1POCR7	0X00XX00₂
0318₁₆	Time measurement control register 0	G1TMCR0	00₁₆
0319₁₆	Time measurement control register 1	G1TMCR1	00₁₆
031A₁₆	Time measurement control register 2	G1TMCR2	00₁₆
031B₁₆	Time measurement control register 3	G1TMCR3	00₁₆
031C₁₆	Time measurement control register 4	G1TMCR4	00₁₆
031D₁₆	Time measurement control register 5	G1TMCR5	00₁₆
031E₁₆	Time measurement control register 6	G1TMCR6	00₁₆
031F₁₆	Time measurement control register 7	G1TMCR7	00₁₆
0320₁₆	Base timer register	G1BT	XX₁₆
0321₁₆			XX₁₆
0322₁₆	Base timer control register 0	G1BCR0	00₁₆
0323₁₆	Base timer control register 1	G1BCR1	00₁₆
0324₁₆	Time measurement prescale register 6	G1TPR6	00₁₆
0325₁₆	Time measurement prescale register 7	G1TPR7	00₁₆
0326₁₆	Function enable register	G1FE	00₁₆
0327₁₆	Function select register	G1FS	00₁₆
0328₁₆	Base timer reset register	G1BTRR	XX₁₆
0329₁₆			XX₁₆
032A₁₆	Count source division register	G1DV	00₁₆
032B₁₆			
032C₁₆			
032D₁₆			
032E₁₆			
032F₁₆			
0330₁₆	Interrupt request register	G1IR	XX₁₆
0331₁₆	Interrupt enable register 0	G1IE0	00₁₆
0332₁₆	Interrupt enable register 1	G1IE1	00₁₆
0333₁₆			
0334₁₆			
0335₁₆			
0336₁₆			
0337₁₆			
0338₁₆			
0339₁₆			
033A₁₆			
033B₁₆			
033C₁₆			
033D₁₆			
033E₁₆	NMI digital debounce register	NDDR	FF₁₆
033F₁₆	Port P17 digital debounce register	P17DDR	FF₁₆

Note 1: The blank areas are reserved and cannot be used by users.

X : Undefined

9.3 Interrupt Control

The following describes how to enable/disable the maskable interrupts, and how to set the priority in which order they are accepted. What is explained here does not apply to nonmaskable interrupts.
Use I flag in the the FLG register, IPL, and bits ILVL2 to ILVL0 in the each interrupt control register to enable/disable the maskable interrupts. Whether an interrupt is requested is indicated by the IR bit in each interrupt control register.
Figure 9.3 shows the interrupt control registers.

Also, the following interrupts share a vector and an interrupt control register.

- $\overline{\text{INT4}}$ and SIO3
- $\overline{\text{INT5}}$ and SIO4
- A/D converter and key input interrupt
- IC/OC base timer and SCL/SDA
- IC/OC interrupt 1 and I^2C bus interface

An interrupt request is set by bits IFSR6 and IFSR7 in the IFSR register and bits IFSR27, IFSR26, and IFSR21 in the IFSR2A register. **Figure 9.4** shows registers IFSR register and IFSR2A.

Timer Ai Mode Register

b7	b6	b5	b4	b3	b2	b1	b0
		0	1		0	1	0

Symbol	Address	After Reset
TA1MR	039716	0016
TA2MR	039816	0016
TA4MR	039A16	0016

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	Set to 102 (one-shot timer mode) for the three-phase motor control timer function	RW
TMOD1			RW
MR0	Pulse output function select bit	Set to 0 for the three-phase motor control timer function	RW
MR1	External trigger select bit	No effect for the three-phase motor control timer function	RW
MR2	Trigger select bit	Set to 1 (selected by event/trigger select register) for the three-phase motor control timer function	RW
MR3	Set to 0 for the three-phase motor control timer function		RW
TCK0	Count source select bit	b7 b6 0 0 : f1 or f2 0 1 : f8 1 0 : f32 1 1 : fC32	RW
TCK1			RW

Timer B2 Mode Register

b7	b6	b5	b4	b3	b2	b1	b0
			0			0	0

Symbol	Address	After Reset
TB2MR	039D16	00XX00002

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	Set to 002 (timer mode) for the three-phase motor control timer function	RW
TMOD1			RW
MR0	No effect for the three-phase motor control timer function. If necessary, set to 0. When read, the contents are undefined		RW
MR1			RW
MR2	Set to 0 for the three-phase motor control timer function		RW
MR3	When write in three-phase motor control timer function, write 0. When read, the content is undefined		RO
TCK0	Count source select bit	b7 b6 0 0: f1 or f2 0 1: f8 1 0: f32 1 1: fC32	RW
TCK1			RW

Figure 12.32 TA1MR, TA2MR, TA4MR, and TB2MR Registers

Figure 13.1 shows the block diagram of the IC/OC.

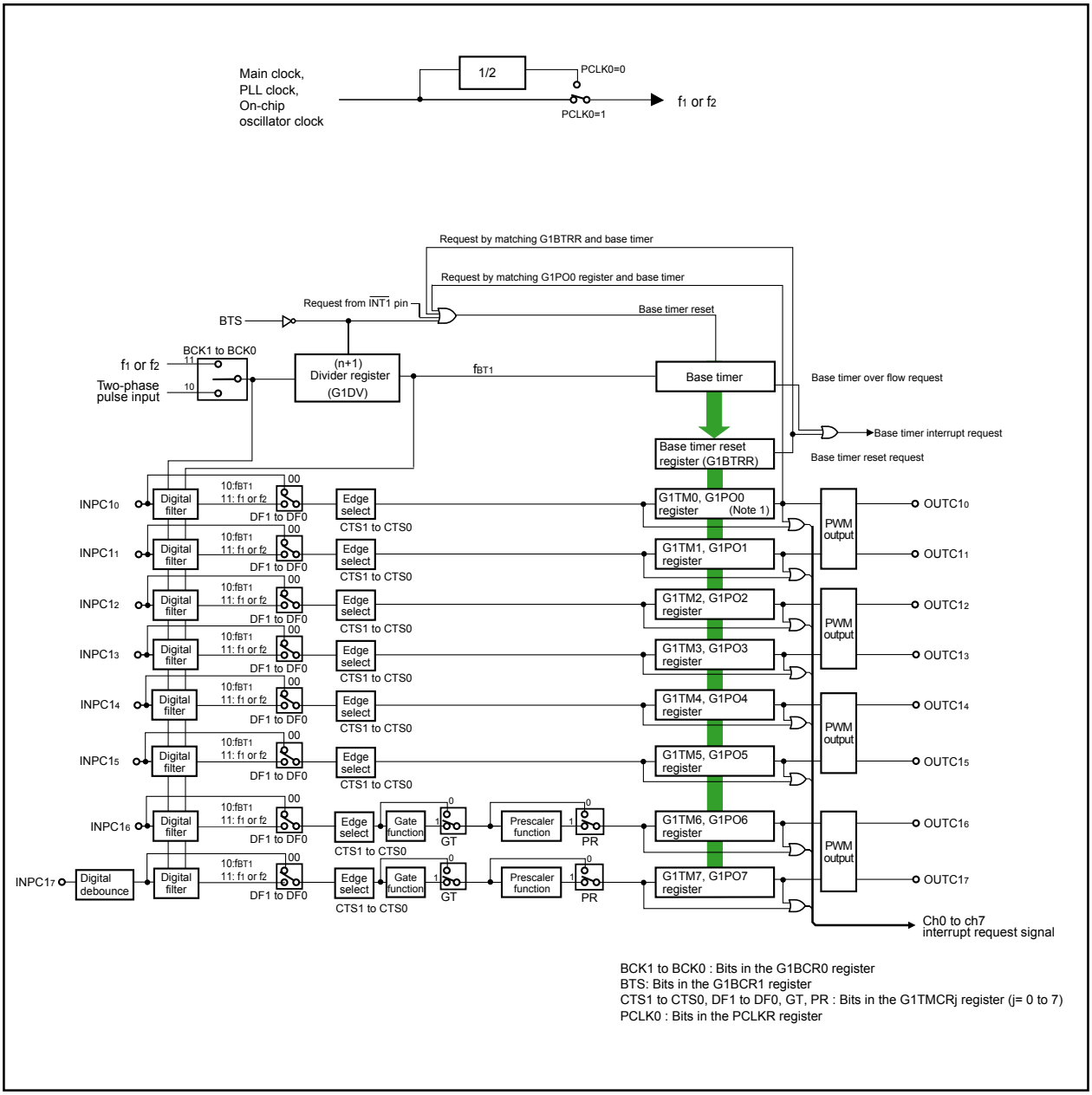
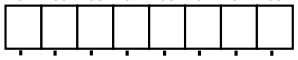


Figure 13.1 IC/OC Block Diagram

Interrupt Request Register (1)



Symbol	Address	After Reset
G1IR	0330_{16}	Undefined

Bit Symbol	Bit Name	Function	RW
G1IR0	Interrupt request, Ch0	0 : No interrupt request 1 : Interrupt requested	RW
G1IR1	Interrupt request, Ch1		RW
G1IR2	Interrupt request, Ch2		RW
G1IR3	Interrupt request, Ch3		RW
G1IR4	Interrupt request, Ch4		RW
G1IR5	Interrupt request, Ch5		RW
G1IR6	Interrupt request, Ch6		RW
G1IR7	Interrupt request, Ch7		RW

NOTE:
1. When writing 0 to each bit in the G1IR register, use the following instruction:
AND, BCLR

Figure 13.9 G1IR Register

14. Serial I/O

Note

The SI/O4 interrupt of peripheral function interrupt is not available in the 64-pin package.

Serial I/O is configured with five channels: UART0 to UART2, SI/O3 and SI/O4.

14.1 UARTi (i=0 to 2)

UARTi each have an exclusive timer to generate a transfer clock, so they operate independently of each other.

Figure 14.1 shows the block diagram of UARTi. **Figures 14.2** and **14.3** shows the block diagram of the UARTi transmit/receive.

UARTi has the following modes:

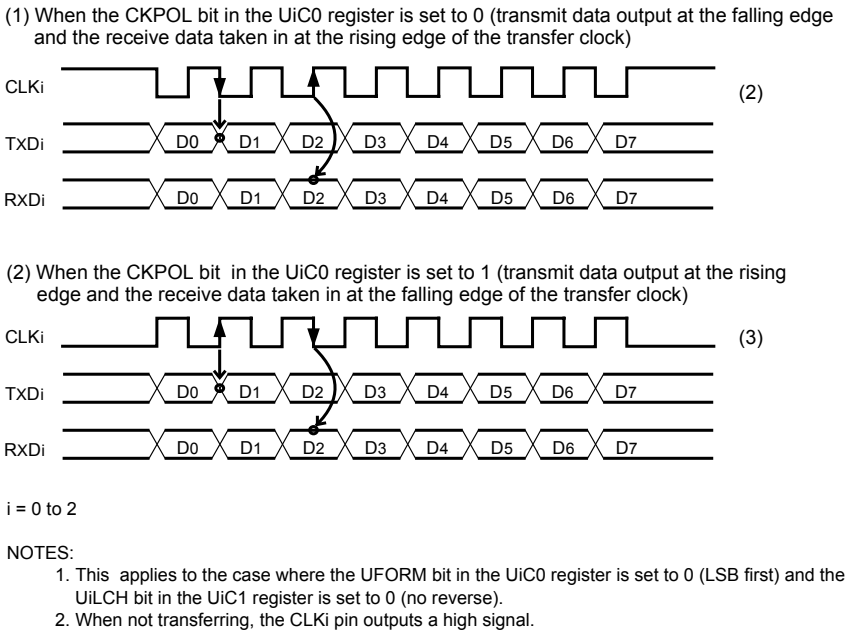
- Clock synchronous serial I/O mode
- Clock asynchronous serial I/O mode (UART mode).
- Special mode 1 (I^2C bus mode): UART2
- Special mode 2: UART2
- Special mode 3 (Bus collision detection function, IEBus mode): UART2
- Special mode 4 (SIM mode): UART2

Figures 14.4 to **14.9** show the UARTi-related registers.

Refer to tables listing each mode for register setting.

14.1.1.2 CLK Polarity Select Function

Use the CKPOL bit in the UiC0 register (i=0 to 2) to select the transfer clock polarity. **Figure 14.11** shows the polarity of the transfer clock.



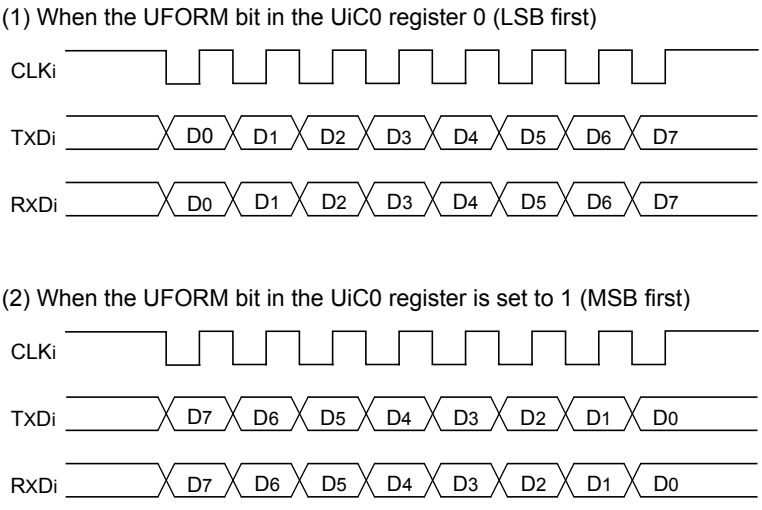
i = 0 to 2

NOTES:
1. This applies to the case where the UFORM bit in the UiC0 register is set to 0 (LSB first) and the UiLCH bit in the UiC1 register is set to 0 (no reverse).
2. When not transferring, the CLKi pin outputs a high signal.

Figure 14.11 Polarity of transfer clock

14.1.1.3 LSB First/MSB First Select Function

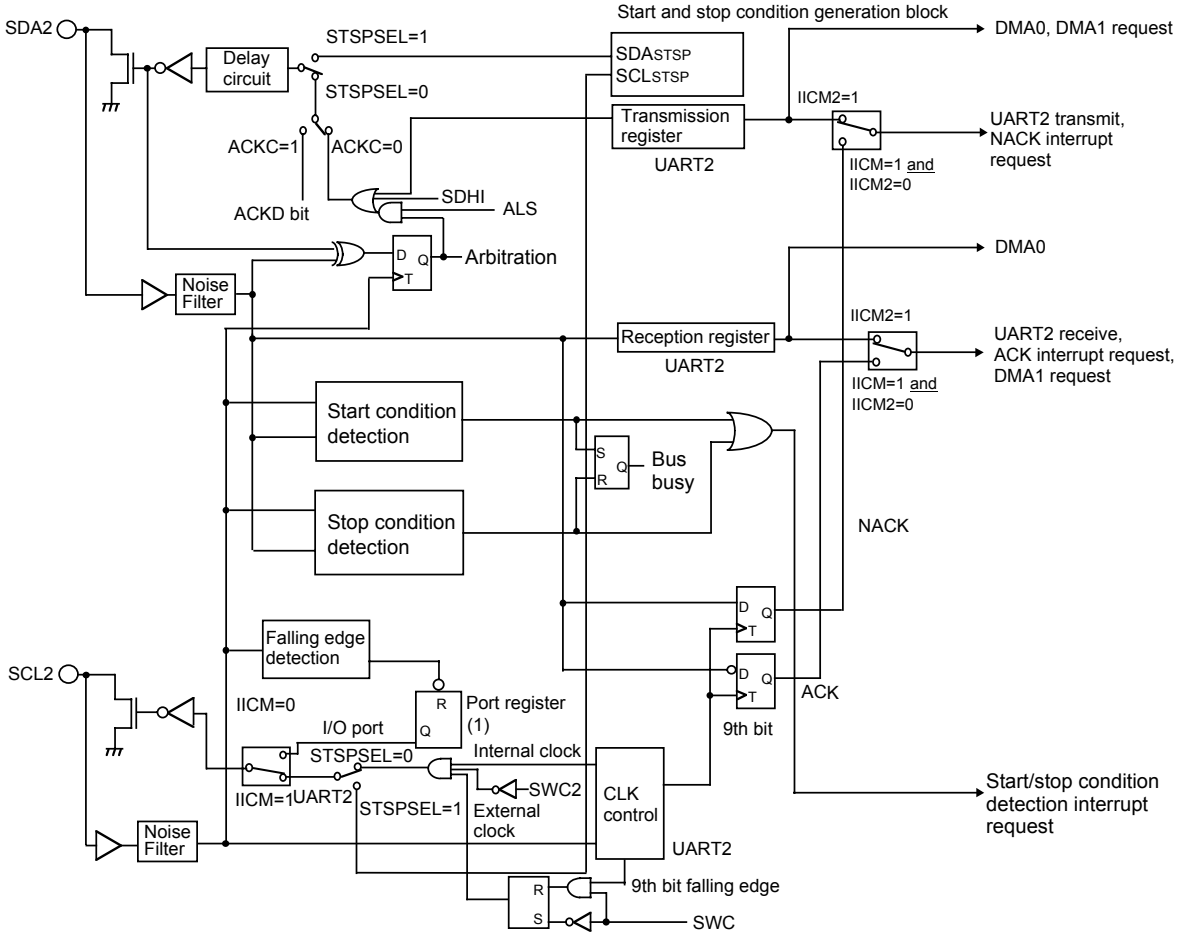
Use the UFORM bit in the UiC0 register (i=0 to 2) to select the transfer format. **Figure 14.12** shows the transfer format.



i = 0 to 2

NOTE:
1. This applies to the case where the CKPOL bit in the UiC0 register is set to 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transfer clock) and the UiLCH bit in the UiC1 register 0 (no reverse).

Figure 14.12 Transfer format



This diagram applies to the case where bits SMD2 to SMD0 in the U2MR register is set to 010$_2$ and the IICM bit in the U2SMR register is set to 1.

IICM: Bit in the U2SMR register
IICM2, SWC, ALS, SWC2, SDHI: Bits in the U2SMR2 register
STSPSEL, ACKD, ACKC: Bits in the U2SMR4 register

NOTE:
1. If the IICM bit is set to 1, the pin can be read even when the PD7_1 bit is set to 1 (output mode).

Figure 14.22 I^{2}C bus mode Block Diagram

14.1.6.2 Format

• Direct Format

Set the PRY bit in the U2MR register to 1, the UFORM bit in U2C0 register to 0 and the U2LCH bit in U2C1 register to 0.

• Inverse Format

Set the PRY bit to 0, UFORM bit to 1 and U2LCH bit to 1.

Figure 14.34 shows the SIM interface format.

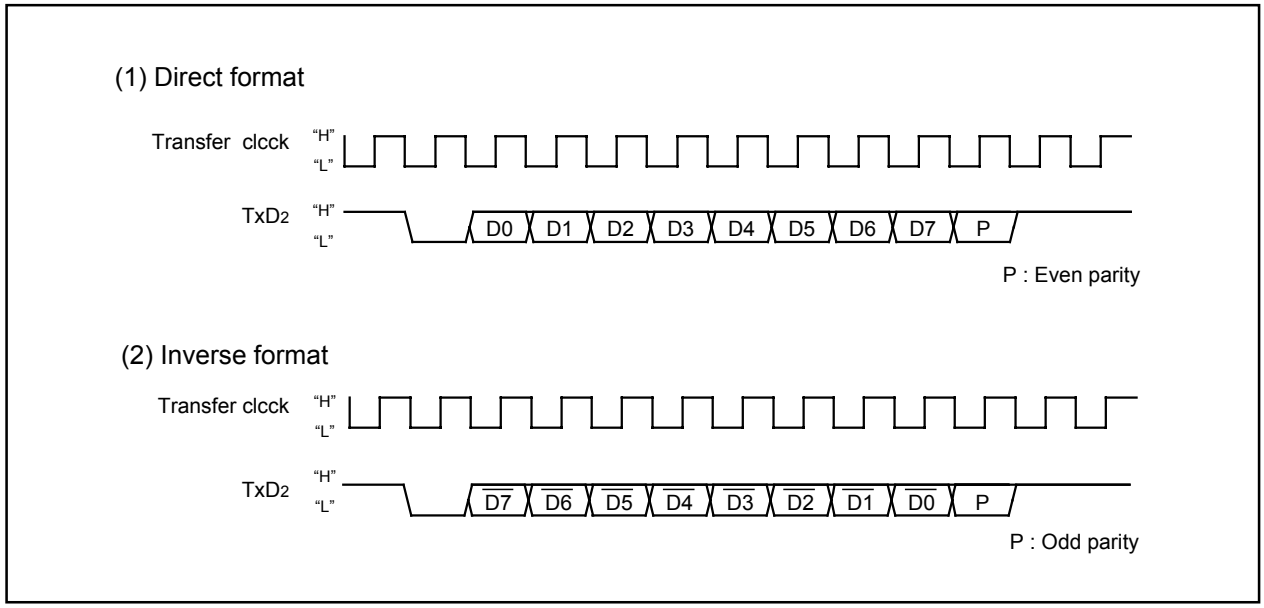


Figure 14.34 SIM Interface Format

I2C0 Data Shift Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
S00	02E016	XX16

Function	RW
Transmit/receive data are stored. In master transmit mode, the start condition/stop condition are triggered by writing data to the register (refer to **16.9 START Condition Generation Method** and **16.11 STOP Condition Generation Method**). Start transmitting/receiving data while synchronizing with SCL	RW(1)

NOTE:
1. Write is enabled only when the ES0 bit in the S1D0 register is 1 (I2C bus interface is enabled). Write the transmit data after the receive data is read because the S00 register is used to store both the transmit and receive data. When the S00 register is set, bits BC2 to BC0 in the S1D0 register are set to 000_2, while bits LRB, AAS, and AL in the S10 register are set to 0 respectively.

I2C0 Clock Control Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
S20	02E416	0016

Bit Symbol	Bit Name	Function	RW
CCR0	SCL Frequency Control Bits	See **Table 16.3**	RW
CCR1			RW
CCR2			RW
CCR3			RW
CCR4			RW
FAST MODE	SCL Mode Specification Bit	0: Standard clock mode 1: High-speed clock mode	RW
ACKBIT	ACK Bit	0: ACK is returned 1: ACK is not returned	RW
ACK-CLK	ACK Clock Bit	0: No ACK clock 1: With ACK clock	RW

Figure 16.3 S00 and S20 Registers

16.4 I2C0 Control Register 0 (S1D0)

The S1D0 register controls data communication format.

16.4.1 Bits 0 to 2: Bit Counter (BC0–BC2)

Bits BC2 to BC0 decide how many bits are in one byte data transferred next. After the selected numbers of bits are transferred successfully, I2C bus interface interrupt request is gnerated and bits BC2 to BC0 are reset to 0002. At this time, if the ACK-CLK bit in the S20 register is set to 1 (with ACK clock), one bit for ACK clock is added to the numbers of bits selected by the BC2 to BC0 bits.

In addition, bits BC2 to BC0 become 0002 even though the START condition is detected and the address data is transferred in 8 bits.

16.4.2 Bit 3: I2C Interface Enable Bit (ES0)

The ES0 bit enables to use the multi-master I2C bus interface. When the ES0 bit is set to 0, I2C bus interface is disabled and the SDA and SCL pins are placed in a high-h-impedance state. When the ES0 bit is set to 1, the interface is enabled.

When the ES0 bit is set to 0, the process is followed.

1)The bits in the S10 register are set as MST = 0, TRX = 0, PIN = 1, BB = 0, AL = 0, AAS = 0, ADR0 = 0

2)The S00 register cannot be written.

3)The TOF bit in the S4D0 register is set to 0 (time-out detection flag is not detected)

4)The I2C system clock (VIIC) stops counting while the internal counter and flags are reset.

16.4.3 Bit 4: Data Format Select Bit (ALS)

The ALS bit determines whether the salve address is recognized. When the ALS bit is set to 0, an addressing format is selected and a address data is recognized. Only if the comparison is matched between the slave address stored into the S0D0 register and the received address data or if the general call is received, the data is transferred. When the ALS bit is set to 1, the free data format is selected and the slave address is not recognized.

16.4.4 Bit 6: I2C bus Interface Reset Bit (IHR)

The IHR bit is used to reset the I2C bus interface circuit when the error communication occurs.

When the ES0 bit in the S1D0 register is set to 1 (I2C bus interface is enabled), the hardware is reset by writing 1 to the IHR bit. Flags are processed as follows:

1)The bits in the S10 register are set as MST = 0, TRX = 0, PIN to 1, BB = 0, AL = 0, AAS = 0, and ADR0 = 0

2)The TOF bit in the S4D0 register is set to 0 (time-out detection flag is not detected)

3)The internal counter and flags are reset.

The I2C bus interface circuit is reset after 2.5 VIIC cycles or less, and the IHR bit becomes 0 automatically by writing 1 to the IHR bit. **Figure 16.10** shows the reset timing.

16.5.7 Bit 6: Communication Mode Select Bit (Transfer Direction Select Bit: TRX)

This TRX bit decides a transfer direction for data communication. When the TRX bit is set to 0, receive mode is entered and data is received from a transmit device. When the TRX bit is set to 1, transmit mode is entered, and address data and control data are output to the SDAMM, synchronized with a clock generated in the SCLMM.

The TRX bit is set to 1 automatically in the following condition:

- In slave mode, when the ALS in the S1D0 register to 0(addressing format), the AAS flag is set to 1 (address match) after the address data is received, and the received R/$\overline{W}$ bit is set to 1

The TRX bit is set to 0 in one of the following conditions:

- When an arbitration lost is detected
- When a STOP condition is detected
- When a START condition is detected
- When a START condition is disabled by the START condition duplicate protect function (1)
- When the MST bit in the S10 register is set to 0(slave mode) and a start condition is detected
- When the MST bit is set to 0 and the ACK non-return is detected
- When the ES0 bit is set to 0(I2C bus interface disabled)
- When the IHR bit in the S1D0 register is set to 1(reset)

16.5.8 Bit 7: Communication mode select bit (master/slave select bit: MST)

The MST bit selects either master mode or slave mode for data communication. When the MST bit is set to 0, slave mode is entered and the START/STOP condition generated by a master device are received. The data communication is synchronized with the clock generted by the master. When the MST bit is set to 1, master mode is entered and the START/STOP condition is generated.

Additionally, clocks required for the data communication are generated on the SCLMM.

The MST bit is set to 0 in one of the following conditions.

- After 1-byte data of a master whose arbtration is lost if arbitration lost is detected
- When a STOP condition is detected
- When a START condition is detected
- When a start condition is disabled by the START condition duplicate protect function (1)
- When the IHR bit in the S1D0 register is set to 1(reset)
- When the ES0 bit is set to 0(I2C bus interface disabled)

NOTE:

1. START condition duplicate protect function:
   When the START condition is generated, after confirming that the BB flag in the S1D0 register is set to 0 (bus free), all the MST, TRX and BB flags are set to 1 at the same time. However, if the BB flag is set to 1 immediately after the BB flag setting is confirmed because a START condition is generated by other master device, bits MST and TRX cannot be written. The duplicate protect function is valid from the rising edge of the BB flag until slave address is received. Refer to **16.9 START Condition Generation Method** for details.

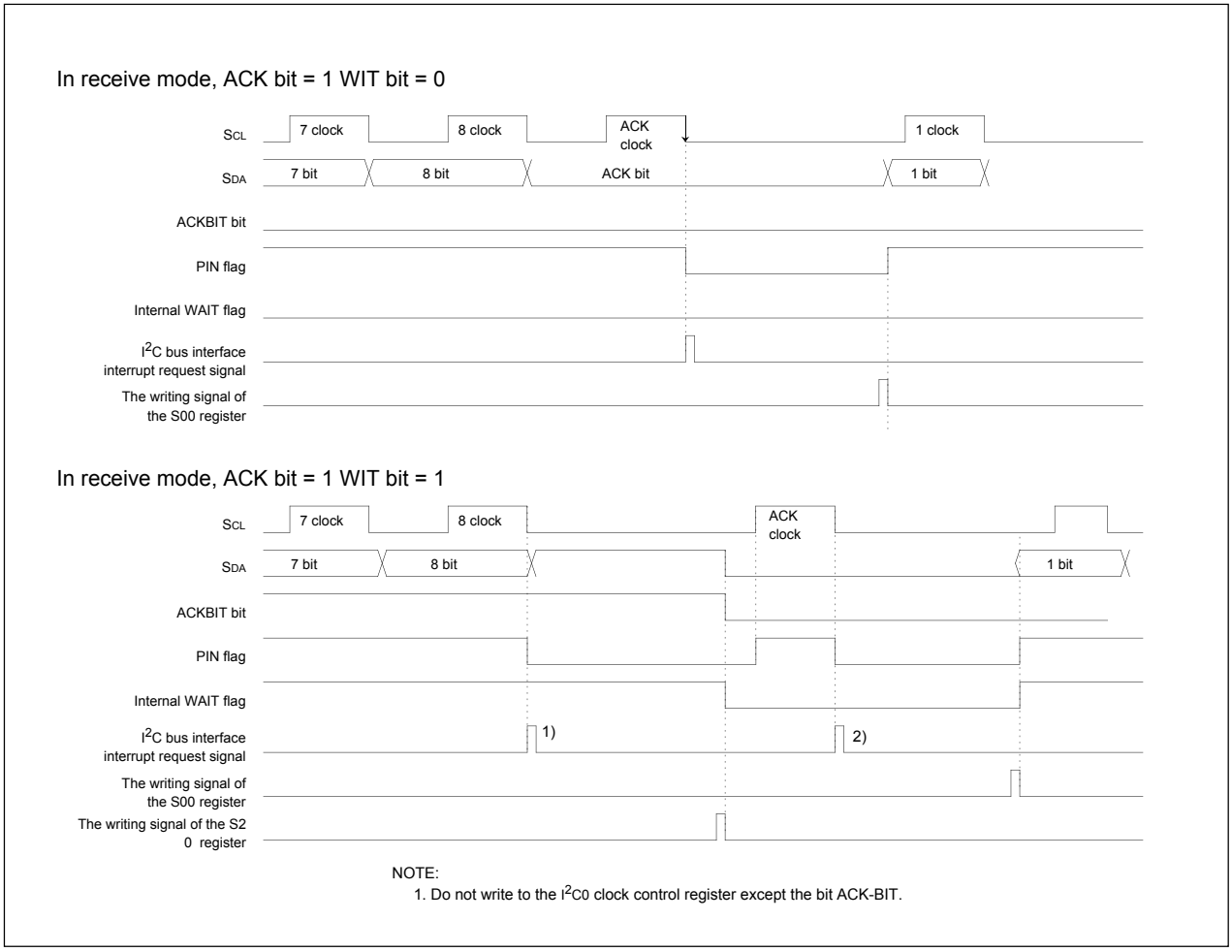


Figure 16.12 The timing of the interrupt generation at the completion of the data receive

16.6.3 Bits 2,3 : Port Function Select Bits PED, PEC

If the ES0 bit in the S1D0 register is set to 1 (I^2C bus interface enabled), the SDAMM functions as an output port. When the PED bit is set to 1 and the SCLMM functions as an output port when the PEC bit is set to 1. Then the setting values of bits P2_0 and P2_1 in the port P2 register are output to the I^2C bus, regardless of he internal SCL/SDA output signals. (SCL/SDA pins are onnected to I^2C bus interface circuit)

The bus data can be read by reading the port pi direction register in input mode, regardless of the setting values of the PED and PEC bits. **Table 16.5** shows the port specification.

Table 16.5 Port specifications

Pin Name	ES9 Bit	PED Bit	P20 Port Direction Register	Function
P20	0	-	0/1	Port I/O function
	1	0	-	SDA I/O function
	1	1	-	SDA input function, port output function
Pin Name	ES0 Bit	PEC Bit	P21 Port Direction Register	Function
P21	0	-	0/1	Port I/O function
	1	0	-	SCL I/O function
	1	1	-	SCL input function, port output funcion

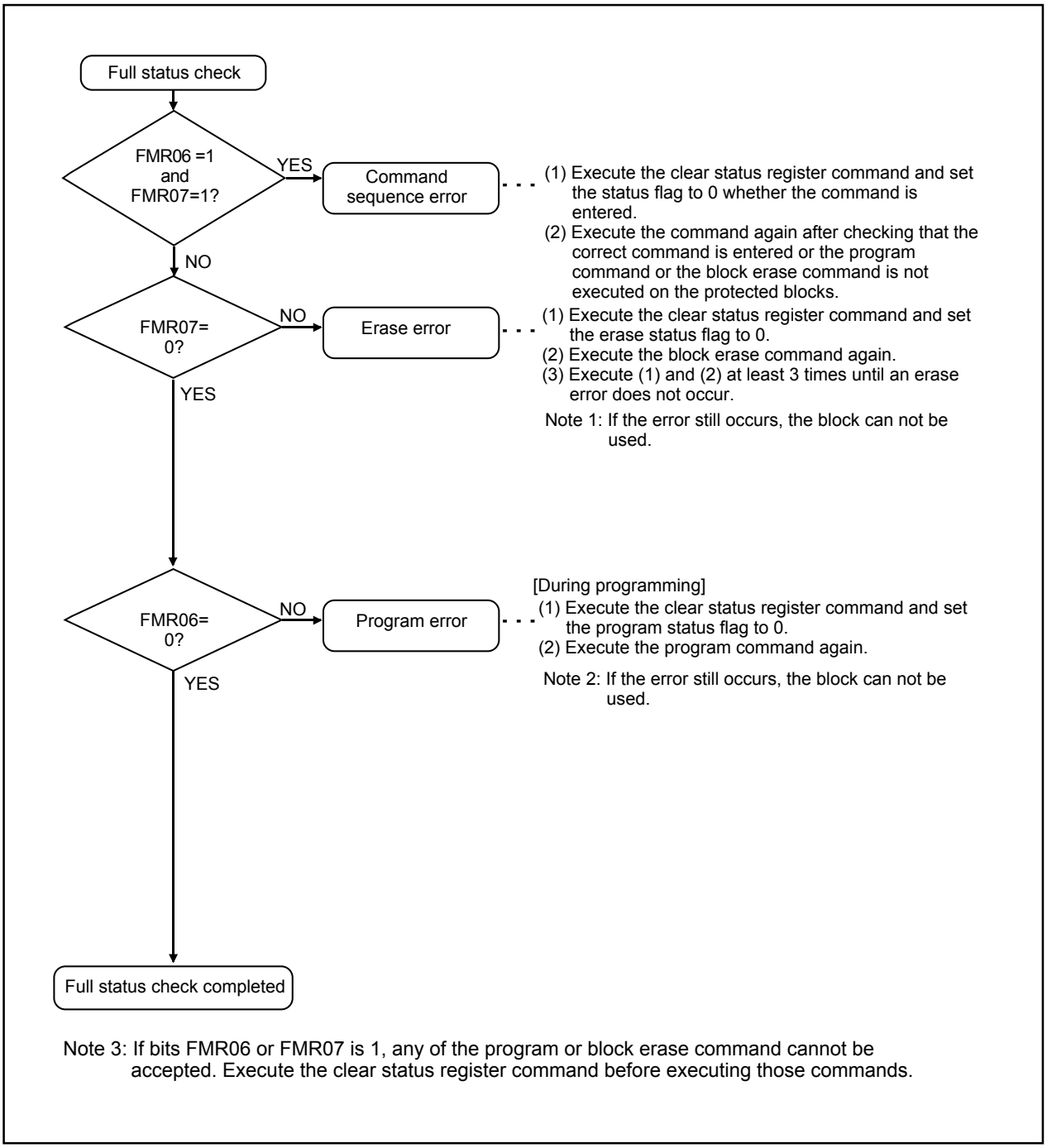


Figure 20.14 Full Status Check and Handling Procedure for Each Error

Table 21.6 Low Voltage Detection Circuit Electrical Characteristics (Note 1, Note 3)

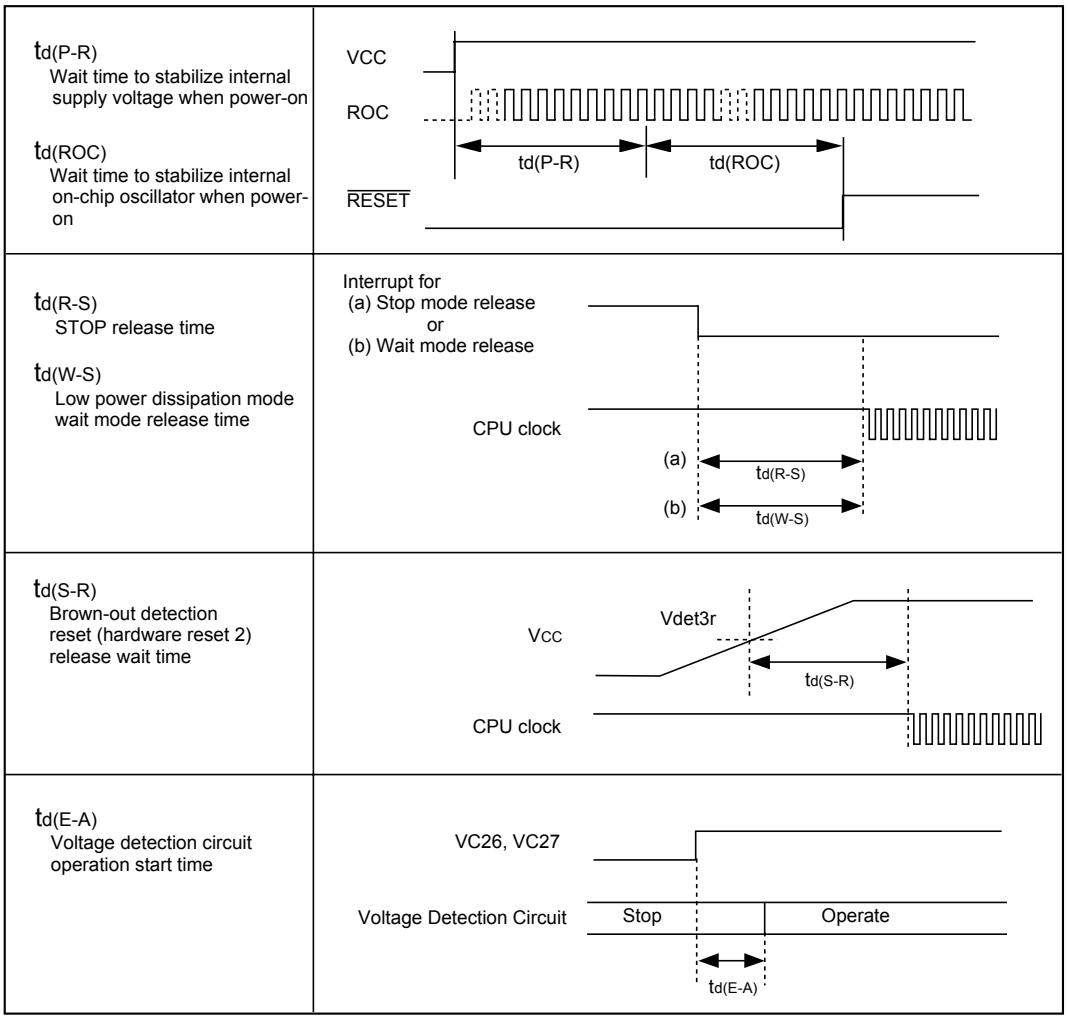
Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet4	Low Voltage Detection Voltage(1)	Vcc=0.8 to 5.5V	3.2	3.8	4.45	V
Vdet3	Reset Space Detection Voltage(1)		2.3	2.8	3.4	V
Vdet3s	Low Voltage Reset Hold Voltage(2)				1.7	V
Vdet3r	Low Voltage Reset Release Voltage		2.35	2.9	3.5	V

NOTES:
1. Vdet4 >Vdet3
2. Vdet3s is the minmum voltage to maintain brown-out detection reset (hardware reset 2).
3. The low Voltage detection circuit is designed to use when Vcc is set to 5V.
4. If the supply power voltage is greater than the reset level detection voltage when the reset level detection voltage is less than 2.7V, the operation at f(BCLK) < 10MHz is guranteed. However, A/D conversion, serial I/O, flash memory program and erase are excluded.

Table 21.7 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait Time to Stabilize Internal Supply Voltage when Power-on	Vcc = 2.7 to 5.5 V			2	ms
td(ROC)	Wait Time to Stabilize Internal On-chip Oscillator when Power-on				40	µs
td(R-S)	STOP Release Time				150	µs
td(W-S)	Low Power Dissipation Mode Wait Mode Release Time				150	µs
td(S-R)	Hardware Reset 2 Release Wait Time	Vcc = Vdet3r to 5.5 V		6(1)	20	ms
td(E-A)	Low Voltage Detection Circuit Operation Start Time	Vcc = 2.7 to 5.5 V			20	µs

NOTE:
1. When Vcc=5



V_{CC} = 5V

Table 21.8 Electrical Characteristics (Note 1)

Symbol	Parameter				Condition	Standard			Unit
						Min.	Typ.	Max.	
V_{OH}	Output High ("H") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$			I_{OH}=-5mA	V_{CC}-2.0		V_{CC}	V
V_{OH}	Output High ("H") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$			I_{OH}=-200µA	V_{CC}-0.3		V_{CC}	V
V_{OH}	Output High ("H") Voltage		X_{OUT}	High Power	I_{OH}=-1mA	V_{CC}-2.0		V_{CC}	V
				Low Power	I_{OH}=-0.5mA	V_{CC}-2.0		V_{CC}	
	Output High ("H") Voltage		X_{COUT}	High Power	No load applied		2.5		V
				Low Power	No load applied		1.6		
V_{OL}	Output Low ("L") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$			I_{OL}=5mA			2.0	V
V_{OL}	Output Low ("L") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$			I_{OL}=200µA			0.45	V
V_{OL}	Output Low ("L") Voltage		X_{OUT}	High Power	I_{OL}=1mA			2.0	V
				Low Power	I_{OL}=0.5mA			2.0	
	Output Low ("L") Voltage		X_{COUT}	High Power	No load applied		0		V
				Low Power	No load applied		0		
V_{T+}-V_{T-}	Hysteresis	$TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB2_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS2}$, SCL, SDA, $CLK0$-$CLK2$, $TA2_{OUT}$-$TA4_{OUT}$, $\overline{KI0}$-$\overline{KI3}$, $RXD0$-$RXD2$, $SIN3$, $SIN4$				0.2		1.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$				0.2		2.5	V
V_{T+}-V_{T-}	Hysteresis	X_{IN}				0.2		0.8	V
I_{IH}	Input High ("H") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}			V_I=5V			5.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}			V_I=0V			-5.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$			V_I=0V	30	50	170	kΩ
Rf_{XIN}	Feedback Resistance		X_{IN}				1.5		MΩ
Rf_{XCIN}	Feedback Resistance		X_{CIN}				15		MΩ
V_{RAM}	RAM Standby Voltage				In stop mode	2.0			V

NOTES:

1. Referenced to V_{CC}=4.2 to 5.5V, V_{SS}=0V at Topr=-20 to 85 ° C / -40 to 85 ° C, f(BCLK)=20MHz unless otherwise specified.

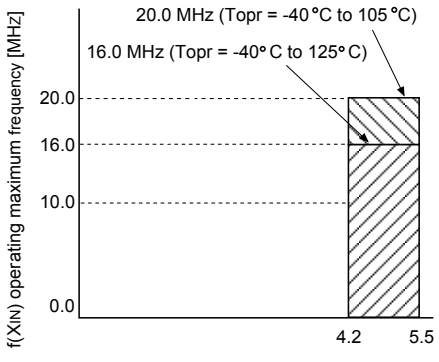
Table 21.79 Recommended Operating Conditions (1)

Symbol	Parameter			Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply Voltage			4.2		5.5	V
AVcc	Analog Supply Voltage				Vcc		V
V_{SS}	Supply Voltage				0		V
AVss	Analog Supply Voltage				0		V
V_{IH}	Input High ("H") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$		0.7 Vcc		Vcc	V
		XIN, $\overline{RESET}$, CNVSS		0.8 Vcc		Vcc	V
		SDAMM, SCLMM	When I^2C bus input level is selected	0.7 Vcc		Vcc	V
			When SMBUS input level is selected	1.4		Vcc	V
V_{IL}	Input Low ("L") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$		0		0.3Vcc	V
		XIN, $\overline{RESET}$, CNVSS		0		0.2Vcc	V
		SDAMM, SCLMM	When I^2C bus input level is selected	0		0.3Vcc	V
			When SMBUS input level is selected	0		0.6	V
$I_{OH(peak)}$	Peak Output High ("H") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$				-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$				-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$				10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$				5.0	mA
f(X_{IN})	Main Clock Input Oscillation Frequency(4)		Topr = -40 to 105 ° C	0		20	MHz
			Topr = -40 to 125 ° C	0		16	MHz
f(X_{CIN})	Sub Clock Oscillation Frequency				32.768	50	kHz
f_1(ROC)	On-chip Oscillator Frequency 1			0.5	1	2	MHz
f2(ROC)	On-chip Oscillator Frequency 2			1	2	4	MHz
f3(ROC)	On-chip Oscillator Frequency 3			8	16	26	MHz
f(PLL)	PLL Clock Oscillation Frequency(4)		Topr = -40 to 105 ° C	10		20	MHz
			Topr = -40 to 125 ° C	10		16	MHz
f(BCLK)	CPU Operation Clock Frequency		Topr = -40 to 105 ° C	0		20	MHz
			Topr = -40 to 125 ° C	0		16	MHz
t_{SU}(PLL)	Wait Time to Stabilize PLL Frequency Synthesizer		Vcc = 5.0 V			20	MHz

NOTES:

1. Referenced to Vcc = 4.2 to 5.5 V at Topr = -40 to 125 ° C unless otherwise specified.
2. The mean output current is the mean value within 100ms.
3. The total $I_{OL(peak)}$ for all ports must be 80 mA or less. The total $I_{OH(peak)}$ for all ports must be -80 mA or less.
4. Relationship among main clock oscillation frequency, PLL clock oscillation frequency and supply voltage.

Main clock input oscillation frequency



PLL clock oscillation frequency

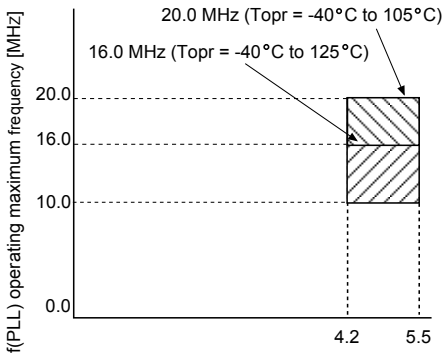
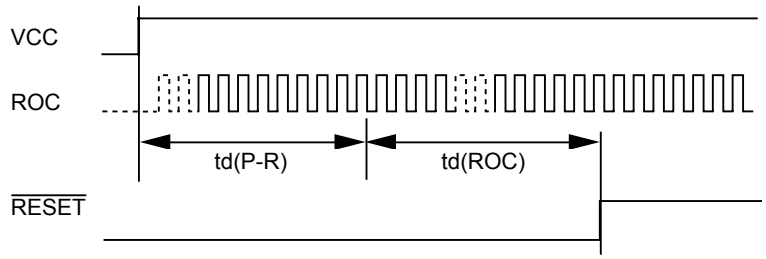


Table 21.83 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait Time to Stabilize Internal Supply Voltage when Power-on	V_{CC}=4.2 to 5.5V			2	ms
td(ROC)	Wait Time to Stabilize Internal On-chip Oscillator when Power-on				40	µs
td(S-R)	STOP Release Time				150	µs
td(E-A)	Low Power Dissipation Mode Wait Mode Release Time				150	µs

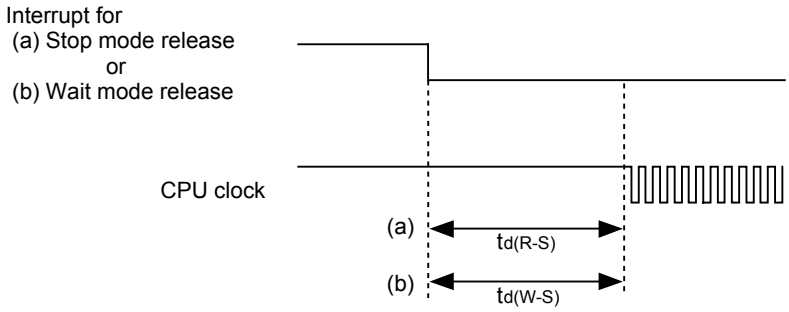
$t_{d(P-R)}$
Wait time to stabilize internal supply voltage when power-on

$t_{d(ROC)}$
Wait time to stabilize internal on-chip oscillator when power-on



$t_{d(R-S)}$
STOP release time

$t_{d(W-S)}$
Low power dissipation mode wait mode release time



22.7.2 Rewrite the ICOCiIC Register

When the interrupt request to the ICOCiIC register is generated during the instruction process, the IR bit may not be set to 1 (interrupt requested) and the interrupt request may not be acknowledged. At that time, when the bit in the G1IR register is held to 1 (interrupt requested), the following IC/OC interrupt request will not be generated. When changing the ICOCiIC register settiing, use the following instruction.

Subject instructions: AND, OR, BCLR, BSET

When initializing Timer S, change the ICOCiIC register setting with the request again after setting registers IOCiIC and G1IR to 00_{16}.

22.7.3 Waveform Generating Function

1. If the BTS bit in the G1BCR1 register is set to 0 (base timer is reset) when the waveform is generating and the base timer is stopped counting, the waveform output pin keeps the same output level. The output level will be changed when the base timer and the G1POj register match the setting value next time after the base timer starts counting again.
2. If the G1POCRj register is set when the waveform is generated, the same setting value of the IVL bit is applied to the waveform generating pin. Do not set the G1POCRj register when the waveform is generating.
3. When the RST1 bit in the G1BCR1 register is set to 1 (the base timer is reset by matching the G1PO0 register), the base timer is reset after two clock cycles of f_{BT1} when the base timer value matches the G1PO0 register value. A high-level ("H") signal is applied to the OUTC10 pin between the base timer value match to the base timer reset.

22.7.4 IC/OC Base Timer Interrupt

If the MCU is operated in the combination selected from **Table 22.1** for use when the RST4 bit in the G1BCR0 register is set to 1 (reset the base timer that matches the G1BTRR register) to reset the base timer, an IC/OC base timer interrupt request is generated twice.

Table 22.1 Uses of IT Bit in the G1BCR0 Register and G1BTRR Register

IT Bit in the G1BCR0 Register	G1BTRR Register
0 (bit 15 in the base timer overflows)	$07FFF_{16}$ to $0FFFE_{16}$
1 (bit 14 in the base timer overflows)	$03FFF_{16}$ to $0FFFE_{16}$ or $0BFFF_{16}$ to $0FFFE_{16}$

The second IC/OC base timer interrupt request is generated because the base timer overflow request is generated after one fBT1 clock cycle as soon as the base timer is reset.

One of the following conditions must be met in order not to generate the IC/OC base timer interrupt request twice:

1) When the RST4 bit is set to 1, set the G1BTRR register with a combination other than what is listed in **Table 22.1**.
2) Do not reset the base timer by matching the G1BTRR register. Reset the base timer by matching the G1P00 register. In other words, do not set the RST4 bit to 1 to reset the base timer. Set the RST1 bit in the G1BCR1 register to 1 (reset the base timer that matches the G1P00 register).