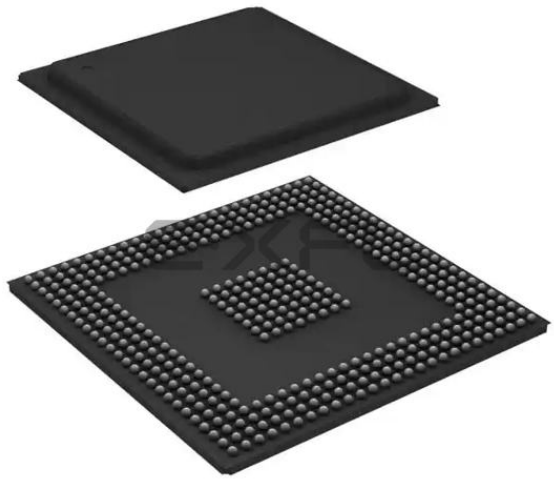

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Details	
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Peripherals	DMA, POR, PWM, WDT
Number of I/O	256
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 40x12b
Oscillator Type	External
Operating Temperature	-55°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc5554azp132

3 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MCU.

3.1 Maximum Ratings

Table 2. Absolute Maximum Ratings [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	1.5 V core supply voltage [2]	V_{DD}	–0.3	1.7	V
2	Flash program/erase voltage	V_{PP}	–0.3	6.5	V
4	Flash read voltage	V_{FLASH}	–0.3	4.6	V
5	SRAM standby voltage	V_{STBY}	–0.3	1.7	V
6	Clock synthesizer voltage	V_{DDSYN}	–0.3	4.6	V
7	3.3 V I/O buffer voltage	V_{DD33}	–0.3	4.6	V
8	Voltage regulator control input voltage	V_{RC33}	–0.3	4.6	V
9	Analog supply voltage (reference to V_{SSA})	V_{DDA}	–0.3	5.5	V
10	I/O supply voltage (fast I/O pads) [3]	V_{DDE}	–0.3	4.6	V
11	I/O supply voltage (slow and medium I/O pads) [3]	V_{DDEH}	–0.3	6.5	V
12	DC input voltage [4] V_{DDEH} powered I/O pads V_{DDE} powered I/O pads	V_{IN}	 –1.0 [5] –1.0 [5]	 6.5 [6] 4.6 [7]	V
13	Analog reference high voltage (reference to V_{RL})	V_{RH}	–0.3	5.5	V
14	V_{SS} to V_{SSA} differential voltage	$V_{SS} – V_{SSA}$	–0.1	0.1	V
15	V_{DD} to V_{DDA} differential voltage	$V_{DD} – V_{DDA}$	$–V_{DDA}$	V_{DD}	V
16	V_{REF} differential voltage	$V_{RH} – V_{RL}$	–0.3	5.5	V
17	V_{RH} to V_{DDA} differential voltage	$V_{RH} – V_{DDA}$	–5.5	5.5	V
18	V_{RL} to V_{SSA} differential voltage	$V_{RL} – V_{SSA}$	–0.3	0.3	V
19	V_{DDEH} to V_{DDA} differential voltage	$V_{DDEH} – V_{DDA}$	$–V_{DDA}$	V_{DDEH}	V
20	V_{DDF} to V_{DD} differential voltage	$V_{DDF} – V_{DD}$	–0.3	0.3	V
21	V_{RC33} to V_{DDSYN} differential voltage spec has been moved to Table 9 DC Electrical Specifications, Spec 43a.				
22	V_{SSSYN} to V_{SS} differential voltage	$V_{SSSYN} – V_{SS}$	–0.1	0.1	V
23	V_{RCVSS} to V_{SS} differential voltage	$V_{RCVSS} – V_{SS}$	–0.1	0.1	V
24	Maximum DC digital input current [8] (per pin, applies to all digital pins) [4]	I_{MAXD}	–2	2	mA
25	Maximum DC analog input current [9] (per pin, applies to all analog pins)	I_{MAXA}	–3	3	mA
26	Maximum operating temperature range [10] Die junction temperature	T_J	T_L	150.0	°C
27	Storage temperature range	T_{STG}	–55.0	150.0	°C

Table 2. Absolute Maximum Ratings [1] (continued)

Spec	Characteristic	Symbol	Min.	Max.	Unit
28	Maximum solder temperature [11] Lead free (Pb-free) Leaded (SnPb)	T_{SDR}	 — —	 260.0 245.0	°C
29	Moisture sensitivity level [12]	MSL	—	3	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond any of the listed maxima can affect device reliability or cause permanent damage to the device.

2 1.5 V ± 10% for proper operation. This parameter is specified at a maximum junction temperature of 150 °C.

3 All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}, or V_{DDEH}.

4 AC signal overshoot and undershoot of up to ± 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).

5 Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met. Keep the negative DC voltage greater than –0.6 V on eTPUB[15] and SINB during the internal power-on reset (POR) state.

6 Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.

7 Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.

8 Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

9 Total injection current for all analog input pins must not exceed 15 mA.

10 Lifetime operation at these specification limits is not guaranteed.

11 Moisture sensitivity profile per IPC/JEDEC J-STD-020D.

12 Moisture sensitivity per JEDEC test method A112.

3.2 Thermal Characteristics

The shaded rows in the following table indicate information specific to a four-layer board.

Table 3. MPC5554 Thermal Characteristics

Spec	MPC5554 Thermal Characteristic	Symbol	416 PBGA	Unit
1	Junction to ambient [1, 2], natural convection (one-layer board)	$R_{\theta JA}$	24	°C/W
2	Junction to ambient [1, 3], natural convection (four-layer board 2s2p)	$R_{\theta JA}$	18	°C/W
3	Junction to ambient [1, 3] (@200 ft./min., one-layer board)	$R_{\theta JMA}$	19	°C/W
4	Junction to ambient [1, 3] (@200 ft./min., four-layer board 2s2p)	$R_{\theta JMA}$	15	°C/W
5	Junction to board [4] (four-layer board 2s2p)	$R_{\theta JB}$	9	°C/W
6	Junction to case [5]	$R_{\theta JC}$	5	°C/W
7	Junction to package top [6], natural convection	Ψ_{JT}	2	°C/W

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (^oC)

T_B = board temperature at the package perimeter ($^oC/W$)

$R_{\theta JB}$ = junction-to-board thermal resistance ($^oC/W$) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction-to-case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case-to-ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Rd.
San Jose, CA., 95134
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the web at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.3 Package

The MPC5554 is available in packaged form. Read the package options in Section 2, “Ordering Information.” Refer to Section 4, “Mechanicals,” for pinouts and package drawings.

3.4 EMI (Electromagnetic Interference) Characteristics

Table 4. EMI Testing Specifications [1]

Spec	Characteristic	Minimum	Typical	Maximum	Unit
1	Scan range	0.15	—	1000	MHz
2	Operating frequency	—	—	f_{MAX}	MHz
3	V_{DD} operating voltages	—	1.5	—	V
4	V_{DDSYN}, V_{RC33}, V_{DD33}, V_{FLASH}, V_{DDE} operating voltages	—	3.3	—	V
5	V_{PP}, V_{DDEH}, V_{DDA} operating voltages	—	5.0	—	V
6	Maximum amplitude	—	—	14 [2] 32 [3]	dBuV
7	Operating temperature	—	—	25	°C

1 EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03. Qualification testing was performed on the MPC5554 and applied to the MPC5500 family as generic EMI performance data.

2 Measured with the single-chip EMI program.

3 Measured with the expanded EMI program.

Table 6. V_{RC} and POR Electrical Specifications (continued)

Spec	Characteristic		Symbol	Min.	Max.	Units
8	Voltage differential during power up such that: V_{DD33} can lag V_{DDSYN} or V_{DDEH6} before V_{DDSYN} and V_{DDEH6} reach the V_{POR33} and V_{POR5} minimums respectively.		V_{DD33_LAG}	—	1.0	V
9	Absolute value of slew rate on power supply pins		—	—	50	V/ms
10	Required gain at Tj: $I_{DD} \div I_{VRCCTL}$ (@ $f_{sys} = f_{MAX}$)[6, 8, 9, 10]	– 55° C[7]	BETA[11]	70	—	—
		– 40° C		70	—	—
		25° C		85[11]	—	—
		150° C		105[11]	500	—

1 The internal POR signals are V_{POR15}, V_{POR33}, and V_{POR5}. On power up, assert $\overline{\text{RESET}}$ before the internal POR negates. $\overline{\text{RESET}}$ must remain asserted until the power supplies are within the operating conditions as specified in Table 9 DC Electrical Specifications. On power down, assert $\overline{\text{RESET}}$ before any power supplies fall outside the operating conditions and until the internal POR asserts.

2 V_{IL_S} (Table 9, Spec15) is guaranteed to scale with V_{DDEH6} down to V_{POR5}.

3 Supply full operating current for the 1.5 V supply when the 3.3 V supply reaches this range.

4 It is possible to reach the current limit during ramp up—do not treat this event as short circuit current.

5 At peak current for device.

6 Requires compliance with Freescale's recommended board requirements and transistor recommendations. Board signal traces/routing from the V_{RCCTL} package signal to the base of the external pass transistor and between the emitter of the pass transistor to the V_{DD} package signals must have a maximum of 100 nH inductance and minimal resistance (less than 1 Ω). V_{RCCTL} must have a nominal 1 μF phase compensation capacitor to ground. V_{DD} must have a 20 μF (nominal) bulk capacitor (greater than 4 μF over all conditions, including lifetime). Place high-frequency bypass capacitors consisting of eight 0.01 μF, two 0.1 μF, and one 1 μF capacitors around the package on the V_{DD} supply signals.

7 Only available on devices that support -55° C.

8 I_{VRCCTL} is measured at the following conditions: V_{DD} = 1.35 V, V_{RC33} = 3.1 V, V_{VRCCTL} = 2.2 V.

9 Refer to Table 1 for the maximum operating frequency.

10 Values are based on I_{DD} from high-use applications as explained in the I_{DD} Electrical Specification.

11 BETA represents the worst-case external transistor. It is measured on a per-part basis and calculated as ($I_{DD} \div I_{VRCCTL}$).

3.7 Power-Up/Down Sequencing

Power sequencing between the 1.5 V power supply and V_{DDSYN} or the $\overline{\text{RESET}}$ power supplies is required if using an external 1.5 V power supply with V_{RC33} tied to ground (GND). To avoid power-sequencing, V_{RC33} must be powered up within the specified operating range, even if the on-chip voltage regulator controller is not used. Refer to Section 3.7.2, "Power-Up Sequence (VRC33 Grounded)," and Section 3.7.3, "Power-Down Sequence (VRC33 Grounded)."

Power sequencing requires that V_{DD33} must reach a certain voltage where the values are read as ones before the POR signal negates. Refer to Section 3.7.1, "Input Value of Pins During POR Dependent on VDD33."

Although power sequencing is not required between V_{RC33} and V_{DDSYN} during power up, V_{RC33} must not lead V_{DDSYN} by more than 600 mV or lag by more than 100 mV for the V_{RC} stage turn-on to operate within specification. Higher spikes in the emitter current of the pass transistor occur if V_{RC33} leads or lags V_{DDSYN} by more than these amounts. The value of that higher spike in current depends on the board power supply circuitry and the amount of board level capacitance.

Furthermore, when all of the PORs negate, the system clock starts to toggle, adding another large increase of the current consumed by V_{RC33}. If V_{RC33} lags V_{DDSYN} by more than 100 mV, the increase in current consumed can drop V_{DD} low enough to assert the 1.5 V POR again. Oscillations are possible when the 1.5 V POR asserts and stops the system clock, causing the voltage on V_{DD} to rise until the 1.5 V POR negates again. All oscillations stop when V_{RC33} is powered sufficiently.

When powering down, V_{RC33} and V_{DDSYN} have no delta requirement to each other, because the bypass capacitors internal and external to the device are already charged. When not powering up or down, no delta between V_{RC33} and V_{DDSYN} is required for the V_{RC} to operate within specification.

There are no power up/down sequencing requirements to prevent issues such as latch-up, excessive current spikes, and so on. Therefore, the state of the I/O pins during power up and power down varies depending on which supplies are powered.

Table 7 gives the pin state for the sequence cases for all pins with pad type pad_fc (fast type).

Table 7. Pin Status for Fast Pads During the Power Sequence

V_{DDE}	V_{DD33}	V_{DD}	POR	Pin Status for Fast Pad Output Driver pad_fc (fast)
Low	—	—	Asserted	Low
V_{DDE}	Low	Low	Asserted	High
V_{DDE}	Low	V_{DD}	Asserted	High
V_{DDE}	V_{DD33}	Low	Asserted	High impedance (Hi-Z)
V_{DDE}	V_{DD33}	V_{DD}	Asserted	Hi-Z
V_{DDE}	V_{DD33}	V_{DD}	Negated	Functional

Table 8 gives the pin state for the sequence cases for all pins with pad type pad_mh (medium type) and pad_sh (slow type).

Table 8. Pin Status for Medium and Slow Pads During the Power Sequence

V_{DDEH}	V_{DD}	POR	Pin Status for Medium and Slow Pad Output Driver pad_mh (medium) pad_sh (slow)
Low	—	Asserted	Low
V_{DDEH}	Low	Asserted	High impedance (Hi-Z)
V_{DDEH}	V_{DD}	Asserted	Hi-Z
V_{DDEH}	V_{DD}	Negated	Functional

The values in Table 7 and Table 8 do not include the effect of the weak-pull devices on the output pins during power up.

Before exiting the internal POR state, the voltage on the pins go to a high-impedance state until POR negates. When the internal POR negates, the functional state of the signal during reset applies and the weak-pull devices
(up or down) are enabled as defined in the device reference manual. If V_{DD} is too low to correctly propagate the logic signals, the weak-pull devices can pull the signals to V_{DDE} and V_{DDEH}.

[2] $| V_{DDA0} - V_{DDA1} |$ must be < 0.1 V.

[3] V_{PP} can drop to 3.0 V during read operations.

[4] If standby operation is not required, connect V_{STBY} to ground.

[5] Applies to CLKOUT, external bus pins, and Nexus pins.

[6] Maximum average RMS DC current.

[7] Average current measured on automotive benchmark.

[8] Peak currents can be higher on specialized code.

[9] High use current measured while running optimized SPE assembly code with all code and data 100% locked in cache (0% miss rate) with all channels of the eMIOS and eTPU running autonomously, plus the eDMA transferring data continuously from SRAM to SRAM. Higher currents are possible if an “idle” loop that crosses cache lines is run from cache. Write code that avoids this condition.

[10] The current specification relates to average standby operation after SRAM has been loaded with data. For power up current see Section 3.7, “Power-Up/Down Sequencing”, Figure 2.

[11] Power requirements for the V_{DD33} supply depend on the frequency of operation, load of all I/O pins, and the voltages on the I/O segments. Refer to Table 11 for values to calculate the power dissipation for a specific operation.

[12] Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. Refer to Table 10 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

[13] Absolute value of current, measured at V_{IL} and V_{IH}.

[14] Weak pullup/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to pad types: pad_fc, pad_sh, and pad_mh.

[15] Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 ^{o}C to 12 ^{o}C, in the ambient temperature range of 50 ^{o}C to 125 ^{o}C. Applies to pad types: pad_a and pad_ae.

[16] V_{SSA} refers to both V_{SSA0} and V_{SSA1}. $| V_{SSA0} - V_{SSA1} |$ must be < 0.1 V.

[17] Up to 0.6 V during power up and power down.

3.8.1 I/O Pad Current Specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a segment. The output pin current can be calculated from Table 10 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 10.

Table 10. I/O Pad Average DC Current ($T_A = T_L$ to T_H)[1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Drive Select / Slew Rate Control Setting	Current (mA)
1	Slow	I_{DRV_SH}	25	50	5.25	11	8.0
2			10	50	5.25	01	3.2
3			2	50	5.25	00	0.7
4			2	200	5.25	00	2.4
5	Medium	I_{DRV_MH}	50	50	5.25	11	17.3
6			20	50	5.25	01	6.5
7			3.33	50	5.25	00	1.1
8			3.33	200	5.25	00	3.9
9	Fast	I_{DRV_FC}	66	10	3.6	00	2.8
10			66	20	3.6	01	5.2
11			66	30	3.6	10	8.5
12			66	50	3.6	11	11.0
13			66	10	1.98	00	1.6
14			66	20	1.98	01	2.9
15			66	30	1.98	10	4.2
16			66	50	1.98	11	6.7
17			56	10	3.6	00	2.4
18			56	20	3.6	01	4.4
19			56	30	3.6	10	7.2
20			56	50	3.6	11	9.3
21			56	10	1.98	00	1.3
22			56	20	1.98	01	2.5
23			56	30	1.98	10	3.5
24			56	50	1.98	11	5.7
25			40	10	3.6	00	1.7
26			40	20	3.6	01	3.1
27			40	30	3.6	10	5.1
28			40	50	3.6	11	6.6
29			40	10	1.98	00	1.0
30			40	20	1.98	01	1.8
31			40	30	1.98	10	2.5
32			40	50	1.98	11	4.0

1 These values are estimates from simulation and are not tested. Currents apply to output pins only.

2 All loads are lumped.

Table 17. Pad AC Specifications (V_{DDEH} = 5.0 V, V_{DDE} = 1.8 V) [1] (continued)

Spec	Pad	SRC / DSC (binary)	Out Delay [2, 3, 4] (ns)	Rise / Fall [4, 5] (ns)	Load Drive (pF)
3	Fast	00	3.1	2.7	10
		01		2.5	20
		10		2.4	30
		11		2.3	50
4	Pullup/down (3.6 V max)	—	—	7500	50
5	Pullup/down (5.5 V max)	—	—	9000	50

1 These are worst-case values that are estimated from simulation (not tested). The values in the table are simulated at: V_{DD} = 1.35–1.65 V; V_{DDE} = 1.62–1.98 V; V_{DDEH} = 4.5–5.25 V; V_{DD33} and V_{DDSYN} = 3.0–3.6 V; and $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and is guaranteed by design (not tested).

3 The output delay is shown in Figure 4. To calculate the output delay with respect to the system clock, add a maximum of one system clock to the output delay.

4 The output delay and rise and fall are measured to 20% or 80% of the respective signal.

5 This parameter is guaranteed by characterization rather than 100% tested.

Table 18. Derated Pad AC Specifications (V_{DDEH} = 3.3 V, V_{DDE} = 3.3 V) [1]

Spec	Pad	SRC/DSC (binary)	Out Delay [2, 3, 4] (ns)	Rise / Fall [3, 5] (ns)	Load Drive (pF)
1	Slow high voltage (SH)	11	39	23	50
			120	87	200
		01	101	52	50
			188	111	200
		00	507	248	50
			597	312	200
2	Medium high voltage (MH)	11	23	12	50
			64	44	200
		01	50	22	50
			90	50	200
		00	261	123	50
			305	156	200
3	Fast	00	3.2	2.4	10
		01		2.2	20
		10		2.1	30
		11		2.1	50
4	Pullup/down (3.6 V max)	—	—	7500	50
5	Pullup/down (5.5 V max)	—	—	9500	50

1 These are worst-case values that are estimated from simulation (not tested). The values in the table are simulated at: V_{DD} = 1.35–1.65 V; V_{DDE} = 3.0–3.6 V; V_{DDEH} = 3.0–3.6 V; V_{DD33} and V_{DDSYN} = 3.0–3.6 V; and $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and guaranteed by design (not tested).

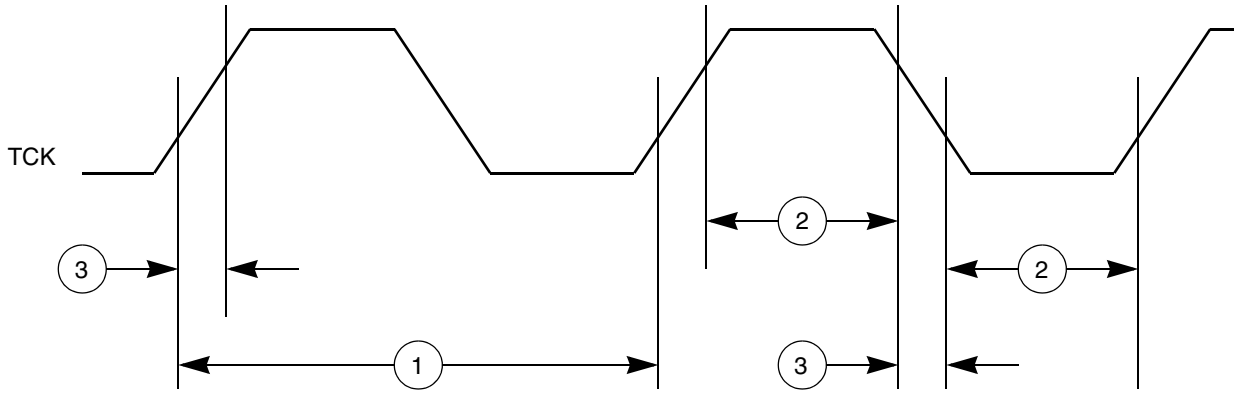


Figure 6. JTAG Test Clock Input Timing

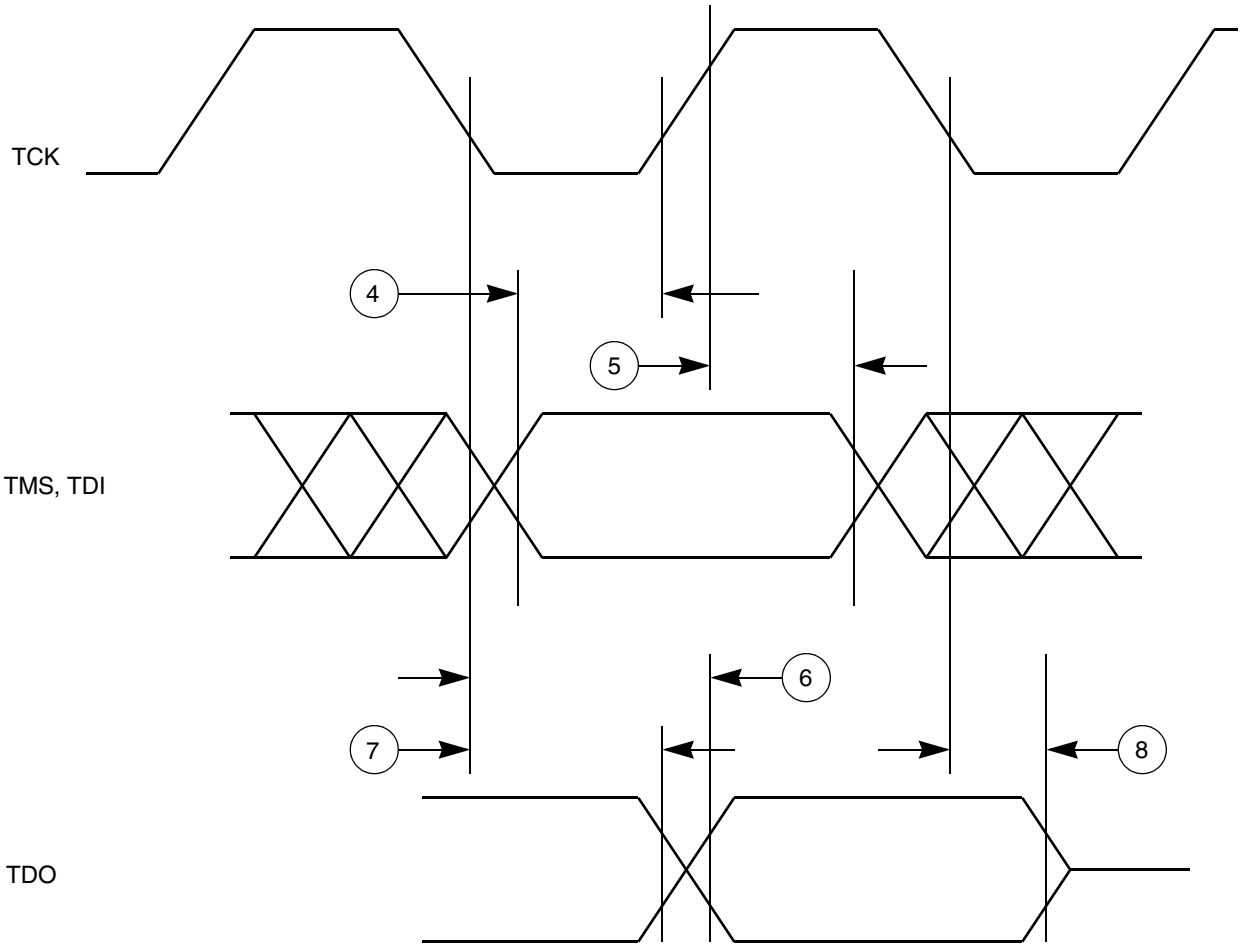


Figure 7. JTAG Test Access Port Timing

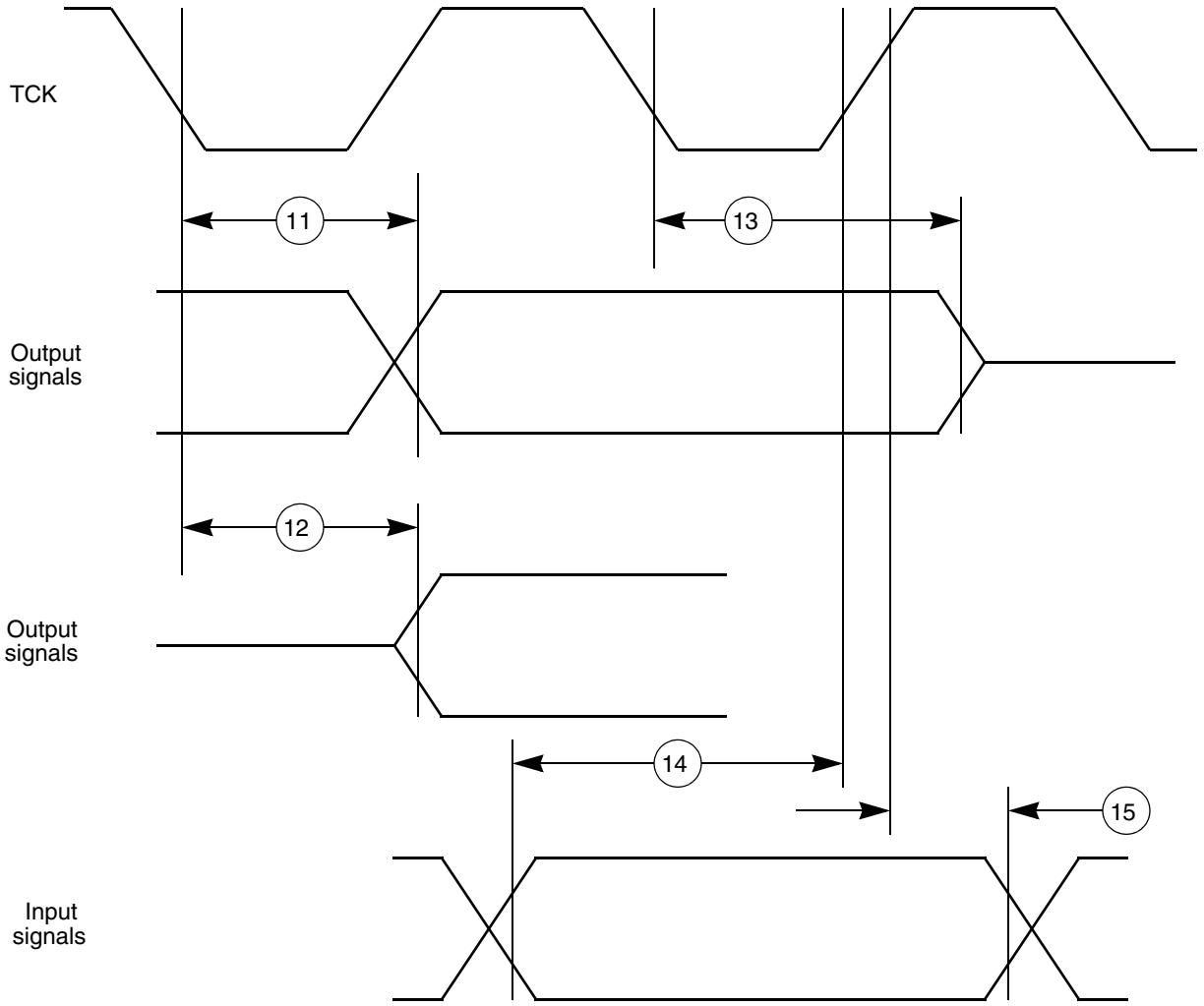


Figure 9. JTAG Boundary Scan Timing

3.13.3 Nexus Timing

Table 21. Nexus Debug Port Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	MCKO cycle time	t_{MCYC}	2[2]	8	t_{CYC}
2	MCKO duty cycle	t_{MDC}	40	60	%
3	MCKO low to MDO data valid [3]	t_{MDOV}	–1.5	3.0	ns
4	MCKO low to $\overline{\text{MSEO}}$ data valid [3]	t_{MSEOV}	–1.5	3.0	ns
5	MCKO low to $\overline{\text{EVTO}}$ data valid [3]	t_{EVTOV}	–1.5	3.0	ns
6	$\overline{\text{EVTI}}$ pulse width	t_{EVTIPW}	4.0	—	t_{TCYC}
7	$\overline{\text{EVTO}}$ pulse width	t_{EVTOPW}	1	—	t_{MCYC}
8	TCK cycle time	t_{TCYC}	4 [4]	—	t_{CYC}
9	TCK duty cycle	t_{TDC}	40	60	%
10	TDI, TMS data setup time	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS data hold time	t_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK low to TDO data valid V_{DDE} = 2.25–3.0 V V_{DDE} = 3.0–3.6 V	t_{JOV}	 0 0	 12 10	 ns ns
13	$\overline{\text{RDY}}$ valid to MCKO [5]	—	—	—	—

1 JTAG specifications apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.35–1.65 V, V_{DDE} = 2.25–3.6 V, V_{DD33} and V_{DDSYN} = 3.0–3.6 V, T_A = T_L to T_H, and CL = 30 pF with DSC = 0b10.

2 The Nexus AUX port runs up to 82 MHz.

3 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until the next MCKO low cycle occurs.

4 Limit the maximum frequency to approximately 16 MHz (V_{DDE} = 2.25–3.0 V) or 20 MHz (V_{DDE} = 3.0–3.6 V) to meet the timing specification for t_{JOV} of [0.2 x t_{JCYC}] as outlined in the IEEE-ISTO 5001-2003 specification.

5 The $\overline{\text{RDY}}$ pin timing is asynchronous to MCKO and is guaranteed by design to function correctly.

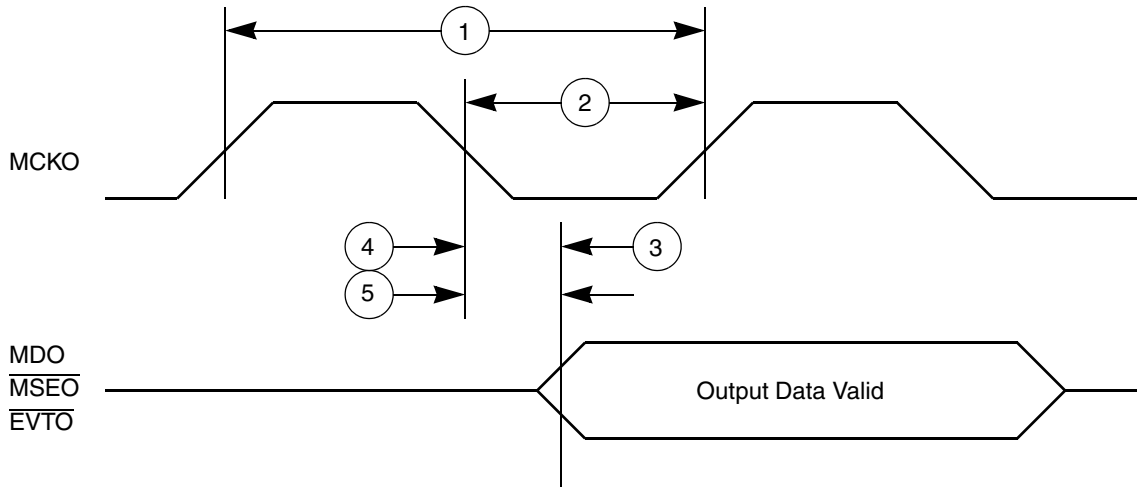


Figure 10. Nexus Output Timing

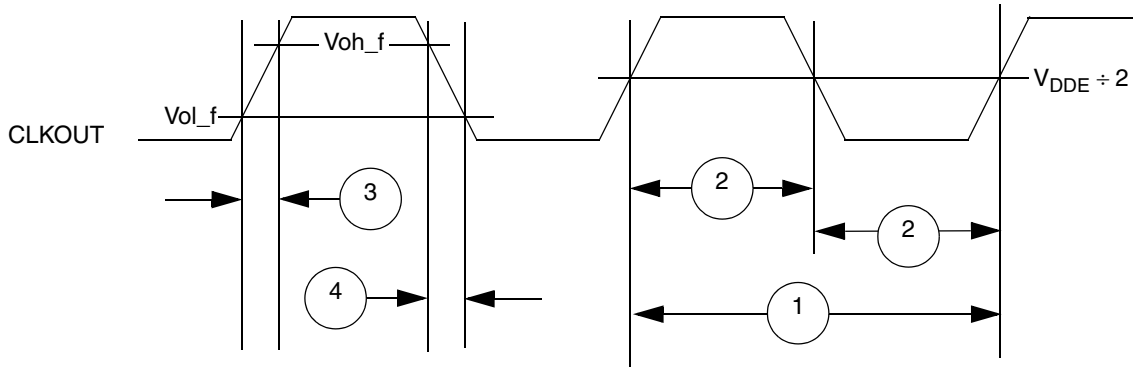


Figure 12. CLKOUT Timing

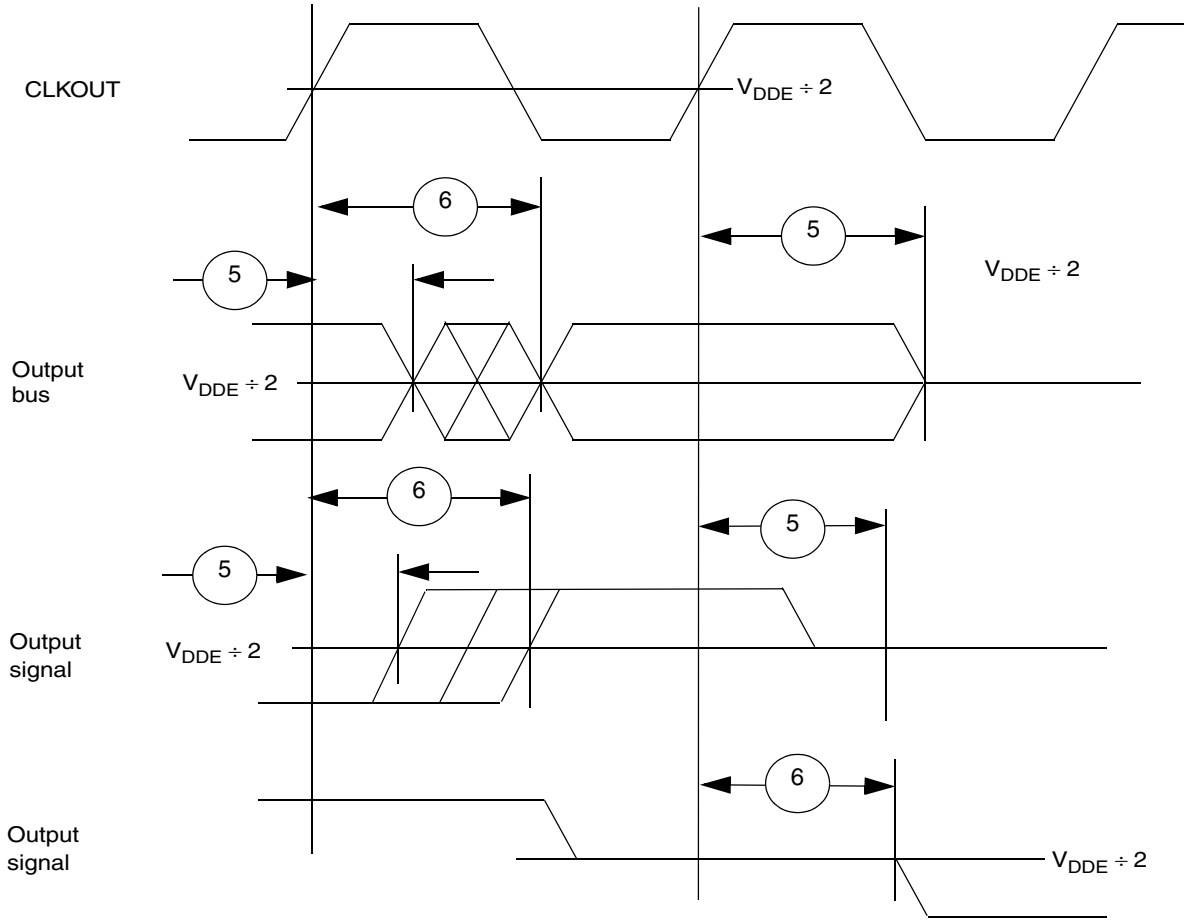


Figure 13. Synchronous Output Timing

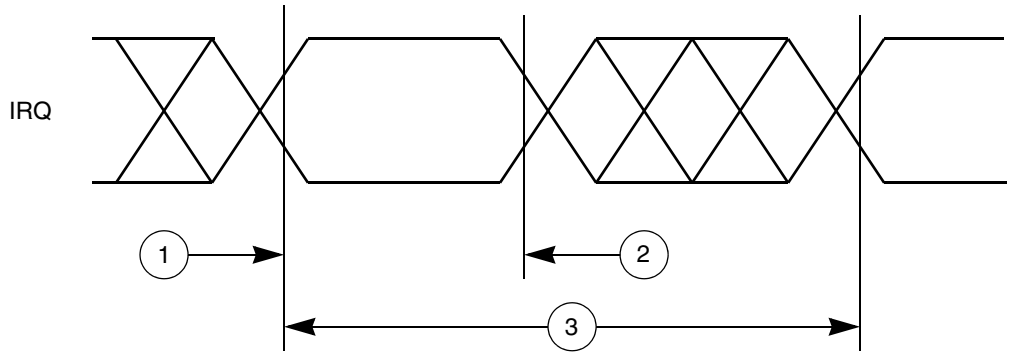


Figure 15. External Interrupt Timing

3.13.6 eTPU Timing

Table 24. eTPU Timing [1]

Spec	Characteristic	Symbol	Min.	Max	Unit
1	eTPU input channel pulse width	t_{ICPW}	4	—	t_{CYC}
2	eTPU output channel pulse width	t_{OCPW}	2 [2]	—	t_{CYC}

1 eTPU timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

2 This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

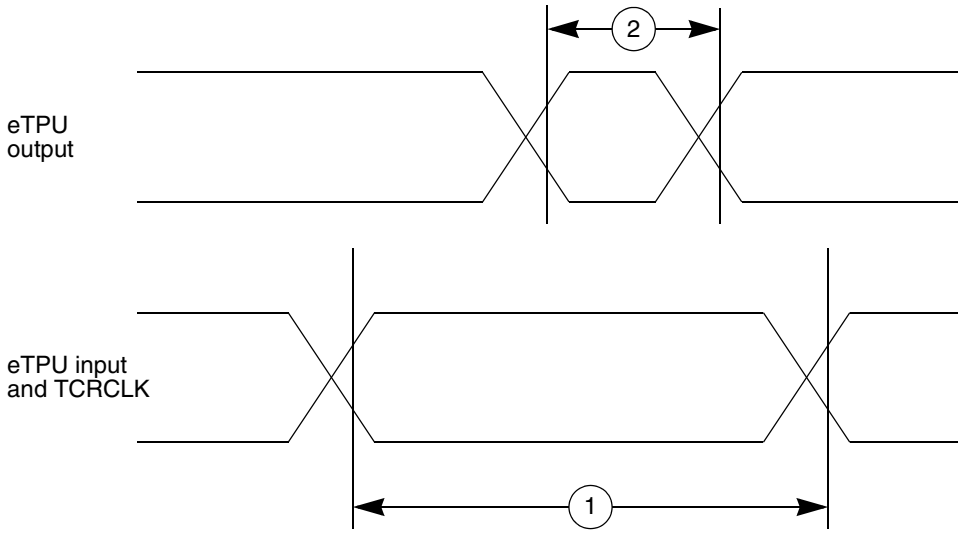


Figure 16. eTPU Timing

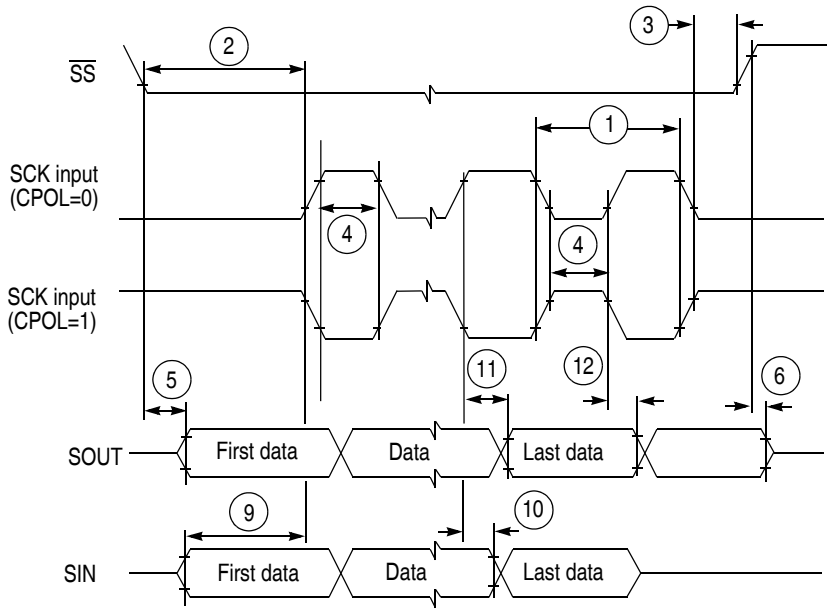


Figure 24. DSPI Modified Transfer Format Timing—Slave, CPHA = 0

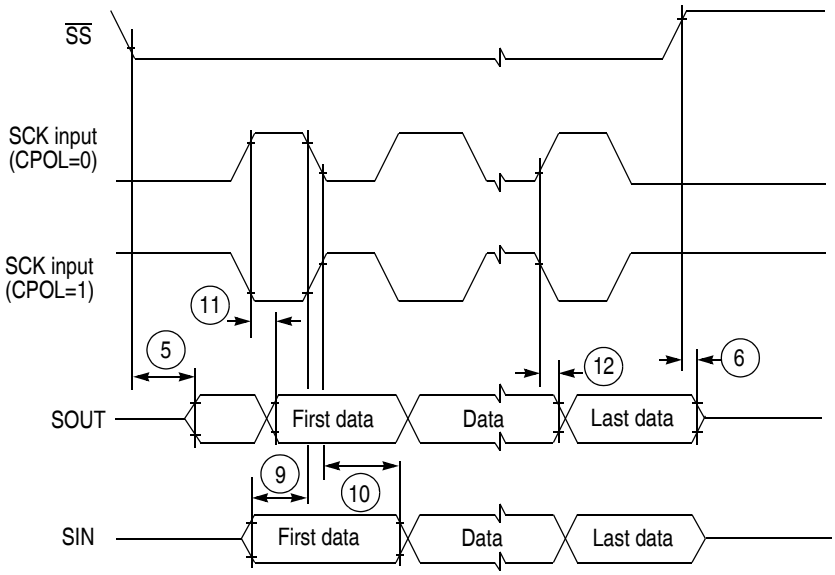


Figure 25. DSPI Modified Transfer Format Timing—Slave, CPHA = 1

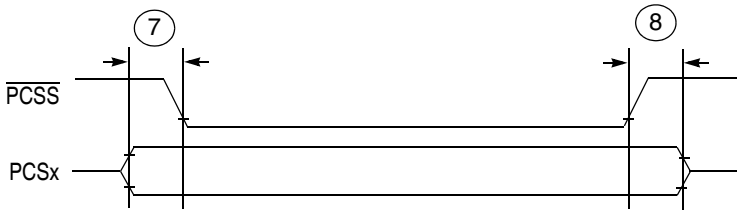


Figure 26. DSPI PCS Strobe (PCSS) Timing

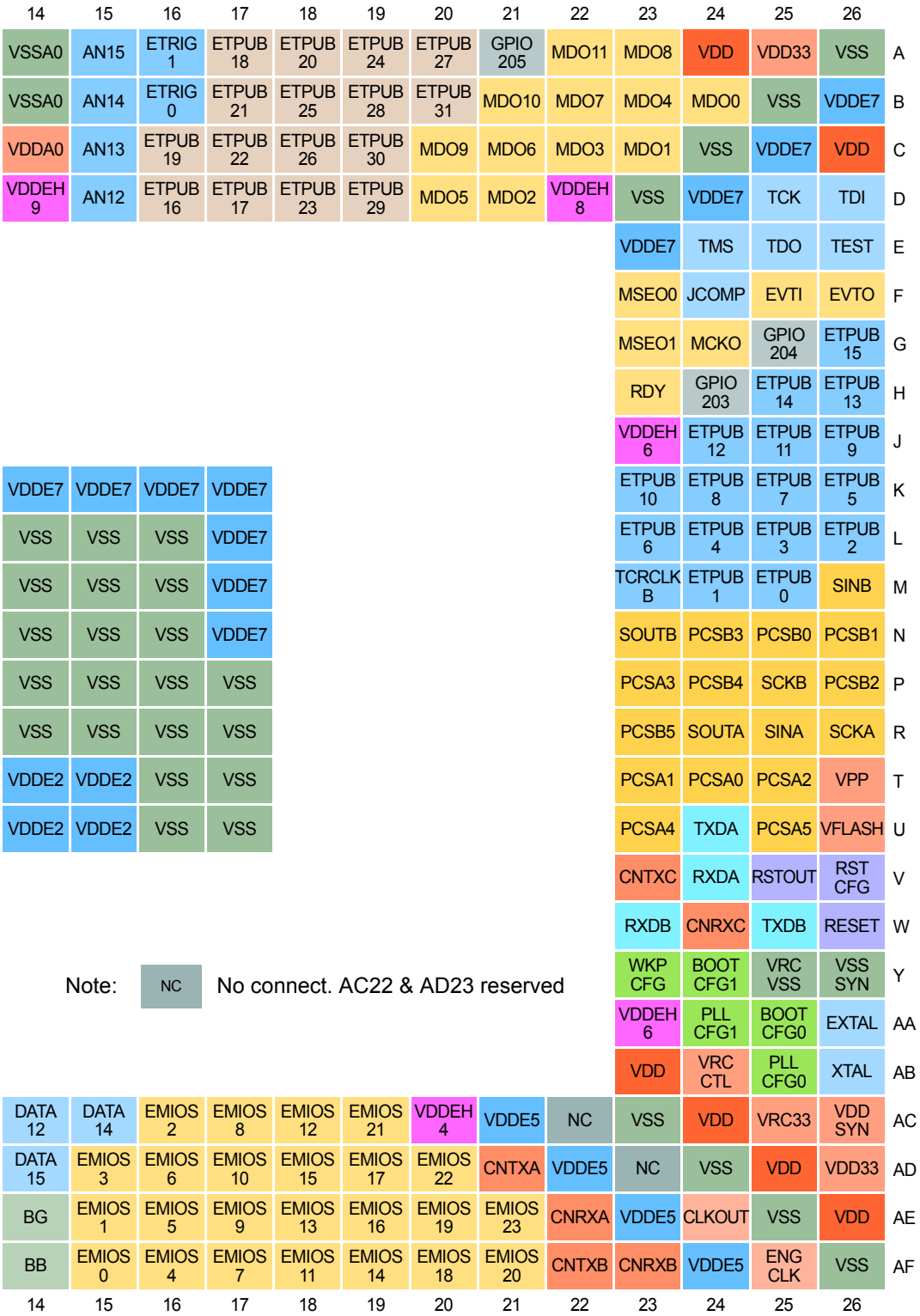
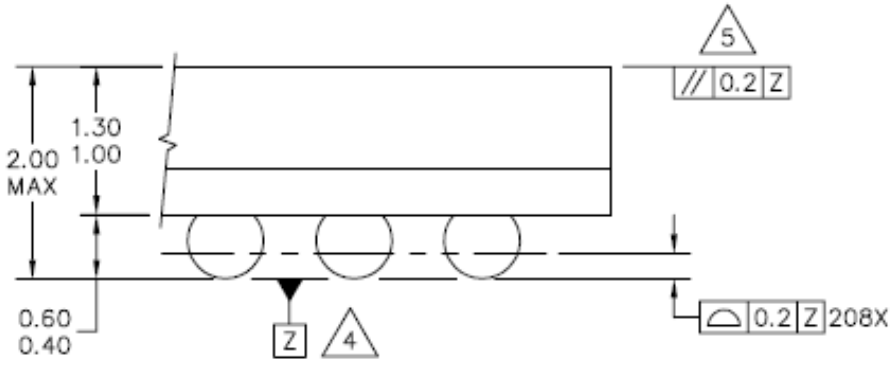


Figure 30. MPC5553546667 416 Package Right Side (view 2 of 2)

Figure 31. MPC5567 416 Package



DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	DOCUMENT NO: 98ARS23882W	REV: D
	CASE NUMBER: 1159A–01	02 AUG 2005
	STANDARD: JEDEC MO–151 AAF–1	

Figure 32. MPC55 208 MAP BGA Package (continued)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 416 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)	DOCUMENT NO: 98ARE10523D	REV: A
	CASE NUMBER: 1494–01	13 JUL 2005
	STANDARD: JEDEC MS–034 AAL–1	

Figure 34. MPC5554 416 TEPBGA Package (continued)

Table 28. Changes Between Rev. 2.0 and 3.0 (continued)

Location	Description of Changes
Section 3.7, "Power-Up/Down Sequencing	
	Last paragraph: Changed the first sentence FROM , , , the voltage on the pins goes to high-impedance until . . . TO. . .the pins go to a high-impedance state until . . .
Section 3.7.3, "Power-Down Sequence (VRC33 Grounded)"	
	Last sentence: Changed from: 'This ensures that the digital 1.5 V logic, which is reset by the ORed POR only and can cause the 1.5 V supply to decrease below its specification, is reset properly.' To: 'This ensures that the digital 1.5 V logic, which is reset only by an ORed POR and can cause the 1.5 V supply to decrease less than its specification, resets correctly.'
Section 4.1, "MPC5553546667 416 PBGA Pinout"	
	Added the following NOTE before the 416 BGA Map: NOTE The MPC5500 devices are pin compatible for software portability and use the primary function names to label the pins in the BGA diagram. Although some devices do not support all the primary functions shown in the BGA diagram, the muxed and GPIO signals on those pins remain available. See the signals chapter in the device reference manual for the signal muxing.
Table 5 (ESD Ratings ,) ESD Ratings:	
	Changed footnote 2 from: • 'Device failure is defined as: 'If after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing will be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.' to: • Device failure is defined as: 'If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.
Table 6 (V_{RC} and POR Electrical Specifications) VCR/POR Electrical Specifications:	
	• Added footnote 1 to specs 1, 2, and 3 that reads: The internal POR signals are V_{POR15}, V_{POR33}, and V_{POR5}. On power up, assert $\overline{\text{RESET}}$ before the internal POR negates. $\overline{\text{RESET}}$ must remain asserted until the power supplies are within the operating conditions as specified in Table 9 DC Electrical Specifications. On power down, assert $\overline{\text{RESET}}$ before any power supplies fall outside the operating conditions and until the internal POR asserts. • Reformatted columns.
Table 9 (DC Electrical Specifications ($T_A = T_L$ to T_H)) DC Electrical Specifications:	
	• Added footnote that reads: V_{DDE2} and V_{DDE3} are limited to 2.25–3.6 V only if SIU_ECCR[EBTS] = 0; V_{DDE2} and V_{DDE3} have a range of 1.6–3.6 V if SIU_ECCR[EBTS] =1. • Added ($T_A = T_L$ to T_H) to the table title.
Table 14 (Flash Program and Erase Specifications ($T_A = T_L$ to T_H)) Flash Program and Erase Specifications ($T_A = T_L$ to T_H)	
	• Footnote 1, Changed 'Typical program and erase times assume nominal supply values and operation at 25 °C' to 'Typical program and erase times are calculated at 25 °C operating temperature using nominal supply values..'
Table 17 (Pad AC Specifications (VDDEH = 5.0 V, VDDE = 1.8 V)) Pad AC Specifications (V_{DDEH} = 5.0 V, V_{DDE} = 1.8 V)	
	• Footnote 1, changed 'V_{DDEH} = 4.5–5.5;' to 'V_{DDEH} = 4.5–5.25;'
Table 19 (Reset and Configuration Pin Timing) Reset and Configuration Pin Timing:	
	• Footnote 1: Removed V_{DD} = 1.35–1.65 V.

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