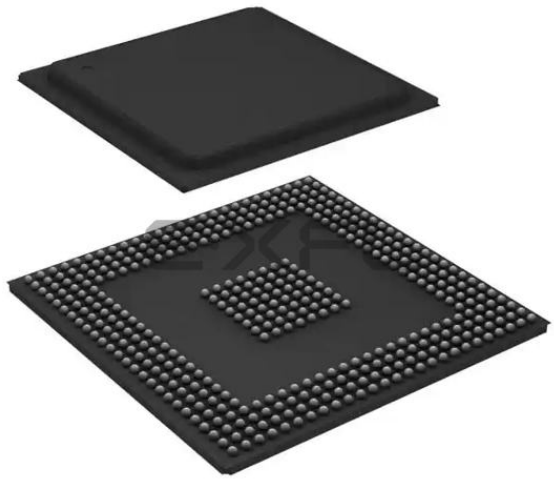

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Details	
Product Status	Not For New Designs
Core Processor	e200z6
Core Size	32-Bit Single-Core
Speed	132MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	256
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 40x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc5554mzp132

3 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MCU.

3.1 Maximum Ratings

Table 2. Absolute Maximum Ratings [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	1.5 V core supply voltage [2]	V_{DD}	–0.3	1.7	V
2	Flash program/erase voltage	V_{PP}	–0.3	6.5	V
4	Flash read voltage	V_{FLASH}	–0.3	4.6	V
5	SRAM standby voltage	V_{STBY}	–0.3	1.7	V
6	Clock synthesizer voltage	V_{DDSYN}	–0.3	4.6	V
7	3.3 V I/O buffer voltage	V_{DD33}	–0.3	4.6	V
8	Voltage regulator control input voltage	V_{RC33}	–0.3	4.6	V
9	Analog supply voltage (reference to V_{SSA})	V_{DDA}	–0.3	5.5	V
10	I/O supply voltage (fast I/O pads) [3]	V_{DDE}	–0.3	4.6	V
11	I/O supply voltage (slow and medium I/O pads) [3]	V_{DDEH}	–0.3	6.5	V
12	DC input voltage [4] V_{DDEH} powered I/O pads V_{DDE} powered I/O pads	V_{IN}	 –1.0 [5] –1.0 [5]	 6.5 [6] 4.6 [7]	V
13	Analog reference high voltage (reference to V_{RL})	V_{RH}	–0.3	5.5	V
14	V_{SS} to V_{SSA} differential voltage	$V_{SS} – V_{SSA}$	–0.1	0.1	V
15	V_{DD} to V_{DDA} differential voltage	$V_{DD} – V_{DDA}$	$–V_{DDA}$	V_{DD}	V
16	V_{REF} differential voltage	$V_{RH} – V_{RL}$	–0.3	5.5	V
17	V_{RH} to V_{DDA} differential voltage	$V_{RH} – V_{DDA}$	–5.5	5.5	V
18	V_{RL} to V_{SSA} differential voltage	$V_{RL} – V_{SSA}$	–0.3	0.3	V
19	V_{DDEH} to V_{DDA} differential voltage	$V_{DDEH} – V_{DDA}$	$–V_{DDA}$	V_{DDEH}	V
20	V_{DDF} to V_{DD} differential voltage	$V_{DDF} – V_{DD}$	–0.3	0.3	V
21	V_{RC33} to V_{DDSYN} differential voltage spec has been moved to Table 9 DC Electrical Specifications, Spec 43a.				
22	V_{SSSYN} to V_{SS} differential voltage	$V_{SSSYN} – V_{SS}$	–0.1	0.1	V
23	V_{RCVSS} to V_{SS} differential voltage	$V_{RCVSS} – V_{SS}$	–0.1	0.1	V
24	Maximum DC digital input current [8] (per pin, applies to all digital pins) [4]	I_{MAXD}	–2	2	mA
25	Maximum DC analog input current [9] (per pin, applies to all analog pins)	I_{MAXA}	–3	3	mA
26	Maximum operating temperature range [10] Die junction temperature	T_J	T_L	150.0	°C
27	Storage temperature range	T_{STG}	–55.0	150.0	°C

3.5 ESD (Electromagnetic Static Discharge) Characteristics

Table 5. ESD Ratings [1, 2]

Characteristic	Symbol	Value	Unit
ESD for human body model (HBM)		2000	V
HBM circuit description	R1	1500	Ω
	C	100	pF
ESD for field induced charge model (FDCM)		500 (all pins) 750 (corner pins)	V
Number of pulses per pin: Positive pulses (HBM) Negative pulses (HBM)	 — —	 1 1	 — —
Interval of pulses	—	1	second

1 All ESD testing conforms to CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 Device failure is defined as: 'If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.

3.6 Voltage Regulator Controller (V_{RC}) and Power-On Reset (POR) Electrical Specifications

The following table lists the V_{RC} and POR electrical specifications:

Table 6. V_{RC} and POR Electrical Specifications

Spec	Characteristic		Symbol	Min.	Max.	Units
1	1.5 V (V_{DD}) POR [1]	Negated (ramp up) Asserted (ramp down)	V_{POR15}	1.1 1.1	1.35 1.35	V
2	3.3 V (V_{DDSYN}) POR [1]	Asserted (ramp up) Negated (ramp up) Asserted (ramp down) Negated (ramp down)	V_{POR33}	0.0 2.0 2.0 0.0	0.30 2.85 2.85 0.30	V
3	$\overline{\text{RESET}}$ pin supply (V_{DDEH6}) POR [1, 2]	Negated (ramp up) Asserted (ramp down)	V_{POR5}	2.0 2.0	2.85 2.85	V
4	V_{RC33} voltage	Before V_{RC} allows the pass transistor to start turning on	V_{TRANS_START}	1.0	2.0	V
5		When V_{RC} allows the pass transistor to completely turn on [3, 4]	V_{TRANS_ON}	2.0	2.85	V
6		When the voltage is greater than the voltage at which the V_{RC} keeps the 1.5 V supply in regulation [5, 6]	$V_{VRC33REG}$	3.0	—	V
		– 55° C [7]		11.0	—	mA
7	Current can be sourced by V_{RCCTL} at Tj:	–40° C 25° C 150° C	I_{VRCCTL} [8]	11.0 9.0 7.5	— — —	mA mA mA

3.7.1 Input Value of Pins During POR Dependent on V_{DD33}

When powering up the device, V_{DD33} must not lag the latest V_{DDSYN} *or* $\overline{\text{RESET}}$ power pin (V_{DDEH6}) by more than the V_{DD33} lag specification listed in Table 6, spec 8. This avoids accidentally selecting the bypass clock mode because the internal versions of PLLCFG[0:1] and $\overline{\text{RSTCFG}}$ are not powered and therefore cannot read the default state when POR negates. V_{DD33} can lag V_{DDSYN} *or* the $\overline{\text{RESET}}$ power pin (V_{DDEH6}), but cannot lag both by more than the V_{DD33} lag specification. This V_{DD33} lag specification applies during power up only. V_{DD33} has no lead or lag requirements when powering down.

3.7.2 Power-Up Sequence (V_{RC33} Grounded)

The 1.5 V V_{DD} power supply must rise to 1.35 V before the 3.3 V V_{DDSYN} power supply and the $\overline{\text{RESET}}$ power supply rises above 2.0 V. This ensures that digital logic in the PLL for the 1.5 V power supply does not begin to operate below the specified operation range lower limit of 1.35 V. Because the internal 1.5 V POR is disabled, the internal 3.3 V POR or the $\overline{\text{RESET}}$ power POR must hold the device in reset. Since they can negate as low as 2.0 V, V_{DD} must be within specification before the 3.3 V POR and the $\overline{\text{RESET}}$ POR negate.

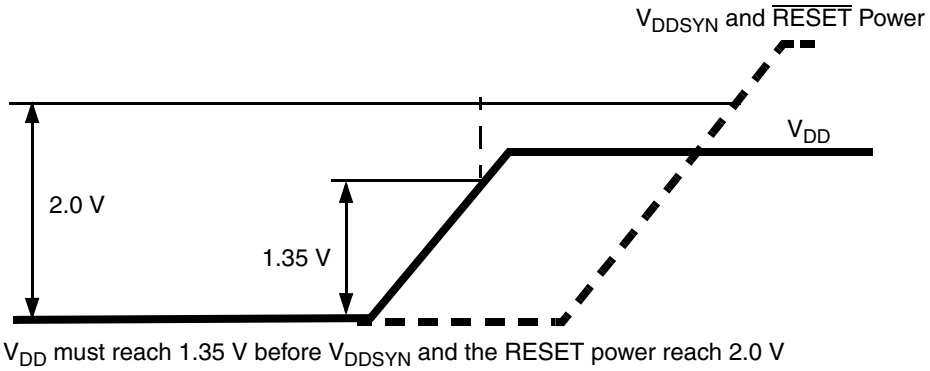


Figure 3. Power-Up Sequence (V_{RC33} Grounded)

3.7.3 Power-Down Sequence (V_{RC33} Grounded)

The only requirement for the power-down sequence with V_{RC33} grounded is if V_{DD} decreases to less than its operating range, V_{DDSYN} or the $\overline{\text{RESET}}$ power must decrease to less than 2.0 V before the V_{DD} power increases to its operating range. This ensures that the digital 1.5 V logic, which is reset only by an ORed POR and can cause the 1.5 V supply to decrease less than its specification value, resets correctly. See Table 6, footnote 1.

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
27a	Operating Current 1.5 V Supplies @ 132 MHz: [6]				
	V_{DD} (including V_{DDF} max current) @1.65 V typical use [7, 8]	I_{DD}	—	700	mA
	V_{DD} (including V_{DDF} max current) @1.4 V typical use [7, 8]	I_{DD}	—	600	mA
	V_{DD} (including V_{DDF} max current) @1.65 V high use [8, 9]	I_{DD}	—	875	mA
	V_{DD} (including V_{DDF} max current) @1.4 V high use [8, 9]	I_{DD}	—	740	mA
27b	Operating Current 1.5 V Supplies @ 114 MHz: [6]				
	V_{DD} (including V_{DDF} max current) @1.65 V typical use [7, 8]	I_{DD}	—	609	mA
	V_{DD} (including V_{DDF} max current) @1.4 V typical use [7, 8]	I_{DD}	—	522	mA
	V_{DD} (including V_{DDF} max current) @1.65 V high use [8, 9]	I_{DD}	—	760	mA
	V_{DD} (including V_{DDF} max current) @1.4 V high use [8, 9]	I_{DD}	—	643	mA
27c	Operating Current 1.5 V Supplies @ 82 MHz: [6]				
	V_{DD} (including V_{DDF} max current) @1.65 V typical use [7, 8]	I_{DD}	—	446	mA
	V_{DD} (including V_{DDF} max current) @1.40 V typical use [7, 8]	I_{DD}	—	384	mA
	V_{DD} (including V_{DDF} max current) @1.65 V high use [8, 9]	I_{DD}	—	555	mA
	V_{DD} (including V_{DDF} max current) @1.40 V high use [8, 9]	I_{DD}	—	471	mA
27d	RAM standby current.[10]				
	I_{DD_STBY} @ 25° C				
	V_{STBY} @ 0.8 V	I_{DD_STBY}	—	20	µA
	V_{STBY} @ 1.0 V	I_{DD_STBY}	—	30	µA
	V_{STBY} @ 1.2 V	I_{DD_STBY}	—	50	µA
	I_{DD_STBY} @ 60° C				
	V_{STBY} @ 0.8 V	I_{DD_STBY}	—	70	µA
	V_{STBY} @ 1.0 V	I_{DD_STBY}	—	100	µA
	V_{STBY} @ 1.2 V	I_{DD_STBY}	—	200	µA
	I_{DD_STBY} @ 150° C (Tj)				
	V_{STBY} @ 0.8 V	I_{DD_STBY}	—	1200	µA
	V_{STBY} @ 1.0 V	I_{DD_STBY}	—	1500	µA
	V_{STBY} @ 1.2 V	I_{DD_STBY}	—	2000	µA
28	Operating current 3.3 V supplies @ f_{MAX} MHz				
	V_{DD33} [11]	I_{DD_33}	—	2 + (values derived from procedure of footnote [11])	mA
	V_{FLASH}	I_{VFLASH}	—	10	mA
	V_{DDSYN}	I_{DDSYN}	—	15	mA
29	Operating current 5.0 V supplies (12 MHz ADCLK):				
	V_{DDA} (V_{DDA0} + V_{DDA1})	I_{DD_A}	—	20.0	mA
	Analog reference supply current (V_{RH}, V_{RL})	I_{REF}	—	1.0	mA
	V_{PP}	I_{PP}	—	25.0	mA

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
30	Operating current V_{DDE} supplies: [12] V_{DDEH1} V_{DDE2} V_{DDE3} V_{DDEH4} V_{DDE5} V_{DDEH6} V_{DDE7} V_{DDEH8} V_{DDEH9}	 I_{DD1} I_{DD2} I_{DD3} I_{DD4} I_{DD5} I_{DD6} I_{DD7} I_{DD8} I_{DD9}	 — — — — — — — — —	 Refer to footnote [12]	 mA mA mA mA mA mA mA mA mA
31	Fast I/O weak pullup current [13] 1.62–1.98 V 2.25–2.75 V 3.00–3.60 V	I_{ACT_F}	 10 20 20	 110 130 170	 µA µA µA
	Fast I/O weak pulldown current [13] 1.62–1.98 V 2.25–2.75 V 3.00–3.60 V		 10 20 20	 100 130 170	 µA µA µA
32	Slow and medium I/O weak pullup/down current [13] 3.0–3.6 V 4.5–5.5 V	I_{ACT_S}	 10 20	 150 170	 µA µA
33	I/O input leakage current [14]	I_{INACT_D}	–2.5	2.5	µA
34	DC injection current (per pin)	I_{IC}	–2.0	2.0	mA
35	Analog input current, channel off [15]	I_{INACT_A}	–150	150	nA
35a	Analog input current, shared analog / digital pins (AN[12], AN[13], AN[14], AN[15])	I_{INACT_AD}	–2.5	2.5	µA
36	V_{SS} to V_{SSA} differential voltage [16]	$V_{SS} - V_{SSA}$	–100	100	mV
37	Analog reference low voltage	V_{RL}	$V_{SSA} - 0.1$	$V_{SSA} + 0.1$	V
38	V_{RL} differential voltage	$V_{RL} - V_{SSA}$	–100	100	mV
39	Analog reference high voltage	V_{RH}	$V_{DDA} - 0.1$	$V_{DDA} + 0.1$	V
40	V_{REF} differential voltage	$V_{RH} - V_{RL}$	4.5	5.25	V
41	V_{SSSYN} to V_{SS} differential voltage	$V_{SSSYN} - V_{SS}$	–50	50	mV
42	V_{RCVSS} to V_{SS} differential voltage	$V_{RCVSS} - V_{SS}$	–50	50	mV
43	V_{DDF} to V_{DD} differential voltage	$V_{DDF} - V_{DD}$	–100	100	mV
43a	V_{RC33} to V_{DDSYN} differential voltage	$V_{RC33} - V_{DDSYN}$	–0.1	0.1 [17]	V
44	Analog input differential signal range (with common mode 2.5 V)	V_{IDIFF}	–2.5	2.5	V
45	Operating temperature range, ambient (packaged)	$T_A = (T_L$ to $T_H)$	T_L	T_H	°C
46	Slew rate on power-supply pins	—	—	50	V/ms

1 V_{DDE2} and V_{DDE3} are limited to 2.25–3.6 V only if SIU_ECCR[EBTS] = 0; V_{DDE2} and V_{DDE3} have a range of 1.6–3.6 V if SIU_ECCR[EBTS] = 1.

[2] $| V_{DDA0} - V_{DDA1} |$ must be < 0.1 V.

[3] V_{PP} can drop to 3.0 V during read operations.

[4] If standby operation is not required, connect V_{STBY} to ground.

[5] Applies to CLKOUT, external bus pins, and Nexus pins.

[6] Maximum average RMS DC current.

[7] Average current measured on automotive benchmark.

[8] Peak currents can be higher on specialized code.

[9] High use current measured while running optimized SPE assembly code with all code and data 100% locked in cache (0% miss rate) with all channels of the eMIOS and eTPU running autonomously, plus the eDMA transferring data continuously from SRAM to SRAM. Higher currents are possible if an “idle” loop that crosses cache lines is run from cache. Write code that avoids this condition.

[10] The current specification relates to average standby operation after SRAM has been loaded with data. For power up current see Section 3.7, “Power-Up/Down Sequencing”, Figure 2.

[11] Power requirements for the V_{DD33} supply depend on the frequency of operation, load of all I/O pins, and the voltages on the I/O segments. Refer to Table 11 for values to calculate the power dissipation for a specific operation.

[12] Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. Refer to Table 10 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

[13] Absolute value of current, measured at V_{IL} and V_{IH}.

[14] Weak pullup/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to pad types: pad_fc, pad_sh, and pad_mh.

[15] Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 ^{o}C to 12 ^{o}C, in the ambient temperature range of 50 ^{o}C to 125 ^{o}C. Applies to pad types: pad_a and pad_ae.

[16] V_{SSA} refers to both V_{SSA0} and V_{SSA1}. $| V_{SSA0} - V_{SSA1} |$ must be < 0.1 V.

[17] Up to 0.6 V during power up and power down.

3.8.1 I/O Pad Current Specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a segment. The output pin current can be calculated from Table 10 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 10.

Table 10. I/O Pad Average DC Current ($T_A = T_L$ to T_H)[1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Drive Select / Slew Rate Control Setting	Current (mA)
1	Slow	I_{DRV_SH}	25	50	5.25	11	8.0
2			10	50	5.25	01	3.2
3			2	50	5.25	00	0.7
4			2	200	5.25	00	2.4
5	Medium	I_{DRV_MH}	50	50	5.25	11	17.3
6			20	50	5.25	01	6.5
7			3.33	50	5.25	00	1.1
8			3.33	200	5.25	00	3.9
9	Fast	I_{DRV_FC}	66	10	3.6	00	2.8
10			66	20	3.6	01	5.2
11			66	30	3.6	10	8.5
12			66	50	3.6	11	11.0
13			66	10	1.98	00	1.6
14			66	20	1.98	01	2.9
15			66	30	1.98	10	4.2
16			66	50	1.98	11	6.7
17			56	10	3.6	00	2.4
18			56	20	3.6	01	4.4
19			56	30	3.6	10	7.2
20			56	50	3.6	11	9.3
21			56	10	1.98	00	1.3
22			56	20	1.98	01	2.5
23			56	30	1.98	10	3.5
24			56	50	1.98	11	5.7
25			40	10	3.6	00	1.7
26			40	20	3.6	01	3.1
27			40	30	3.6	10	5.1
28			40	50	3.6	11	6.6
29			40	10	1.98	00	1.0
30			40	20	1.98	01	1.8
31			40	30	1.98	10	2.5
32			40	50	1.98	11	4.0

1 These values are estimates from simulation and are not tested. Currents apply to output pins only.

2 All loads are lumped.

3.8.2 I/O Pad V_{DD33} Current Specifications

The power consumption of the V_{DD33} supply dependents on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{DD33} currents for all I/O segments. The output pin V_{DD33} current can be calculated from Table 11 based on the voltage, frequency, and load on all fast (pad_fc) pins. The input pin V_{DD33} current can be calculated from Table 11 based on the voltage, frequency, and load on all pad_sh and pad_mh pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 11.

Table 11. V_{DD33} Pad Average DC Current ($T_A = T_L$ to T_H) [1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load [2] (pF)	V_{DD33} (V)	V_{DDE} (V)	Drive Select	Current (mA)
Inputs								
1	Slow	I_{33_SH}	66	0.5	3.6	5.5	NA	0.003
2	Medium	I_{33_MH}	66	0.5	3.6	5.5	NA	0.003
Outputs								
3	Fast	I_{33_FC}	66	10	3.6	3.6	00	0.35
4			66	20	3.6	3.6	01	0.53
5			66	30	3.6	3.6	10	0.62
6			66	50	3.6	3.6	11	0.79
7			66	10	3.6	1.98	00	0.35
8			66	20	3.6	1.98	01	0.44
9			66	30	3.6	1.98	10	0.53
10			66	50	3.6	1.98	11	0.70
11			56	10	3.6	3.6	00	0.30
12			56	20	3.6	3.6	01	0.45
13			56	30	3.6	3.6	10	0.52
14			56	50	3.6	3.6	11	0.67
15			56	10	3.6	1.98	00	0.30
16			56	20	3.6	1.98	01	0.37
17			56	30	3.6	1.98	10	0.45
18			56	50	3.6	1.98	11	0.60
19			40	10	3.6	3.6	00	0.21
20			40	20	3.6	3.6	01	0.31
21			40	30	3.6	3.6	10	0.37
22			40	50	3.6	3.6	11	0.48
23			40	10	3.6	1.98	00	0.21
24			40	20	3.6	1.98	01	0.27
25			40	30	3.6	1.98	10	0.32
26			40	50	3.6	1.98	11	0.42

1 These values are estimated from simulation and not tested. Currents apply to output pins for the fast pads only and to input pins for the slow and medium pads only.

2 All loads are lumped.

3.9 Oscillator and FMPLL Electrical Characteristics

Table 12. FMPLL Electrical Specifications

(V_{DDSYN} = 3.0–3.6 V; V_{SS} = V_{SSSYN} = 0.0 V; T_A = T_L to T_H)

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
1	PLL reference frequency range: [1] Crystal reference External reference Dual controller (1:1 mode)	 $f_{ref\_crystal}$ f_{ref_ext} $f_{ref\_1:1}$	 8 8 24	 20 20 $f_{sys} \div 2$	MHz
2	System frequency [2]	f_{sys}	$f_{ICO(MIN)} \div 2^{RFD}$	f_{MAX} [3]	MHz
3	System clock period	t_{CYC}	—	$1 \div f_{sys}$	ns
4	Loss of reference frequency [4]	f_{LOR}	100	1000	kHz
5	Self-clocked mode (SCM) frequency [5]	f_{SCM}	7.4	17.5	MHz
6	EXTAL input high voltage crystal mode [6] All other modes [dual controller (1:1), bypass, external reference]	V_{IHEXT} V_{IHEXT}	V_{XTAL} + 0.4 V ($V_{DDE5} \div 2$) + 0.4 V	— —	V V
7	EXTAL input low voltage crystal mode [7] All other modes [dual controller (1:1), bypass, external reference]	V_{ILEXT} V_{ILEXT}	— —	V_{XTAL} – 0.4 V ($V_{DDE5} \div 2$) – 0.4 V	V V
8	XTAL current [8]	I_{XTAL}	0.8	3	mA
9	Total on-chip stray capacitance on XTAL	C_{S_XTAL}	—	1.5	pF
10	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
11	Crystal manufacturer's recommended capacitive load	C_L	Refer to crystal specification	Refer to crystal specification	pF
12	Discrete load capacitance to connect to EXTAL	C_{L_EXTAL}	—	$(2 \times C_L) - C_{S\_EXTAL} - C_{PCB\_EXTAL}$ [9]	pF
13	Discrete load capacitance to connect to XTAL	C_{L_XTAL}	—	$(2 \times C_L) - C_{S\_XTAL} - C_{PCB\_XTAL}$ [9]	pF
14	PLL lock time [10]	t_{lpll}	—	750	µs
15	Dual controller (1:1) clock skew (between CLKOUT and EXTAL) [11, 12]	t_{skew}	–2	2	ns
16	Duty cycle of reference	t_{DC}	40	60	%
17	Frequency unLOCK range	f_{UL}	–4.0	4.0	% f_{SYS}
18	Frequency LOCK range	f_{LCK}	–2.0	2.0	% f_{SYS}

3.10 eQADC Electrical Characteristics

Table 13. eQADC Conversion Specifications ($T_A = T_L$ to T_H)

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
1	ADC clock (ADCLK) frequency [1]	F_{ADCLK}	1	12	MHz
2	Conversion cycles Differential Single ended	CC	 13 + 2 (15) 14 + 2 (16)	 13 + 128 (141) 14 + 128 (142)	ADCLK cycles
3	Stop mode recovery time [2]	T_{SR}	10	—	µs
4	Resolution [3]	—	1.25	—	mV
5	INL: 6 MHz ADC clock	INL6	–4	4	Counts [3]
6	INL: 12 MHz ADC clock	INL12	–8	8	Counts
7	DNL: 6 MHz ADC clock	DNL6	–3 [4]	3 [4]	Counts
8	DNL: 12 MHz ADC clock	DNL12	–6 [4]	6 [4]	Counts
9	Offset error with calibration	OFFWC	–4 [5]	4 [5]	Counts
10	Full-scale gain error with calibration	GAINWC	–8 [6]	8 [6]	Counts
11	Disruptive input injection current [7, 8, 9, 10]	I_{INJ}	–1	1	mA
12	Incremental error due to injection current. All channels are 10 kΩ < Rs <100 kΩ Channel under test has Rs = 10 kΩ, $I_{INJ} = I_{INJMAX}$, I_{INJMIN}	E_{INJ}	–4	4	Counts
13	Total unadjusted error (TUE) for single ended conversions with calibration [11, 12, 13, 14, 15]	TUE	–4	4	Counts

1 Conversion characteristics vary with F_{ADCLK} rate. Reduced conversion accuracy occurs at maximum F_{ADCLK} rate. The maximum value is based on 800 KS/s and the minimum value is based on 20 MHz oscillator clock frequency divided by a maximum 16 factor.

2 Stop mode recovery time begins when the ADC control register enable bits are set until the ADC is ready to perform conversions.

3 At $V_{RH} - V_{RL}$ = 5.12 V, one least significant bit (LSB) = 1.25, mV = one count.

4 Guaranteed 10-bit mono tonicity.

5 The absolute value of the offset error without calibration ≤ 100 counts.

6 The absolute value of the full scale gain error without calibration ≤ 120 counts.

7 Below disruptive current conditions, the channel being stressed has conversion values of: 0x3FF for analog inputs greater than V_{RH}, and 0x000 for values less than V_{RL}. This assumes that $V_{RH} \leq V_{DDA}$ and $V_{RL} \geq V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.

8 Exceeding the limit can cause a conversion error on both stressed and unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

9 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA}$ + 0.5 V and $V_{NEGCLAMP}$ = – 0.3 V, then use the larger of the calculated values.

10 This condition applies to two adjacent pads on the internal pad.

11 The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to canceling errors.

12 TUE does not apply to differential conversions.

13 Measured at 6 MHz ADC clock. TUE with a 12 MHz ADC clock is: –16 counts < TUE < 16 counts.

14 TUE includes all internal device errors such as internal reference variation (75% Ref, 25% Ref).

15 Depending on the input impedance, the analog input leakage current (Table 9. DC Electrical Specifications, spec 35a) can affect the actual TUE measured on analog channels AN[12], AN[13], AN[14], AN[15].

3.13.3 Nexus Timing

Table 21. Nexus Debug Port Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	MCKO cycle time	t_{MCYC}	2[2]	8	t_{CYC}
2	MCKO duty cycle	t_{MDC}	40	60	%
3	MCKO low to MDO data valid [3]	t_{MDOV}	–1.5	3.0	ns
4	MCKO low to $\overline{\text{MSEO}}$ data valid [3]	t_{MSEOV}	–1.5	3.0	ns
5	MCKO low to $\overline{\text{EVTO}}$ data valid [3]	t_{EVTOV}	–1.5	3.0	ns
6	$\overline{\text{EVTI}}$ pulse width	t_{EVTIPW}	4.0	—	t_{TCYC}
7	$\overline{\text{EVTO}}$ pulse width	t_{EVTOPW}	1	—	t_{MCYC}
8	TCK cycle time	t_{TCYC}	4 [4]	—	t_{CYC}
9	TCK duty cycle	t_{TDC}	40	60	%
10	TDI, TMS data setup time	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS data hold time	t_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK low to TDO data valid V_{DDE} = 2.25–3.0 V V_{DDE} = 3.0–3.6 V	t_{JOV}	 0 0	 12 10	 ns ns
13	$\overline{\text{RDY}}$ valid to MCKO [5]	—	—	—	—

1 JTAG specifications apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.35–1.65 V, V_{DDE} = 2.25–3.6 V, V_{DD33} and V_{DDSYN} = 3.0–3.6 V, T_A = T_L to T_H, and CL = 30 pF with DSC = 0b10.

2 The Nexus AUX port runs up to 82 MHz.

3 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until the next MCKO low cycle occurs.

4 Limit the maximum frequency to approximately 16 MHz (V_{DDE} = 2.25–3.0 V) or 20 MHz (V_{DDE} = 3.0–3.6 V) to meet the timing specification for t_{JOV} of [0.2 x t_{JCYC}] as outlined in the IEEE-ISTO 5001-2003 specification.

5 The $\overline{\text{RDY}}$ pin timing is asynchronous to MCKO and is guaranteed by design to function correctly.

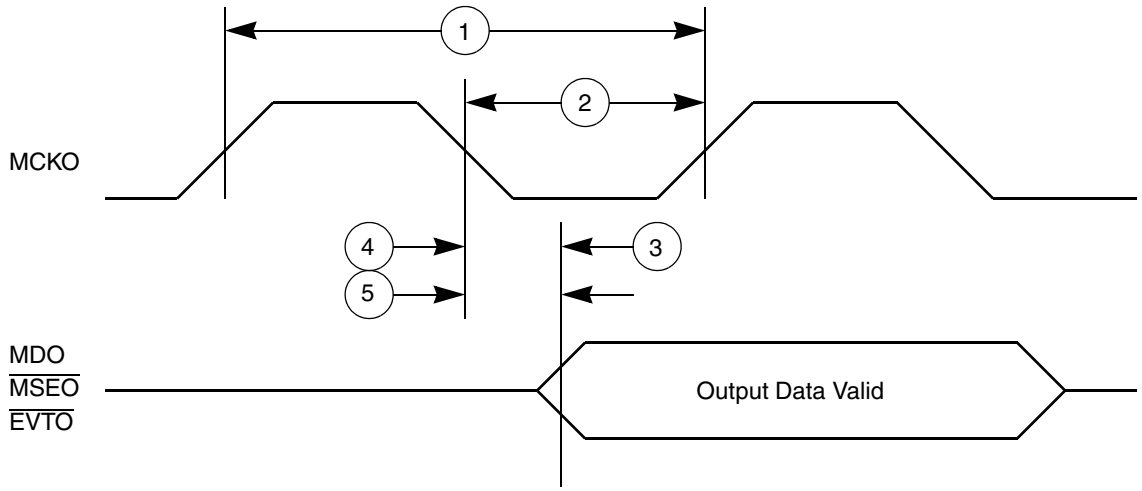


Figure 10. Nexus Output Timing

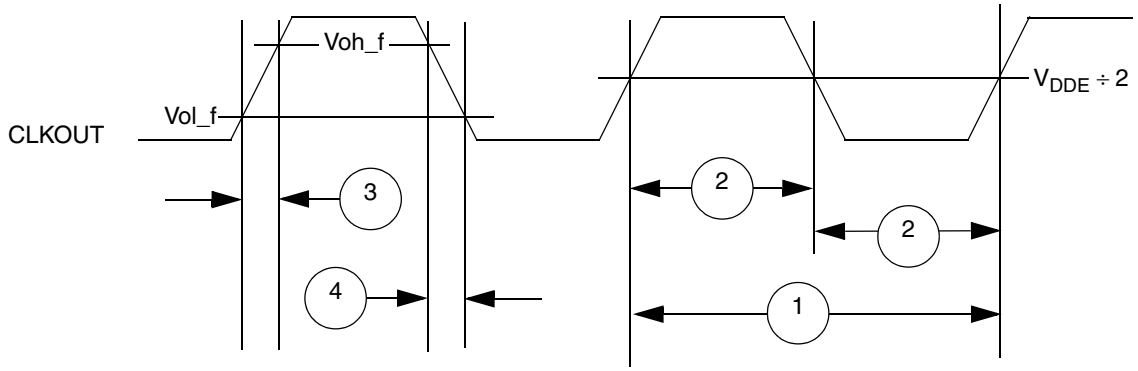


Figure 12. CLKOUT Timing

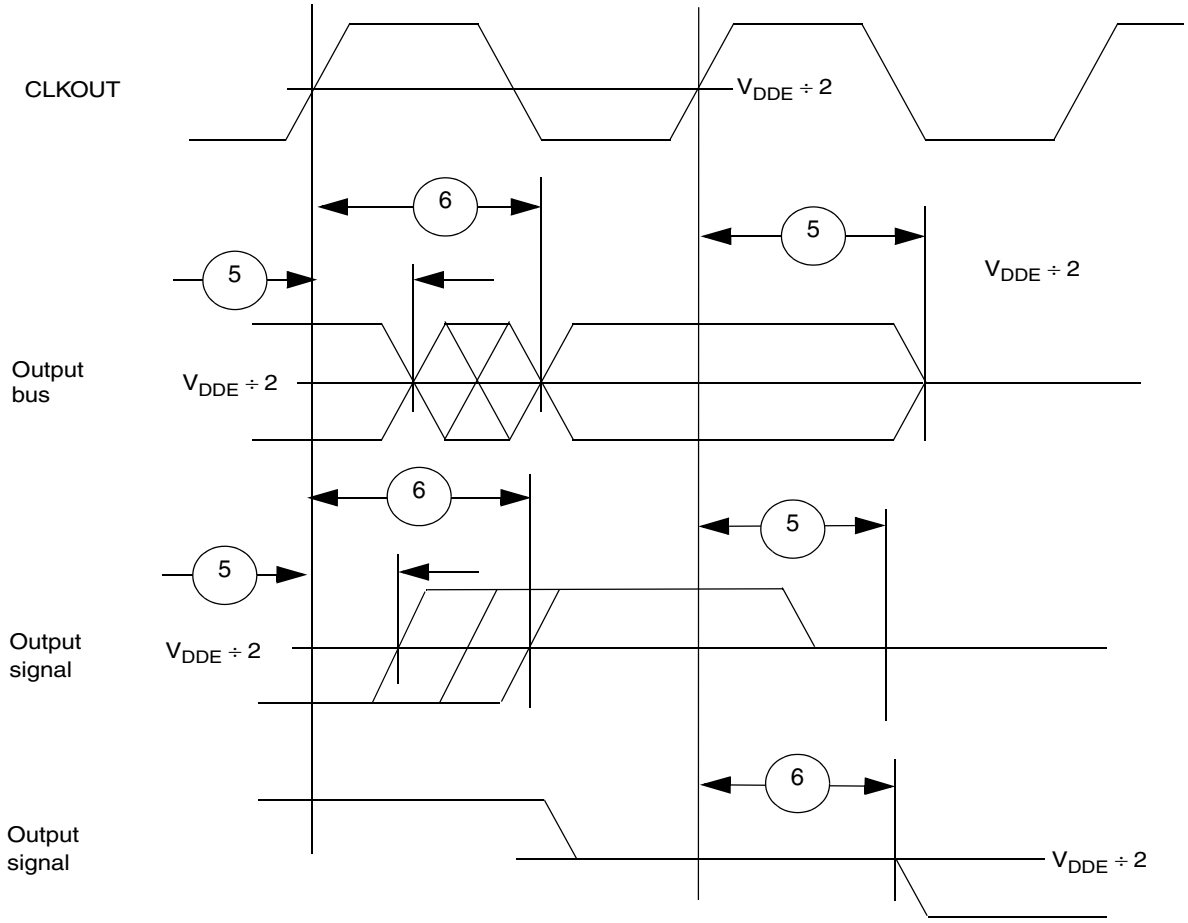


Figure 13. Synchronous Output Timing

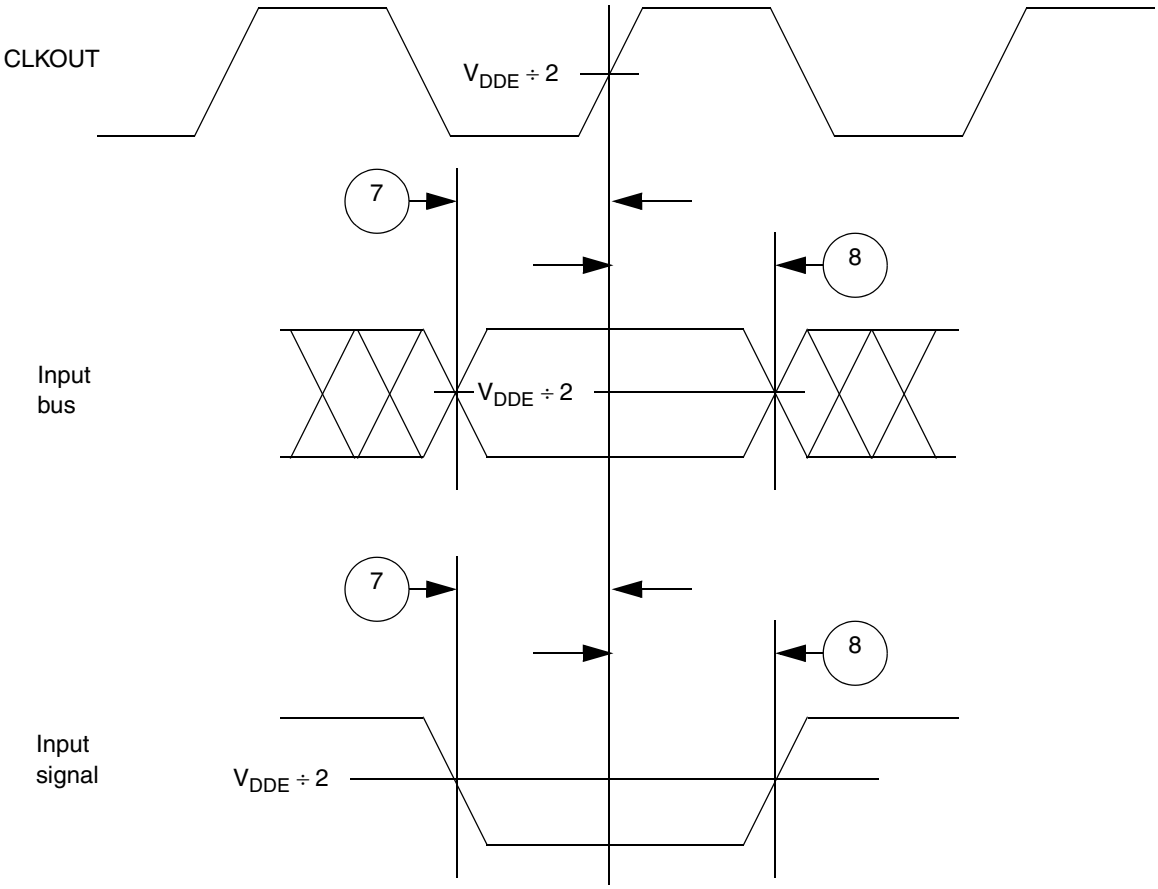


Figure 14. Synchronous Input Timing

3.13.5 External Interrupt Timing (IRQ Signals)

Table 23. External Interrupt Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	IRQ pulse-width low	t_{IPWL}	3	—	t_{CYC}
2	IRQ pulse-width high	T_{IPWH}	3	—	t_{CYC}
3	IRQ edge-to-edge time [2]	t_{ICYC}	6	—	t_{CYC}

[1] IRQ timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

[2] Applies when IRQ signals are configured for rising-edge or falling-edge events, but not both.

3.13.7 eMIOS Timing

Table 25. eMIOS Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	eMIOS input pulse width	t_{MIPW}	4	—	t_{CYC}
2	eMIOS output pulse width	t_{MOPW}	1 [2]	—	t_{CYC}

1 eMIOS timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

2 This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control field (SRC) in the pad configuration register (PCR).

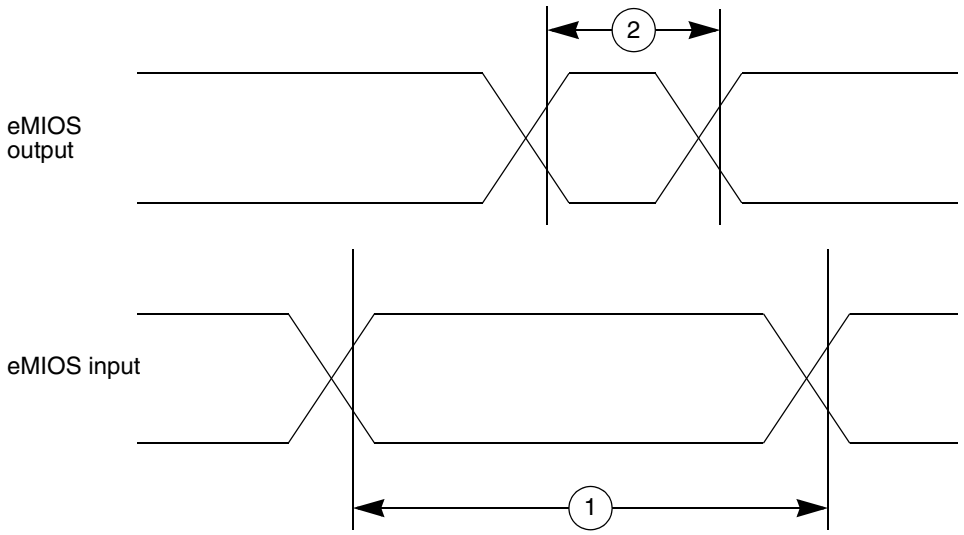


Figure 17. eMIOS Timing

3.13.8 DSPI Timing

Table 26. DSPI Timing[1, 2]

Spec	Characteristic	Symbol	80 MHz		112 MHz		132 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	SCK cycle time[3, 4]	t_{SCK}	24.4 ns	2.9 ms	17.5 ns	2.1 ms	15.2 ns	1.7 ms	—
2	PCS to SCK delay[5]	t_{CSC}	23	—	15	—	13	—	ns
3	After SCK delay[6]	t_{ASC}	22	—	14	—	12	—	ns
4	SCK duty cycle	t_{SDC}	($t_{SCK} \div 2$) – 2 ns	($t_{SCK} \div 2$) + 2 ns	($t_{SCK} \div 2$) – 2 ns	($t_{SCK} \div 2$) + 2 ns	($t_{SCK} \div 2$) – 2 ns	($t_{SCK} \div 2$) + 2 ns	ns
5	Slave access time ($\overline{SS}$ active to SOUT driven)	t_A	—	25	—	25	—	25	ns
6	Slave SOUT disable time ($\overline{SS}$ inactive to SOUT Hi-Z, or invalid)	t_{DIS}	—	25	—	25	—	25	ns
7	PCS*x* to $\overline{PCSS}$ time	t_{PCSC}	4	—	4	—	4	—	ns
8	$\overline{PCSS}$ to PCS*x* time	t_{PASC}	5	—	5	—	5	—	ns

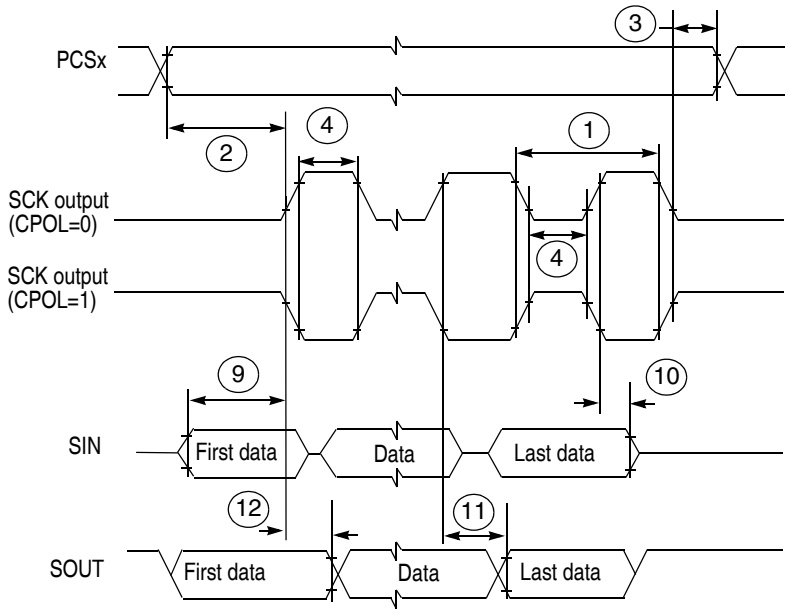


Figure 22. DSPI Modified Transfer Format Timing—Master, CPHA = 0

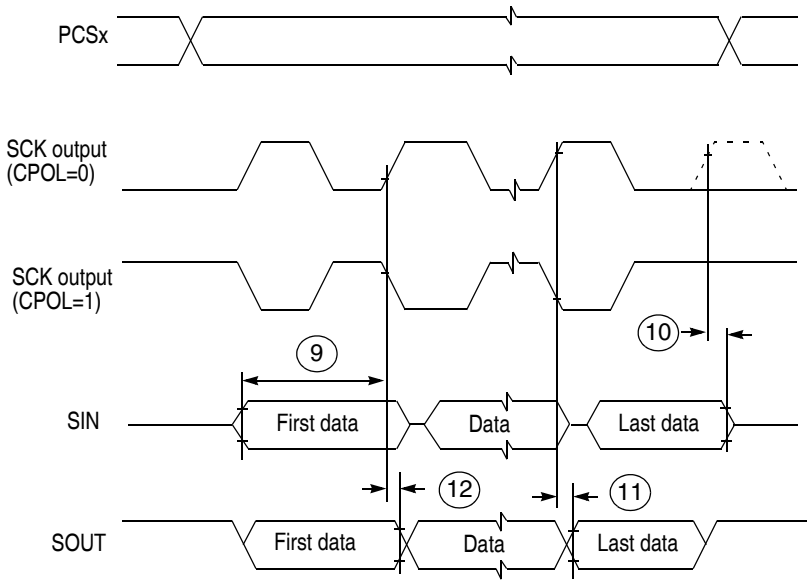
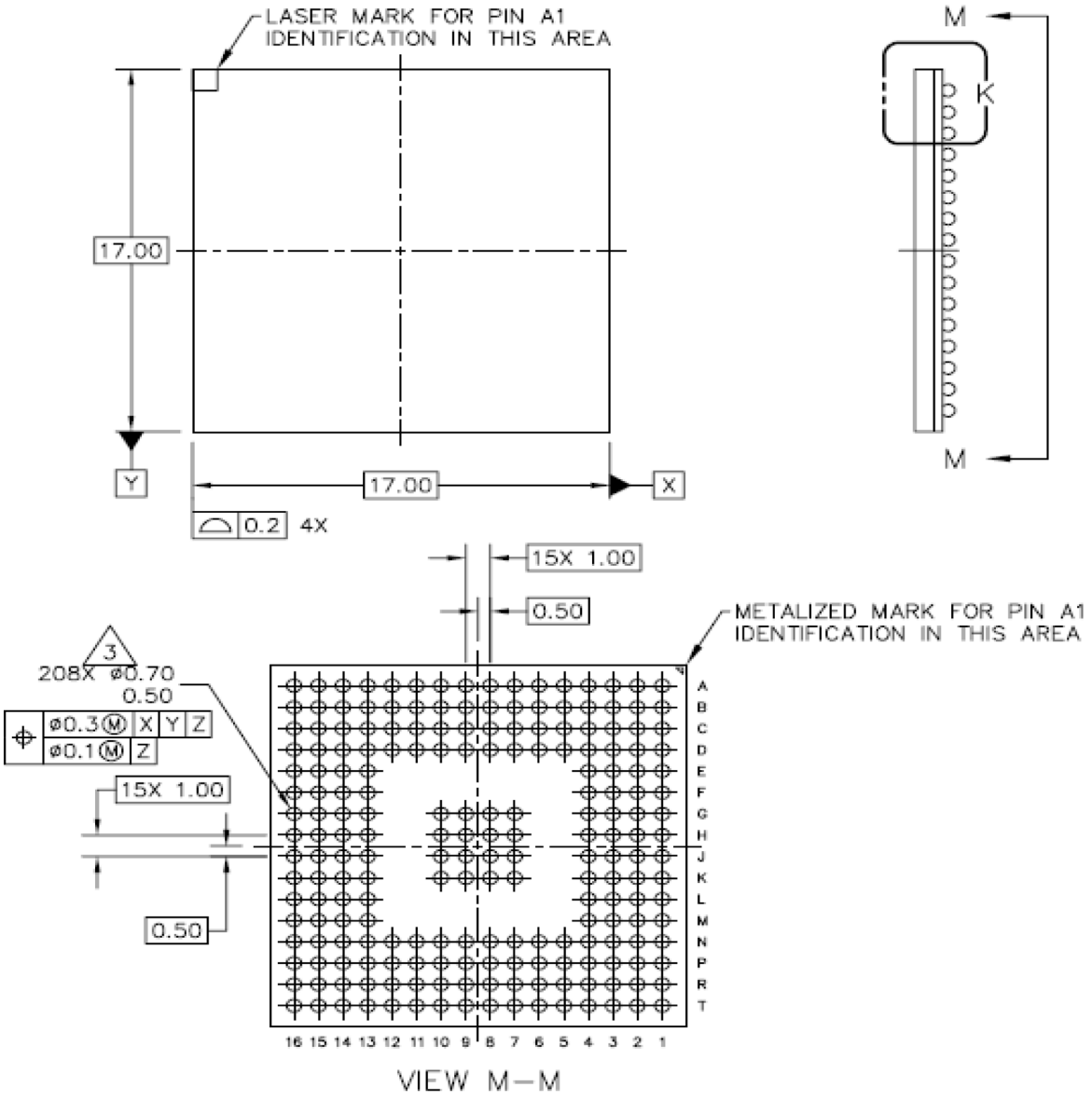


Figure 23. DSPI Modified Transfer Format Timing—Master, CPHA = 1

The package drawings of the MPC55 208-pin MAP BGA are shown below.



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TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	DOCUMENT NO: 98ARS23882W	REV: D
	CASE NUMBER: 1159A–01	02 AUG 2005
	STANDARD: JEDEC MO–151 AAF–1	

Figure 32. 208-Pin Package

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

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TITLE: 416 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)	DOCUMENT NO: 98ARE10523D	REV: A
	CASE NUMBER: 1494–01	13 JUL 2005
	STANDARD: JEDEC MS–034 AAL–1	

Figure 34. MPC5554 416 TEPBGA Package (continued)

5 Revision History for the MPC5554 Data Sheet

The history of revisions made to this data sheet are described in this section.

5.1 Changes between Revision 3 and Revision 4

Location	Description of Changes
Section 3.7, "Power-Up/Down Sequencing"	Added the following paragraph in Section 3.7, "Power-Up/Down Sequencing": "During initial power ramp-up, when Vstby is 0.6v or above. a typical current of 1-3mA and maximum of 4mA may be seen until VDD is applied. This current will not reoccur until Vstby is lowered below Vstby min. specification".
	Moved Figure 2 (fISTBY Worst-case Specifications) "ISTBY Worst-case Specifications" to Section 3.7, "Power-Up/Down Sequencing".
Section 3.8, "DC Electrical Specifications"	Removed the footnote "Figure 3 shows an illustration of the IDD_STBY values interpolated for these temperature values".
	Changed the footnote attached to IDD_STBY" to "The current specification relates to average standby operation after SRAM has been loaded with data. For power up current see Section 3.7, "Power-Up/Down Sequencing",Figure 2 (fISTBY Worst-case Specifications)."
	In Table 9 (DC Electrical Specifications ($T_A = T_L$ to T_H)) the Characteristic "Refer to Figure 3 for an interpolation of this data" changed to "RAM standby current".

5.2 Changes between Revision 2 and Revision 3

The substantive changes incorporated in MPC5554 Data Sheet Rev. 2.0 to produce Rev. 3.0 are listed in Table 28. The changes are listed in sequential page number order.

Table 28. Changes Between Rev. 2.0 and 3.0

Location	Description of Changes
Throughout:	
	Changed '$T_A = T_L - T_H$' to '$T_A = T_L$ to T_H.'
Title page:	
	Changed the Revision number from 2 to 3. Changed the date. Made the same change in the lower left corner of the back page.
Section 1, "Overview"	
	• Fourth paragraph, First sentence: Deleted 'of the MPC5500 family'; Second to last sentence: Deleted 'can'. • Fifth paragraph, First sentence: Replaced 'MPC5500 family' with 'MPC5554'; Last sentence: Replaced 'can be' with 'is'. • Sixth paragraph, First sentence: Replaced 'MPC5500 family' with 'MPC5554'; • Second to last paragraph: Rewrote to read: The MCU has an on-chip enhanced queued dual analog-to-digital converter (eQADC). The 416 package has 40-channels.
Section 3.2.1, "General Notes for Specifications at Maximum Junction Temperature	
	Updated the address of Semiconductor Equipment and Materials International 3081 Zanker Rd. San Jose, CA., 95134 (408) 943-6900

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