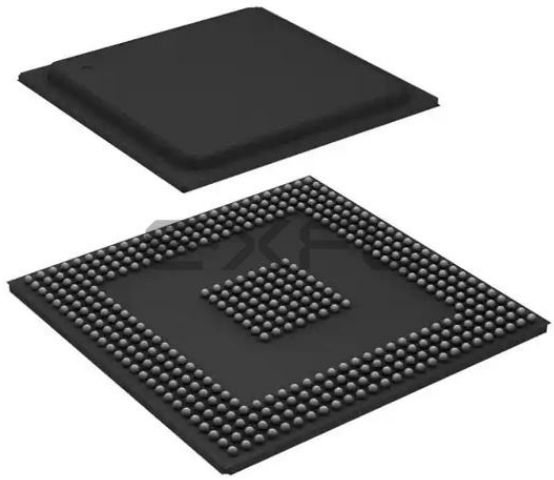

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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
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3 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MCU.

3.1 Maximum Ratings

Table 2. Absolute Maximum Ratings [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	1.5 V core supply voltage [2]	V_{DD}	–0.3	1.7	V
2	Flash program/erase voltage	V_{PP}	–0.3	6.5	V
4	Flash read voltage	V_{FLASH}	–0.3	4.6	V
5	SRAM standby voltage	V_{STBY}	–0.3	1.7	V
6	Clock synthesizer voltage	V_{DDSYN}	–0.3	4.6	V
7	3.3 V I/O buffer voltage	V_{DD33}	–0.3	4.6	V
8	Voltage regulator control input voltage	V_{RC33}	–0.3	4.6	V
9	Analog supply voltage (reference to V_{SSA})	V_{DDA}	–0.3	5.5	V
10	I/O supply voltage (fast I/O pads) [3]	V_{DDE}	–0.3	4.6	V
11	I/O supply voltage (slow and medium I/O pads) [3]	V_{DDEH}	–0.3	6.5	V
12	DC input voltage [4] V_{DDEH} powered I/O pads V_{DDE} powered I/O pads	V_{IN}	 –1.0 [5] –1.0 [5]	 6.5 [6] 4.6 [7]	V
13	Analog reference high voltage (reference to V_{RL})	V_{RH}	–0.3	5.5	V
14	V_{SS} to V_{SSA} differential voltage	$V_{SS} – V_{SSA}$	–0.1	0.1	V
15	V_{DD} to V_{DDA} differential voltage	$V_{DD} – V_{DDA}$	$–V_{DDA}$	V_{DD}	V
16	V_{REF} differential voltage	$V_{RH} – V_{RL}$	–0.3	5.5	V
17	V_{RH} to V_{DDA} differential voltage	$V_{RH} – V_{DDA}$	–5.5	5.5	V
18	V_{RL} to V_{SSA} differential voltage	$V_{RL} – V_{SSA}$	–0.3	0.3	V
19	V_{DDEH} to V_{DDA} differential voltage	$V_{DDEH} – V_{DDA}$	$–V_{DDA}$	V_{DDEH}	V
20	V_{DDF} to V_{DD} differential voltage	$V_{DDF} – V_{DD}$	–0.3	0.3	V
21	V_{RC33} to V_{DDSYN} differential voltage spec has been moved to Table 9 DC Electrical Specifications, Spec 43a.				
22	V_{SSSYN} to V_{SS} differential voltage	$V_{SSSYN} – V_{SS}$	–0.1	0.1	V
23	V_{RCVSS} to V_{SS} differential voltage	$V_{RCVSS} – V_{SS}$	–0.1	0.1	V
24	Maximum DC digital input current [8] (per pin, applies to all digital pins) [4]	I_{MAXD}	–2	2	mA
25	Maximum DC analog input current [9] (per pin, applies to all analog pins)	I_{MAXA}	–3	3	mA
26	Maximum operating temperature range [10] Die junction temperature	T_J	T_L	150.0	°C
27	Storage temperature range	T_{STG}	–55.0	150.0	°C

3.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the device junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

Table 6. V_{RC} and POR Electrical Specifications (continued)

Spec	Characteristic		Symbol	Min.	Max.	Units
8	Voltage differential during power up such that: V_{DD33} can lag V_{DDSYN} or V_{DDEH6} before V_{DDSYN} and V_{DDEH6} reach the V_{POR33} and V_{POR5} minimums respectively.		V_{DD33_LAG}	—	1.0	V
9	Absolute value of slew rate on power supply pins		—	—	50	V/ms
10	Required gain at Tj: $I_{DD} \div I_{VRCCTL}$ (@ $f_{sys} = f_{MAX}$)[6, 8, 9, 10]	– 55° C[7]	BETA[11]	70	—	—
		– 40° C		70	—	—
		25° C		85[11]	—	—
		150° C		105[11]	500	—

1 The internal POR signals are V_{POR15}, V_{POR33}, and V_{POR5}. On power up, assert $\overline{\text{RESET}}$ before the internal POR negates. $\overline{\text{RESET}}$ must remain asserted until the power supplies are within the operating conditions as specified in Table 9 DC Electrical Specifications. On power down, assert $\overline{\text{RESET}}$ before any power supplies fall outside the operating conditions and until the internal POR asserts.

2 V_{IL_S} (Table 9, Spec15) is guaranteed to scale with V_{DDEH6} down to V_{POR5}.

3 Supply full operating current for the 1.5 V supply when the 3.3 V supply reaches this range.

4 It is possible to reach the current limit during ramp up—do not treat this event as short circuit current.

5 At peak current for device.

6 Requires compliance with Freescale's recommended board requirements and transistor recommendations. Board signal traces/routing from the V_{RCCTL} package signal to the base of the external pass transistor and between the emitter of the pass transistor to the V_{DD} package signals must have a maximum of 100 nH inductance and minimal resistance (less than 1 Ω). V_{RCCTL} must have a nominal 1 μF phase compensation capacitor to ground. V_{DD} must have a 20 μF (nominal) bulk capacitor (greater than 4 μF over all conditions, including lifetime). Place high-frequency bypass capacitors consisting of eight 0.01 μF, two 0.1 μF, and one 1 μF capacitors around the package on the V_{DD} supply signals.

7 Only available on devices that support -55° C.

8 I_{VRCCTL} is measured at the following conditions: V_{DD} = 1.35 V, V_{RC33} = 3.1 V, V_{VRCCTL} = 2.2 V.

9 Refer to Table 1 for the maximum operating frequency.

10 Values are based on I_{DD} from high-use applications as explained in the I_{DD} Electrical Specification.

11 BETA represents the worst-case external transistor. It is measured on a per-part basis and calculated as ($I_{DD} \div I_{VRCCTL}$).

3.7 Power-Up/Down Sequencing

Power sequencing between the 1.5 V power supply and V_{DDSYN} or the $\overline{\text{RESET}}$ power supplies is required if using an external 1.5 V power supply with V_{RC33} tied to ground (GND). To avoid power-sequencing, V_{RC33} must be powered up within the specified operating range, even if the on-chip voltage regulator controller is not used. Refer to Section 3.7.2, "Power-Up Sequence (VRC33 Grounded)," and Section 3.7.3, "Power-Down Sequence (VRC33 Grounded)."

Power sequencing requires that V_{DD33} must reach a certain voltage where the values are read as ones before the POR signal negates. Refer to Section 3.7.1, "Input Value of Pins During POR Dependent on VDD33."

Although power sequencing is not required between V_{RC33} and V_{DDSYN} during power up, V_{RC33} must not lead V_{DDSYN} by more than 600 mV or lag by more than 100 mV for the V_{RC} stage turn-on to operate within specification. Higher spikes in the emitter current of the pass transistor occur if V_{RC33} leads or lags V_{DDSYN} by more than these amounts. The value of that higher spike in current depends on the board power supply circuitry and the amount of board level capacitance.

Furthermore, when all of the PORs negate, the system clock starts to toggle, adding another large increase of the current consumed by V_{RC33}. If V_{RC33} lags V_{DDSYN} by more than 100 mV, the increase in current consumed can drop V_{DD} low enough to assert the 1.5 V POR again. Oscillations are possible when the 1.5 V POR asserts and stops the system clock, causing the voltage on V_{DD} to rise until the 1.5 V POR negates again. All oscillations stop when V_{RC33} is powered sufficiently.

When powering down, V_{RC33} and V_{DDSYN} have no delta requirement to each other, because the bypass capacitors internal and external to the device are already charged. When not powering up or down, no delta between V_{RC33} and V_{DDSYN} is required for the V_{RC} to operate within specification.

There are no power up/down sequencing requirements to prevent issues such as latch-up, excessive current spikes, and so on. Therefore, the state of the I/O pins during power up and power down varies depending on which supplies are powered.

Table 7 gives the pin state for the sequence cases for all pins with pad type pad_fc (fast type).

Table 7. Pin Status for Fast Pads During the Power Sequence

V_{DDE}	V_{DD33}	V_{DD}	POR	Pin Status for Fast Pad Output Driver pad_fc (fast)
Low	—	—	Asserted	Low
V_{DDE}	Low	Low	Asserted	High
V_{DDE}	Low	V_{DD}	Asserted	High
V_{DDE}	V_{DD33}	Low	Asserted	High impedance (Hi-Z)
V_{DDE}	V_{DD33}	V_{DD}	Asserted	Hi-Z
V_{DDE}	V_{DD33}	V_{DD}	Negated	Functional

Table 8 gives the pin state for the sequence cases for all pins with pad type pad_mh (medium type) and pad_sh (slow type).

Table 8. Pin Status for Medium and Slow Pads During the Power Sequence

V_{DDEH}	V_{DD}	POR	Pin Status for Medium and Slow Pad Output Driver pad_mh (medium) pad_sh (slow)
Low	—	Asserted	Low
V_{DDEH}	Low	Asserted	High impedance (Hi-Z)
V_{DDEH}	V_{DD}	Asserted	Hi-Z
V_{DDEH}	V_{DD}	Negated	Functional

The values in Table 7 and Table 8 do not include the effect of the weak-pull devices on the output pins during power up.

Before exiting the internal POR state, the voltage on the pins go to a high-impedance state until POR negates. When the internal POR negates, the functional state of the signal during reset applies and the weak-pull devices
(up or down) are enabled as defined in the device reference manual. If V_{DD} is too low to correctly propagate the logic signals, the weak-pull devices can pull the signals to V_{DDE} and V_{DDEH}.

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
27a	Operating Current 1.5 V Supplies @ 132 MHz: [6]				
	V_{DD} (including V_{DDF} max current) @1.65 V typical use [7, 8]	I_{DD}	—	700	mA
	V_{DD} (including V_{DDF} max current) @1.4 V typical use [7, 8]	I_{DD}	—	600	mA
	V_{DD} (including V_{DDF} max current) @1.65 V high use [8, 9]	I_{DD}	—	875	mA
	V_{DD} (including V_{DDF} max current) @1.4 V high use [8, 9]	I_{DD}	—	740	mA
27b	Operating Current 1.5 V Supplies @ 114 MHz: [6]				
	V_{DD} (including V_{DDF} max current) @1.65 V typical use [7, 8]	I_{DD}	—	609	mA
	V_{DD} (including V_{DDF} max current) @1.4 V typical use [7, 8]	I_{DD}	—	522	mA
	V_{DD} (including V_{DDF} max current) @1.65 V high use [8, 9]	I_{DD}	—	760	mA
	V_{DD} (including V_{DDF} max current) @1.4 V high use [8, 9]	I_{DD}	—	643	mA
27c	Operating Current 1.5 V Supplies @ 82 MHz: [6]				
	V_{DD} (including V_{DDF} max current) @1.65 V typical use [7, 8]	I_{DD}	—	446	mA
	V_{DD} (including V_{DDF} max current) @1.40 V typical use [7, 8]	I_{DD}	—	384	mA
	V_{DD} (including V_{DDF} max current) @1.65 V high use [8, 9]	I_{DD}	—	555	mA
	V_{DD} (including V_{DDF} max current) @1.40 V high use [8, 9]	I_{DD}	—	471	mA
27d	RAM standby current.[10]				
	I_{DD_STBY} @ 25° C				
	V_{STBY} @ 0.8 V	I_{DD_STBY}	—	20	µA
	V_{STBY} @ 1.0 V	I_{DD_STBY}	—	30	µA
	V_{STBY} @ 1.2 V	I_{DD_STBY}	—	50	µA
	I_{DD_STBY} @ 60° C				
	V_{STBY} @ 0.8 V	I_{DD_STBY}	—	70	µA
	V_{STBY} @ 1.0 V	I_{DD_STBY}	—	100	µA
	V_{STBY} @ 1.2 V	I_{DD_STBY}	—	200	µA
	I_{DD_STBY} @ 150° C (Tj)				
	V_{STBY} @ 0.8 V	I_{DD_STBY}	—	1200	µA
	V_{STBY} @ 1.0 V	I_{DD_STBY}	—	1500	µA
	V_{STBY} @ 1.2 V	I_{DD_STBY}	—	2000	µA
28	Operating current 3.3 V supplies @ f_{MAX} MHz				
	V_{DD33} [11]	I_{DD_33}	—	2 + (values derived from procedure of footnote [11])	mA
	V_{FLASH}	I_{VFLASH}	—	10	mA
	V_{DDSYN}	I_{DDSYN}	—	15	mA
29	Operating current 5.0 V supplies (12 MHz ADCLK):				
	V_{DDA} (V_{DDA0} + V_{DDA1})	I_{DD_A}	—	20.0	mA
	Analog reference supply current (V_{RH}, V_{RL})	I_{REF}	—	1.0	mA
	V_{PP}	I_{PP}	—	25.0	mA

3.8.2 I/O Pad V_{DD33} Current Specifications

The power consumption of the V_{DD33} supply dependents on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{DD33} currents for all I/O segments. The output pin V_{DD33} current can be calculated from Table 11 based on the voltage, frequency, and load on all fast (pad_fc) pins. The input pin V_{DD33} current can be calculated from Table 11 based on the voltage, frequency, and load on all pad_sh and pad_mh pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 11.

Table 11. V_{DD33} Pad Average DC Current ($T_A = T_L$ to T_H) [1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load [2] (pF)	V_{DD33} (V)	V_{DDE} (V)	Drive Select	Current (mA)
Inputs								
1	Slow	I_{33_SH}	66	0.5	3.6	5.5	NA	0.003
2	Medium	I_{33_MH}	66	0.5	3.6	5.5	NA	0.003
Outputs								
3	Fast	I_{33_FC}	66	10	3.6	3.6	00	0.35
4			66	20	3.6	3.6	01	0.53
5			66	30	3.6	3.6	10	0.62
6			66	50	3.6	3.6	11	0.79
7			66	10	3.6	1.98	00	0.35
8			66	20	3.6	1.98	01	0.44
9			66	30	3.6	1.98	10	0.53
10			66	50	3.6	1.98	11	0.70
11			56	10	3.6	3.6	00	0.30
12			56	20	3.6	3.6	01	0.45
13			56	30	3.6	3.6	10	0.52
14			56	50	3.6	3.6	11	0.67
15			56	10	3.6	1.98	00	0.30
16			56	20	3.6	1.98	01	0.37
17			56	30	3.6	1.98	10	0.45
18			56	50	3.6	1.98	11	0.60
19			40	10	3.6	3.6	00	0.21
20			40	20	3.6	3.6	01	0.31
21			40	30	3.6	3.6	10	0.37
22			40	50	3.6	3.6	11	0.48
23			40	10	3.6	1.98	00	0.21
24			40	20	3.6	1.98	01	0.27
25			40	30	3.6	1.98	10	0.32
26			40	50	3.6	1.98	11	0.42

1 These values are estimated from simulation and not tested. Currents apply to output pins for the fast pads only and to input pins for the slow and medium pads only.

2 All loads are lumped.

3.9 Oscillator and FMPLL Electrical Characteristics

Table 12. FMPLL Electrical Specifications

(V_{DDSYN} = 3.0–3.6 V; V_{SS} = V_{SSSYN} = 0.0 V; T_A = T_L to T_H)

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
1	PLL reference frequency range: [1] Crystal reference External reference Dual controller (1:1 mode)	 $f_{ref\_crystal}$ f_{ref_ext} $f_{ref\_1:1}$	 8 8 24	 20 20 $f_{sys} \div 2$	MHz
2	System frequency [2]	f_{sys}	$f_{ICO(MIN)} \div 2^{RFD}$	f_{MAX} [3]	MHz
3	System clock period	t_{CYC}	—	$1 \div f_{sys}$	ns
4	Loss of reference frequency [4]	f_{LOR}	100	1000	kHz
5	Self-clocked mode (SCM) frequency [5]	f_{SCM}	7.4	17.5	MHz
6	EXTAL input high voltage crystal mode [6] All other modes [dual controller (1:1), bypass, external reference]	V_{IHEXT} V_{IHEXT}	V_{XTAL} + 0.4 V ($V_{DDE5} \div 2$) + 0.4 V	— —	V V
7	EXTAL input low voltage crystal mode [7] All other modes [dual controller (1:1), bypass, external reference]	V_{ILEXT} V_{ILEXT}	— —	V_{XTAL} – 0.4 V ($V_{DDE5} \div 2$) – 0.4 V	V V
8	XTAL current [8]	I_{XTAL}	0.8	3	mA
9	Total on-chip stray capacitance on XTAL	C_{S_XTAL}	—	1.5	pF
10	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
11	Crystal manufacturer's recommended capacitive load	C_L	Refer to crystal specification	Refer to crystal specification	pF
12	Discrete load capacitance to connect to EXTAL	C_{L_EXTAL}	—	$(2 \times C_L) - C_{S\_EXTAL} - C_{PCB\_EXTAL}$ [9]	pF
13	Discrete load capacitance to connect to XTAL	C_{L_XTAL}	—	$(2 \times C_L) - C_{S\_XTAL} - C_{PCB\_XTAL}$ [9]	pF
14	PLL lock time [10]	t_{lpll}	—	750	µs
15	Dual controller (1:1) clock skew (between CLKOUT and EXTAL) [11, 12]	t_{skew}	–2	2	ns
16	Duty cycle of reference	t_{DC}	40	60	%
17	Frequency unLOCK range	f_{UL}	–4.0	4.0	% f_{SYS}
18	Frequency LOCK range	f_{LCK}	–2.0	2.0	% f_{SYS}

Table 12. FMPLL Electrical Specifications (continued)

(V_{DDSYN} = 3.0–3.6 V; V_{SS} = V_{SSSYN} = 0.0 V; T_A = T_L to T_H)

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
19	CLKOUT period jitter, measured at f_{SYS} max: [13, 14] Peak-to-peak jitter (clock edge to clock edge) Long term jitter (averaged over a 2 ms interval)	C_{JITTER}	 — —	 5.0 0.01	% f_{CLKOUT}
20	Frequency modulation range limit [15] (do not exceed f_{sys} maximum)	C_{MOD}	0.8	2.4	$\%f_{SYS}$
21	ICO frequency $f_{ico} = [f_{ref\_crystal} \times (MFD + 4)] \div (PREDIV + 1)$ [16] $f_{ico} = [f_{ref\_ext} \times (MFD + 4)] \div (PREDIV + 1)$	f_{ico}	48	f_{MAX}	MHz
22	Predivider output frequency (to PLL)	f_{PREDIV}	4	20 [17]	MHz

1 Nominal crystal and external reference values are worst-case not more than 1%. The device operates correctly if the frequency remains within ± 5% of the specification limit. This tolerance range allows for a slight frequency drift of the crystals over time. The designer must thoroughly understand the drift margin of the source clock.

2 All internal registers retain data at 0 Hz.

3 Up to the maximum frequency rating of the device (refer to Table 1).

4 Loss of reference frequency is defined as the reference frequency detected internally, which transitions the PLL into self-clocked mode.

5 The PLL operates at self-clocked mode (SCM) frequency when the reference frequency falls below f_{LOR}. SCM frequency is measured on the CLKOUT ball with the divider set to divide-by-two of the system clock.
NOTE: In SCM, the MFD and PREDIV have no effect and the RFD is bypassed.

6 Use the EXTAL input high voltage parameter when using the FlexCAN oscillator in crystal mode (no quartz crystals or resonators). ($V_{extal} - V_{xtal}$) must be ≥ 400 mV for the oscillator's comparator to produce the output clock.

7 Use the EXTAL input low voltage parameter when using the FlexCAN oscillator in crystal mode (no quartz crystals or resonators). ($V_{xtal} - V_{extal}$) must be ≥ 400 mV for the oscillator's comparator to produce the output clock.

8 I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

9 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

10 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, the lock time also includes the crystal startup time.

11 PLL is operating in 1:1 PLL mode.

12 V_{DDE} = 3.0–3.6 V.

13 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the jitter percentage for a given interval. CLKOUT divider is set to divide-by-two.

14 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of (jitter + Cmod).

15 Modulation depth selected must not result in f_{sys} value greater than the f_{sys} maximum specified value.

16 $f_{sys} = f_{ico} \div (2^{RFD})$.

17 Maximum value for dual controller (1:1) mode is ($f_{MAX} \div 2$) with the predivider set to 1 (FMPLL_SYNCR[PREDIV] = 0b001).

3.10 eQADC Electrical Characteristics

Table 13. eQADC Conversion Specifications ($T_A = T_L$ to T_H)

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
1	ADC clock (ADCLK) frequency [1]	F_{ADCLK}	1	12	MHz
2	Conversion cycles Differential Single ended	CC	 13 + 2 (15) 14 + 2 (16)	 13 + 128 (141) 14 + 128 (142)	ADCLK cycles
3	Stop mode recovery time [2]	T_{SR}	10	—	µs
4	Resolution [3]	—	1.25	—	mV
5	INL: 6 MHz ADC clock	INL6	–4	4	Counts [3]
6	INL: 12 MHz ADC clock	INL12	–8	8	Counts
7	DNL: 6 MHz ADC clock	DNL6	–3 [4]	3 [4]	Counts
8	DNL: 12 MHz ADC clock	DNL12	–6 [4]	6 [4]	Counts
9	Offset error with calibration	OFFWC	–4 [5]	4 [5]	Counts
10	Full-scale gain error with calibration	GAINWC	–8 [6]	8 [6]	Counts
11	Disruptive input injection current [7, 8, 9, 10]	I_{INJ}	–1	1	mA
12	Incremental error due to injection current. All channels are 10 kΩ < Rs <100 kΩ Channel under test has Rs = 10 kΩ, $I_{INJ} = I_{INJMAX}$, I_{INJMIN}	E_{INJ}	–4	4	Counts
13	Total unadjusted error (TUE) for single ended conversions with calibration [11, 12, 13, 14, 15]	TUE	–4	4	Counts

1 Conversion characteristics vary with F_{ADCLK} rate. Reduced conversion accuracy occurs at maximum F_{ADCLK} rate. The maximum value is based on 800 KS/s and the minimum value is based on 20 MHz oscillator clock frequency divided by a maximum 16 factor.

2 Stop mode recovery time begins when the ADC control register enable bits are set until the ADC is ready to perform conversions.

3 At $V_{RH} - V_{RL}$ = 5.12 V, one least significant bit (LSB) = 1.25, mV = one count.

4 Guaranteed 10-bit mono tonicity.

5 The absolute value of the offset error without calibration ≤ 100 counts.

6 The absolute value of the full scale gain error without calibration ≤ 120 counts.

7 Below disruptive current conditions, the channel being stressed has conversion values of: 0x3FF for analog inputs greater than V_{RH}, and 0x000 for values less than V_{RL}. This assumes that $V_{RH} \leq V_{DDA}$ and $V_{RL} \geq V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.

8 Exceeding the limit can cause a conversion error on both stressed and unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

9 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA}$ + 0.5 V and $V_{NEGCLAMP}$ = – 0.3 V, then use the larger of the calculated values.

10 This condition applies to two adjacent pads on the internal pad.

11 The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to canceling errors.

12 TUE does not apply to differential conversions.

13 Measured at 6 MHz ADC clock. TUE with a 12 MHz ADC clock is: –16 counts < TUE < 16 counts.

14 TUE includes all internal device errors such as internal reference variation (75% Ref, 25% Ref).

15 Depending on the input impedance, the analog input leakage current (Table 9. DC Electrical Specifications, spec 35a) can affect the actual TUE measured on analog channels AN[12], AN[13], AN[14], AN[15].

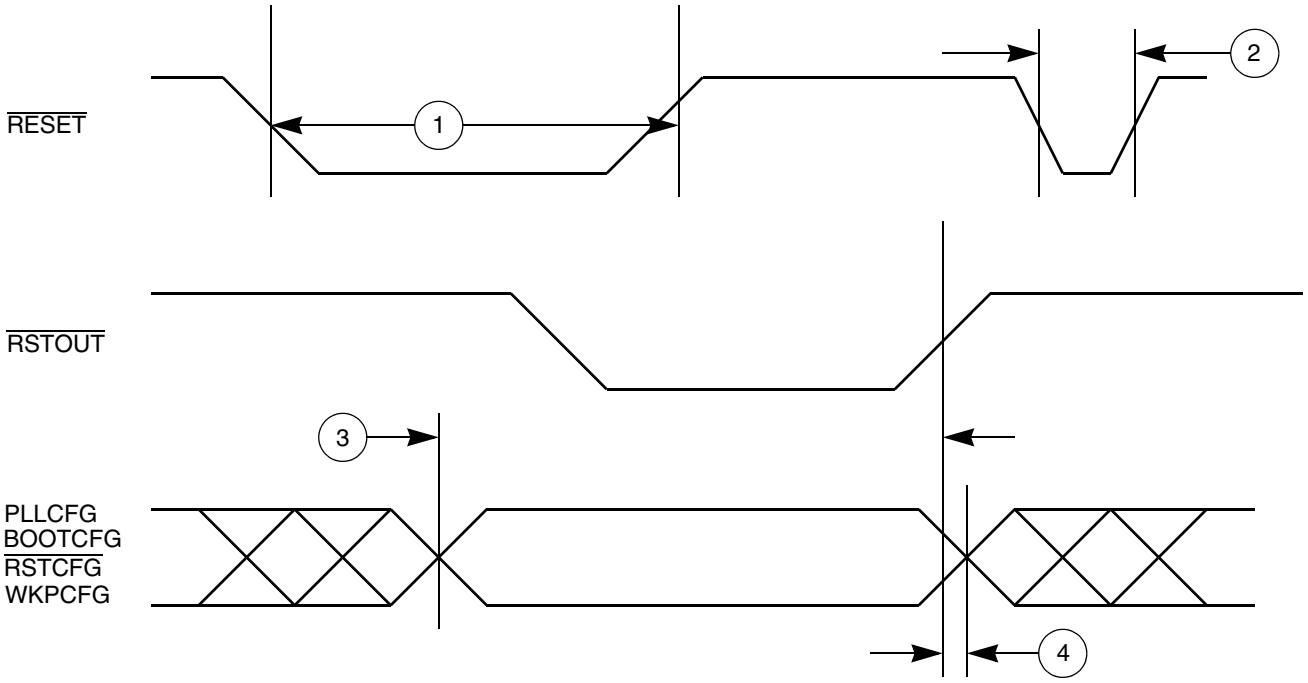


Figure 5. Reset and Configuration Pin Timing

3.13.2 IEEE 1149.1 Interface Timing

Table 20. JTAG Pin AC Electrical Characteristics [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	TCK cycle time	t_{JCYC}	100	—	ns
2	TCK clock pulse width (measured at $V_{DDE} \div 2$)	t_{JDC}	40	60	ns
3	TCK rise and fall times (40% to 70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI data setup time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI data hold time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK low to TDO data valid	t_{TDOV}	—	20	ns
7	TCK low to TDO data invalid	t_{TDOI}	0	—	ns
8	TCK low to TDO high impedance	t_{TDOHZ}	—	20	ns
9	JCOMP assertion time	t_{JCMPPW}	100	—	ns
10	JCOMP setup time to TCK low	t_{JCMPS}	40	—	ns
11	TCK falling-edge to output valid	t_{BSDV}	—	50	ns
12	TCK falling-edge to output valid out of high impedance	t_{BSDVZ}	—	50	ns
13	TCK falling-edge to output high impedance (Hi-Z)	t_{BSDHZ}	—	50	ns
14	Boundary scan input valid to TCK rising-edge	t_{BSDST}	50	—	ns
15	TCK rising-edge to boundary scan input invalid	t_{BSDHT}	50	—	ns

[1] These specifications apply to JTAG boundary scan only. JTAG timing specified at: V_{DDE} = 3.0–3.6 V and $T_A = T_L$ to T_H. Refer to Table 21 for Nexus specifications.

3.13.3 Nexus Timing

Table 21. Nexus Debug Port Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	MCKO cycle time	t_{MCYC}	2[2]	8	t_{CYC}
2	MCKO duty cycle	t_{MDC}	40	60	%
3	MCKO low to MDO data valid [3]	t_{MDOV}	–1.5	3.0	ns
4	MCKO low to $\overline{\text{MSEO}}$ data valid [3]	t_{MSEOV}	–1.5	3.0	ns
5	MCKO low to $\overline{\text{EVTO}}$ data valid [3]	t_{EVTOV}	–1.5	3.0	ns
6	$\overline{\text{EVTI}}$ pulse width	t_{EVTIPW}	4.0	—	t_{TCYC}
7	$\overline{\text{EVTO}}$ pulse width	t_{EVTOPW}	1	—	t_{MCYC}
8	TCK cycle time	t_{TCYC}	4 [4]	—	t_{CYC}
9	TCK duty cycle	t_{TDC}	40	60	%
10	TDI, TMS data setup time	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS data hold time	t_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK low to TDO data valid V_{DDE} = 2.25–3.0 V V_{DDE} = 3.0–3.6 V	t_{JOV}	 0 0	 12 10	 ns ns
13	$\overline{\text{RDY}}$ valid to MCKO [5]	—	—	—	—

1 JTAG specifications apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.35–1.65 V, V_{DDE} = 2.25–3.6 V, V_{DD33} and V_{DDSYN} = 3.0–3.6 V, T_A = T_L to T_H, and CL = 30 pF with DSC = 0b10.

2 The Nexus AUX port runs up to 82 MHz.

3 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until the next MCKO low cycle occurs.

4 Limit the maximum frequency to approximately 16 MHz (V_{DDE} = 2.25–3.0 V) or 20 MHz (V_{DDE} = 3.0–3.6 V) to meet the timing specification for t_{JOV} of [0.2 x t_{JCYC}] as outlined in the IEEE-ISTO 5001-2003 specification.

5 The $\overline{\text{RDY}}$ pin timing is asynchronous to MCKO and is guaranteed by design to function correctly.

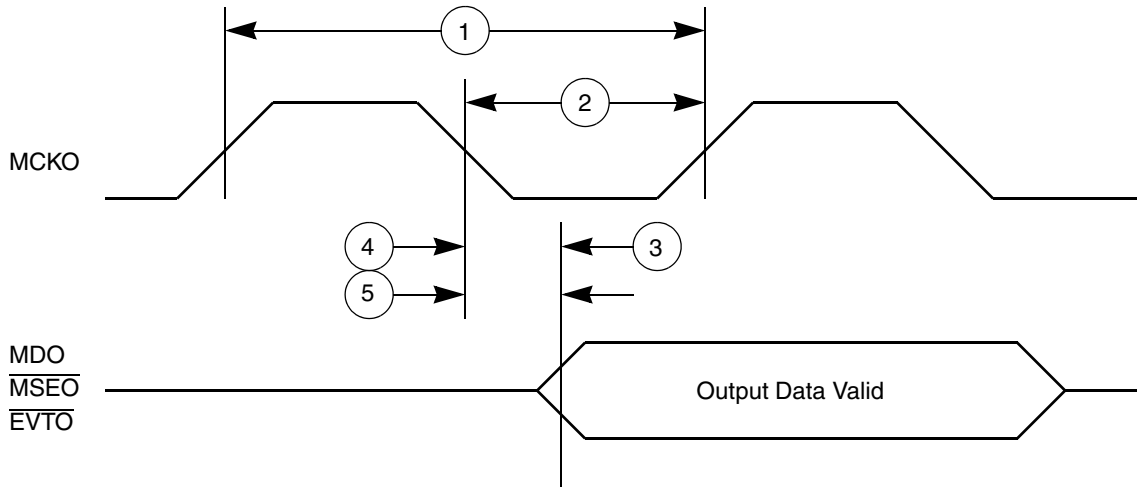


Figure 10. Nexus Output Timing

Table 22. Bus Operation Timing[1] (continued)

Spec	Characteristic and Description	Symbol	External Bus Frequency [2, 3]						Unit	Notes
			40 MHz		56 MHz		66 MHz			
			Min.	Max.	Min.	Max.	Min.	Max.		
7	Input signal *valid* to CLKOUT positive edge (setup time) External bus interface ADDR[8:31] DATA[0:31] [7] $\overline{BG}$ [6] $\overline{BR}$ [5] $\overline{BB}$ RD_$\overline{WR}$ $\overline{TA}$ $\overline{TEA}$ [8] $\overline{TS}$	t_{CIS}	10.0	—	7.0	—	5.0	—	ns	
8	CLKOUT positive edge to input signal *invalid* (hold time) External bus interface ADDR[8:31] DATA[0:31] [7] $\overline{BG}$ [6] $\overline{BR}$ [5] $\overline{BB}$ RD_$\overline{WR}$ $\overline{TA}$ $\overline{TEA}$ [8] $\overline{TS}$	t_{CIH}	1.0	—	1.0	—	1.0	—	ns	

1 EBI timing specified at: V_{DDE} = 1.6–3.6 V (unless stated otherwise); $T_A = T_L$ to T_H; and CL = 30 pF with DSC = 0b10.

2 Speed is the nominal maximum frequency. Max. speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; and 132 MHz parts allow for 128 MHz system clock + 2% FM.

3 The external bus is limited to half the speed of the internal bus.

4 Refer to fast pad timing in Table 17 and Table 18 (different values for 1.8 V and 3.3 V).

5 Internal arbitration.

6 External arbitration.

7 Due to pin limitations, the DATA[16:31] signals are not available on the 324 package.

8 Due to pin limitations, the $\overline{TEA}$ signal is not available on the 324 package.

9 Due to pin limitations, the $\overline{WE}$/$\overline{BE}$[2:3] signals are not available on the 324 package.

10 SIU_ECCR[EBTS] = 0 timings are tested and valid at V_{DDE} = 2.25–3.6 V only; SIU_ECCR[EBTS] = 1 timings are tested and valid at V_{DDE} = 1.6–3.6 V.

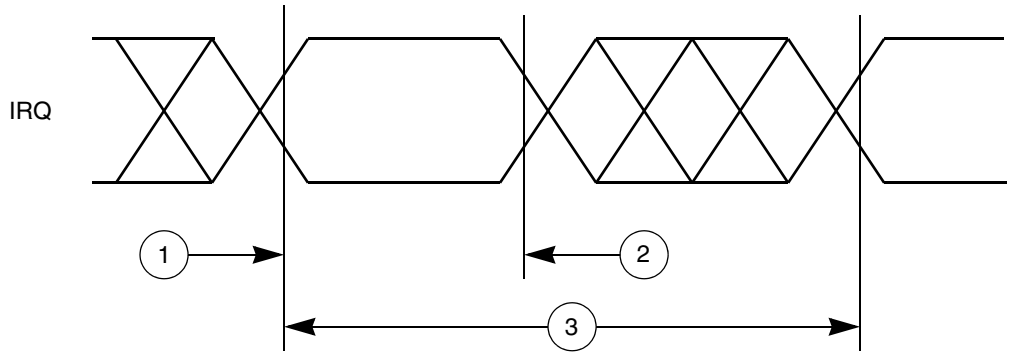


Figure 15. External Interrupt Timing

3.13.6 eTPU Timing

Table 24. eTPU Timing [1]

Spec	Characteristic	Symbol	Min.	Max	Unit
1	eTPU input channel pulse width	t_{ICPW}	4	—	t_{CYC}
2	eTPU output channel pulse width	t_{OCPW}	2 [2]	—	t_{CYC}

1 eTPU timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

2 This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

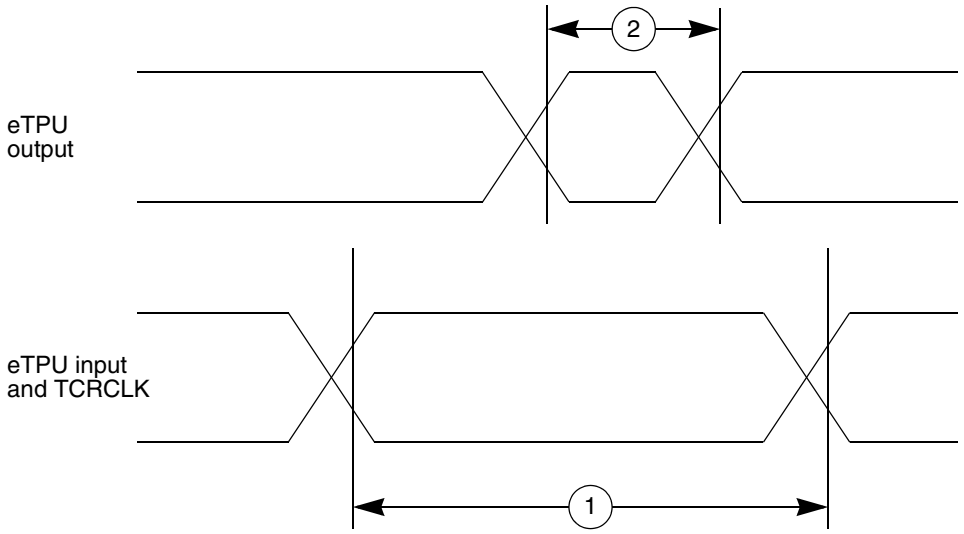


Figure 16. eTPU Timing

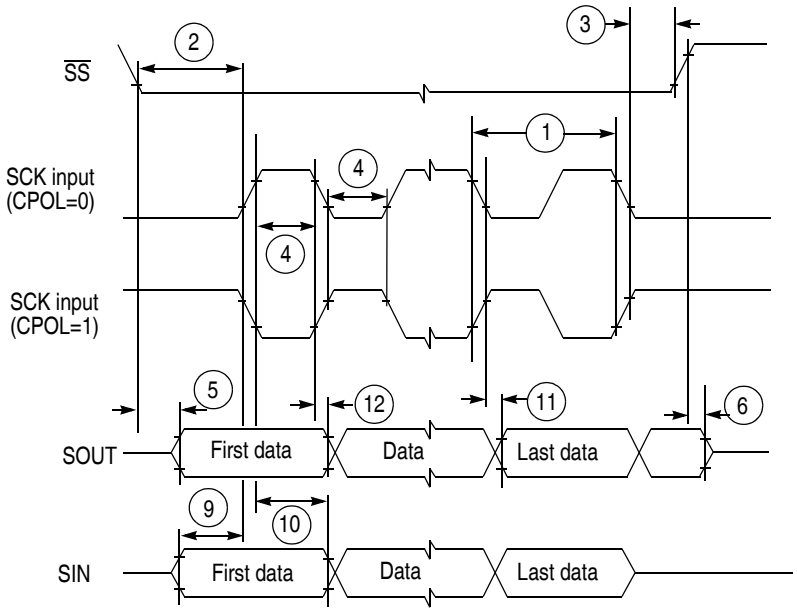


Figure 20. DSPI Classic SPI Timing—Slave, CPHA = 0

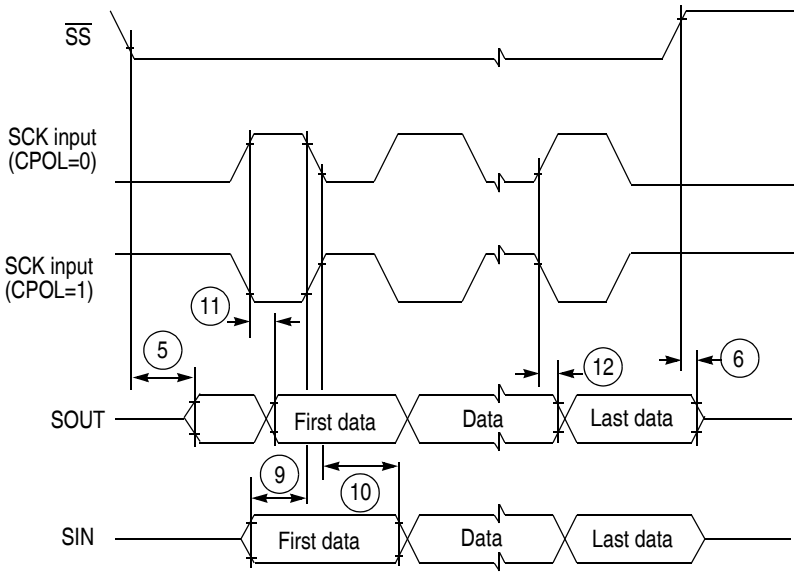


Figure 21. DSPI Classic SPI Timing—Slave, CPHA = 1

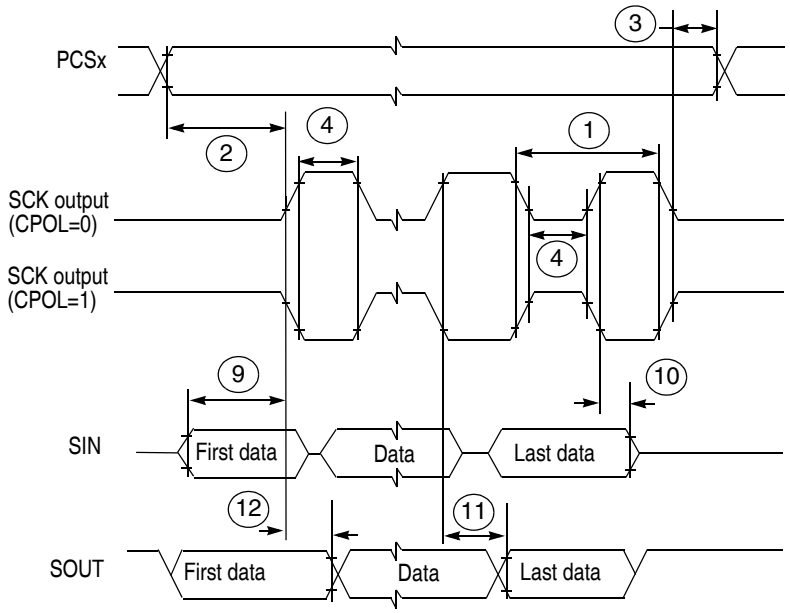


Figure 22. DSPI Modified Transfer Format Timing—Master, CPHA = 0

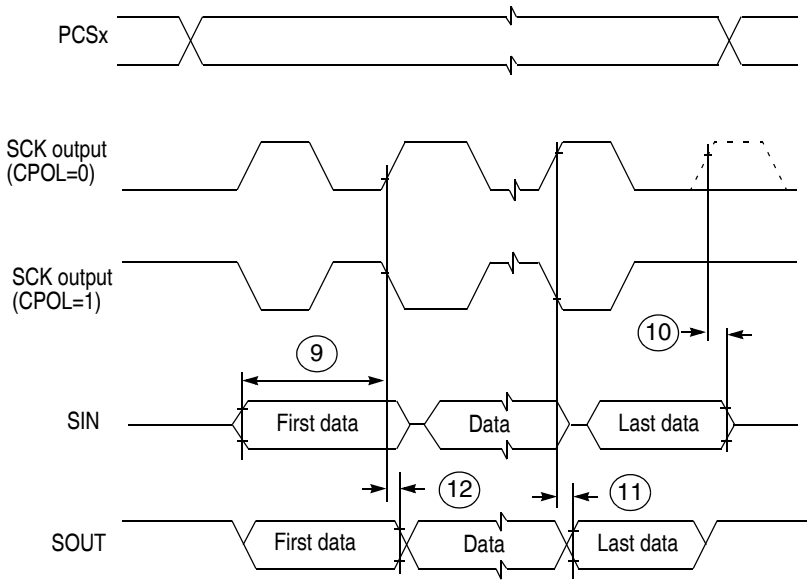
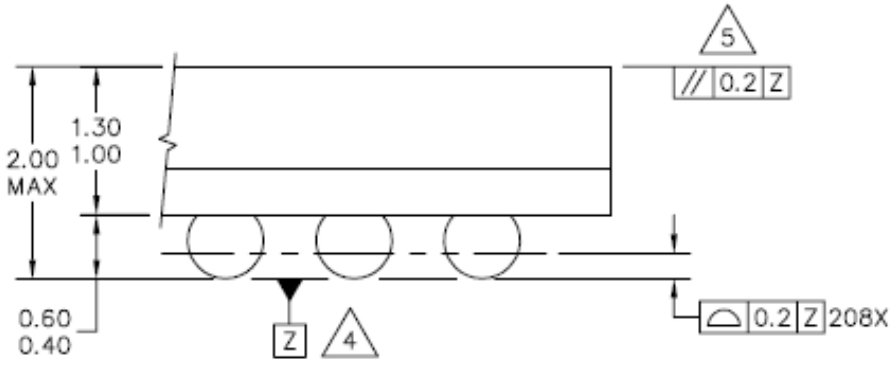


Figure 23. DSPI Modified Transfer Format Timing—Master, CPHA = 1



DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	DOCUMENT NO: 98ARS23882W	REV: D
	CASE NUMBER: 1159A–01	02 AUG 2005
	STANDARD: JEDEC MO–151 AAF–1	

Figure 32. MPC55 208 MAP BGA Package (continued)

The package drawings of the 324-pin TEPBGA package are shown in Figure 33.

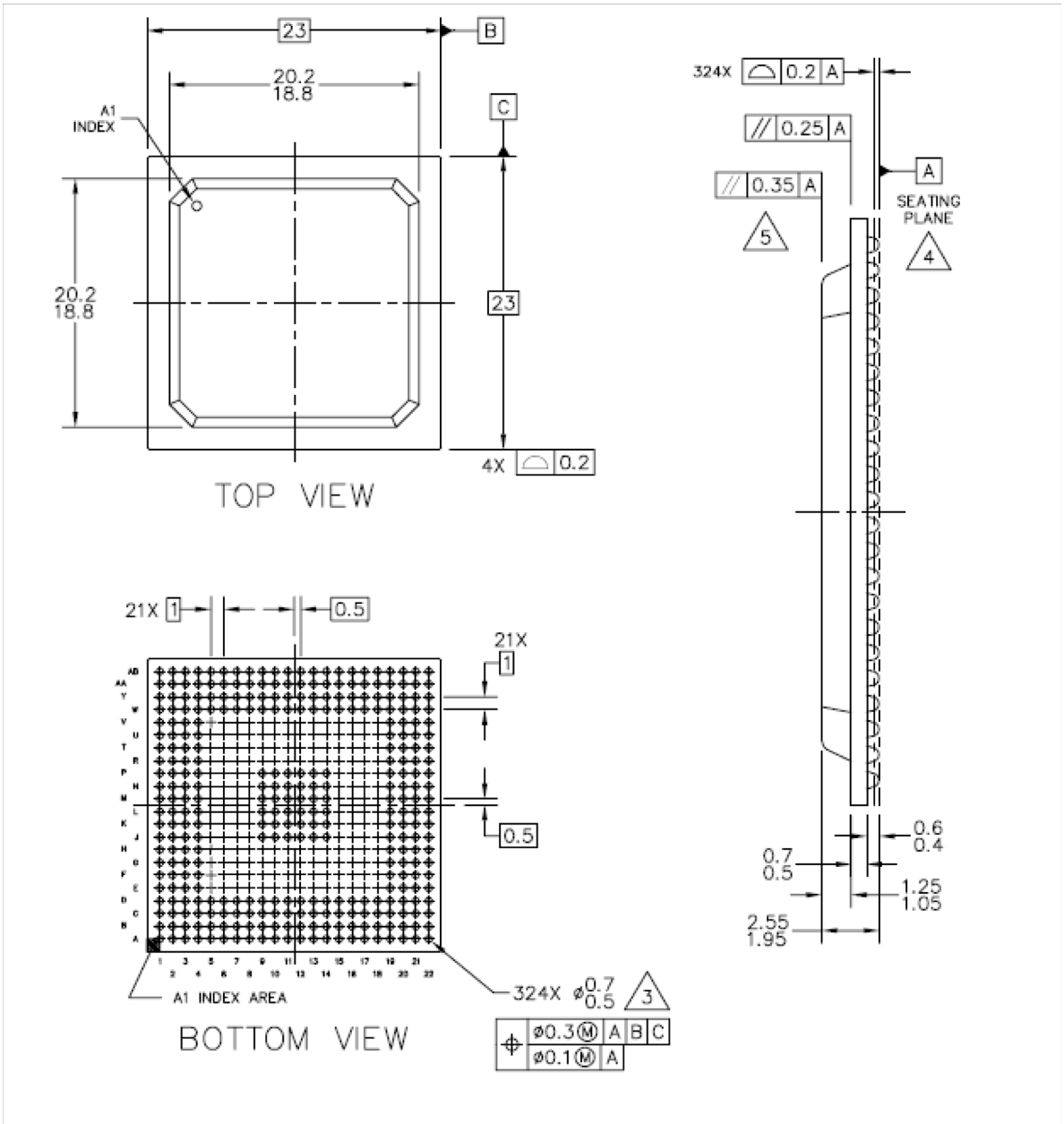

Figure 33. 324 TEPBGA Package

4.2 MPC5554 416-Pin Package Dimensions

The package drawings of the MPC5554 416 pin TEPBGA package are shown in Figure 34.

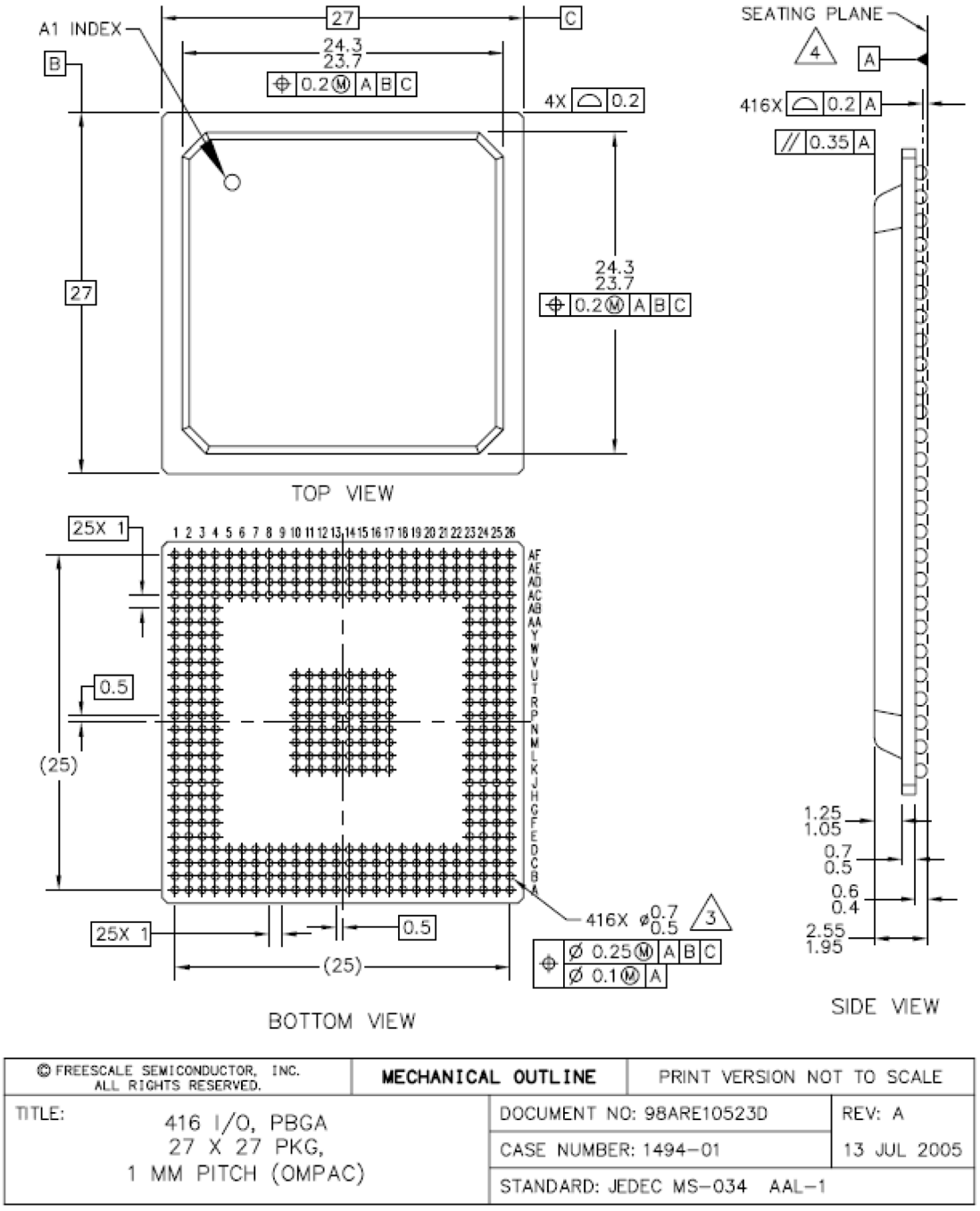

Figure 34. MPC5554 416 TEPBGA Package

Table 28. Changes Between Rev. 2.0 and 3.0 (continued)

Location	Description of Changes
Table 20 (JTAG Pin AC Electrical Characteristics) JTAG Pin AC Electrical Characteristics	• Footnote 1: Removed V_{DD} = 1.35–1.65 V, and V_{DD33} and V_{DDSYN} = 3.0–3.6 V.
Table 22 (Bus Operation Timing) Bus Operation Timing:	• External Bus Frequency in the table heading: Added footnote that reads: Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; and 132 MHz parts allow for 128 MHz system clock + 2% FM. • Specifications 5, 6, 7, and 8: Reordered the EBI signals within each specification. • Specifications 7 and 8: Removed EBI signals $\overline{BDIP}$, $\overline{OE}$, TSIZ[0:1], $\overline{WE}$/$\overline{BE}$[0:3]. • Footnote 1: Removed V_{DD} = 1.35–1.65 V, and V_{DD33} and V_{DDSYN} = 3.0–3.6 V. • Footnote 8: Changed EBTS to SIU_ECCR[EBTS].
Table 23 (External Interrupt Timing) External Interrupt Timing (IRQ Signals)	• Footnote 1: Removed V_{DD} = 1.35–1.65 V; changed V_{DDEH} = 3.0–5.5 V to V_{DDEH} = 3.0–5.25 V.
Table 24 (eTPU Timing) eTPU Timing	• Footnote 1: Changed V_{DDEH} = 3.0–5.5 V to V_{DDEH} = 3.0–5.25 V.
Table 25 (eMIOS Timing) eMIOS Timing	• Footnote 1: Changed V_{DDEH} = 3.0–5.5 V to V_{DDEH} = 3.0–5.25 V.
Table 26 (DSPI Timing') DSPI Timing:	• Footnote 1, changed 'V_{DDEH} = 3.0–5.5 V;' to 'V_{DDEH} = 3.0–5.25 V;' • Table Title: Added footnote that reads: Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; and 132 MHz parts allow for 128 MHz system clock + 2% FM. • Spec 1: SCK cycle time; Changed to 80 MHz minimum column from 25 to 24.4; 112 MHz minimum column from 17.9 to 17.5; 112 MHz maximum column from 2.0 to 2.1.
Table 27 (EQADC SSI Timing Characteristics) EQADC SSI Timing Characteristics	• Footnote 1: Changed V_{DDEH} = 3.0–5.5 V to V_{DDEH} = 3.0–5.25 V.

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