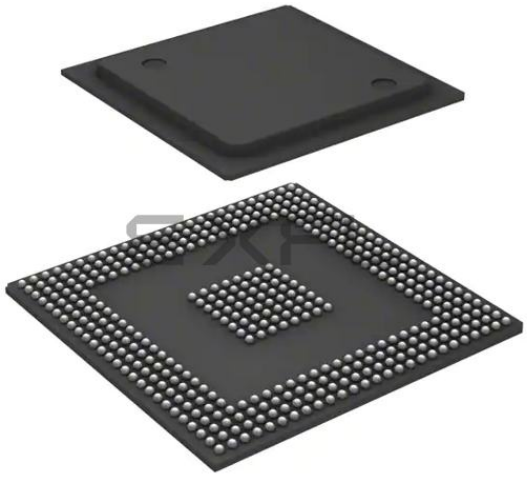

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z6
Core Size	32-Bit Single-Core
Speed	132MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	256
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 40x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/sc5554mvr132

The MPC5500 family of parts contains many new features coupled with high performance CMOS technology to provide significant performance improvement over the MPC565.

The MPC5554 has two levels of memory hierarchy. The fastest accesses are to the 32-kilobytes (KB) unified cache. The next level in the hierarchy contains the 64-KB on-chip internal SRAM and two-megabytes (MB) internal flash memory. The internal SRAM and flash memory hold instructions and data. The external bus interface is designed to support most of the standard memories used with the MPC5*xx* family.

The complex input/output timer functions of the MPC5554 are performed by two enhanced time processor unit (eTPU) engines. Each eTPU engine controls 32 hardware channels, providing a total of 64 hardware channels. The eTPU has been enhanced over the TPU by providing: 24-bit timers, double-action hardware channels, variable number of parameters per channel, angle clock hardware, and additional control and arithmetic instructions. The eTPU is programmed using a high-level programming language.

The less complex timer functions of the MPC5554 are performed by the enhanced modular input/output system (eMIOS). The eMIOS' 24 hardware channels are capable of single-action, double-action, pulse-width modulation (PWM), and modulus-counter operations. Motor control capabilities include edge-aligned and center-aligned PWM.

Off-chip communication is performed by a suite of serial protocols including controller area networks (FlexCANs), enhanced deserial/serial peripheral interfaces (DSPIs), and enhanced serial communications interfaces (eSCIs). The DSPIs support pin reduction through hardware serialization and deserialization of timer channels and general-purpose input/output (GPIOs) signals.

The MCU has an on-chip enhanced queued dual analog-to-digital converter (eQADC). 324 s40-channels.

The system integration unit (SIU) performs several chip-wide configuration functions. Pad configuration and general-purpose input and output (GPIO) are controlled from the SIU. External interrupts and reset control are also determined by the SIU. The internal multiplexer submodule provides multiplexing of eQADC trigger sources, daisy chaining the DSPIs, and external interrupt signal multiplexing.

3 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MCU.

3.1 Maximum Ratings

Table 2. Absolute Maximum Ratings [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	1.5 V core supply voltage [2]	V_{DD}	–0.3	1.7	V
2	Flash program/erase voltage	V_{PP}	–0.3	6.5	V
4	Flash read voltage	V_{FLASH}	–0.3	4.6	V
5	SRAM standby voltage	V_{STBY}	–0.3	1.7	V
6	Clock synthesizer voltage	V_{DDSYN}	–0.3	4.6	V
7	3.3 V I/O buffer voltage	V_{DD33}	–0.3	4.6	V
8	Voltage regulator control input voltage	V_{RC33}	–0.3	4.6	V
9	Analog supply voltage (reference to V_{SSA})	V_{DDA}	–0.3	5.5	V
10	I/O supply voltage (fast I/O pads) [3]	V_{DDE}	–0.3	4.6	V
11	I/O supply voltage (slow and medium I/O pads) [3]	V_{DDEH}	–0.3	6.5	V
12	DC input voltage [4] V_{DDEH} powered I/O pads V_{DDE} powered I/O pads	V_{IN}	 –1.0 [5] –1.0 [5]	 6.5 [6] 4.6 [7]	V
13	Analog reference high voltage (reference to V_{RL})	V_{RH}	–0.3	5.5	V
14	V_{SS} to V_{SSA} differential voltage	$V_{SS} – V_{SSA}$	–0.1	0.1	V
15	V_{DD} to V_{DDA} differential voltage	$V_{DD} – V_{DDA}$	$–V_{DDA}$	V_{DD}	V
16	V_{REF} differential voltage	$V_{RH} – V_{RL}$	–0.3	5.5	V
17	V_{RH} to V_{DDA} differential voltage	$V_{RH} – V_{DDA}$	–5.5	5.5	V
18	V_{RL} to V_{SSA} differential voltage	$V_{RL} – V_{SSA}$	–0.3	0.3	V
19	V_{DDEH} to V_{DDA} differential voltage	$V_{DDEH} – V_{DDA}$	$–V_{DDA}$	V_{DDEH}	V
20	V_{DDF} to V_{DD} differential voltage	$V_{DDF} – V_{DD}$	–0.3	0.3	V
21	V_{RC33} to V_{DDSYN} differential voltage spec has been moved to Table 9 DC Electrical Specifications, Spec 43a.				
22	V_{SSSYN} to V_{SS} differential voltage	$V_{SSSYN} – V_{SS}$	–0.1	0.1	V
23	V_{RCVSS} to V_{SS} differential voltage	$V_{RCVSS} – V_{SS}$	–0.1	0.1	V
24	Maximum DC digital input current [8] (per pin, applies to all digital pins) [4]	I_{MAXD}	–2	2	mA
25	Maximum DC analog input current [9] (per pin, applies to all analog pins)	I_{MAXA}	–3	3	mA
26	Maximum operating temperature range [10] Die junction temperature	T_J	T_L	150.0	°C
27	Storage temperature range	T_{STG}	–55.0	150.0	°C

Table 2. Absolute Maximum Ratings [1] (continued)

Spec	Characteristic	Symbol	Min.	Max.	Unit
28	Maximum solder temperature [11] Lead free (Pb-free) Leaded (SnPb)	T_{SDR}	 — —	 260.0 245.0	°C
29	Moisture sensitivity level [12]	MSL	—	3	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond any of the listed maxima can affect device reliability or cause permanent damage to the device.

2 1.5 V ± 10% for proper operation. This parameter is specified at a maximum junction temperature of 150 °C.

3 All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}, or V_{DDEH}.

4 AC signal overshoot and undershoot of up to ± 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).

5 Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met. Keep the negative DC voltage greater than –0.6 V on eTPUB[15] and SINB during the internal power-on reset (POR) state.

6 Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.

7 Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.

8 Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

9 Total injection current for all analog input pins must not exceed 15 mA.

10 Lifetime operation at these specification limits is not guaranteed.

11 Moisture sensitivity profile per IPC/JEDEC J-STD-020D.

12 Moisture sensitivity per JEDEC test method A112.

3.2 Thermal Characteristics

The shaded rows in the following table indicate information specific to a four-layer board.

Table 3. MPC5554 Thermal Characteristics

Spec	MPC5554 Thermal Characteristic	Symbol	416 PBGA	Unit
1	Junction to ambient [1, 2], natural convection (one-layer board)	$R_{\theta JA}$	24	°C/W
2	Junction to ambient [1, 3], natural convection (four-layer board 2s2p)	$R_{\theta JA}$	18	°C/W
3	Junction to ambient [1, 3] (@200 ft./min., one-layer board)	$R_{\theta JMA}$	19	°C/W
4	Junction to ambient [1, 3] (@200 ft./min., four-layer board 2s2p)	$R_{\theta JMA}$	15	°C/W
5	Junction to board [4] (four-layer board 2s2p)	$R_{\theta JB}$	9	°C/W
6	Junction to case [5]	$R_{\theta JC}$	5	°C/W
7	Junction to package top [6], natural convection	Ψ_{JT}	2	°C/W

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 6. V_{RC} and POR Electrical Specifications (continued)

Spec	Characteristic		Symbol	Min.	Max.	Units
8	Voltage differential during power up such that: V_{DD33} can lag V_{DDSYN} or V_{DDEH6} before V_{DDSYN} and V_{DDEH6} reach the V_{POR33} and V_{POR5} minimums respectively.		V_{DD33_LAG}	—	1.0	V
9	Absolute value of slew rate on power supply pins		—	—	50	V/ms
10	Required gain at Tj: $I_{DD} \div I_{VRCCTL}$ (@ $f_{sys} = f_{MAX}$)[6, 8, 9, 10]	– 55° C[7]	BETA[11]	70	—	—
		– 40° C		70	—	—
		25° C		85[11]	—	—
		150° C		105[11]	500	—

1 The internal POR signals are V_{POR15}, V_{POR33}, and V_{POR5}. On power up, assert $\overline{\text{RESET}}$ before the internal POR negates. $\overline{\text{RESET}}$ must remain asserted until the power supplies are within the operating conditions as specified in Table 9 DC Electrical Specifications. On power down, assert $\overline{\text{RESET}}$ before any power supplies fall outside the operating conditions and until the internal POR asserts.

2 V_{IL_S} (Table 9, Spec15) is guaranteed to scale with V_{DDEH6} down to V_{POR5}.

3 Supply full operating current for the 1.5 V supply when the 3.3 V supply reaches this range.

4 It is possible to reach the current limit during ramp up—do not treat this event as short circuit current.

5 At peak current for device.

6 Requires compliance with Freescale's recommended board requirements and transistor recommendations. Board signal traces/routing from the V_{RCCTL} package signal to the base of the external pass transistor and between the emitter of the pass transistor to the V_{DD} package signals must have a maximum of 100 nH inductance and minimal resistance (less than 1 Ω). V_{RCCTL} must have a nominal 1 μF phase compensation capacitor to ground. V_{DD} must have a 20 μF (nominal) bulk capacitor (greater than 4 μF over all conditions, including lifetime). Place high-frequency bypass capacitors consisting of eight 0.01 μF, two 0.1 μF, and one 1 μF capacitors around the package on the V_{DD} supply signals.

7 Only available on devices that support -55° C.

8 I_{VRCCTL} is measured at the following conditions: V_{DD} = 1.35 V, V_{RC33} = 3.1 V, V_{VRCCTL} = 2.2 V.

9 Refer to Table 1 for the maximum operating frequency.

10 Values are based on I_{DD} from high-use applications as explained in the I_{DD} Electrical Specification.

11 BETA represents the worst-case external transistor. It is measured on a per-part basis and calculated as ($I_{DD} \div I_{VRCCTL}$).

3.7 Power-Up/Down Sequencing

Power sequencing between the 1.5 V power supply and V_{DDSYN} or the $\overline{\text{RESET}}$ power supplies is required if using an external 1.5 V power supply with V_{RC33} tied to ground (GND). To avoid power-sequencing, V_{RC33} must be powered up within the specified operating range, even if the on-chip voltage regulator controller is not used. Refer to Section 3.7.2, "Power-Up Sequence (VRC33 Grounded)," and Section 3.7.3, "Power-Down Sequence (VRC33 Grounded)."

Power sequencing requires that V_{DD33} must reach a certain voltage where the values are read as ones before the POR signal negates. Refer to Section 3.7.1, "Input Value of Pins During POR Dependent on VDD33."

Although power sequencing is not required between V_{RC33} and V_{DDSYN} during power up, V_{RC33} must not lead V_{DDSYN} by more than 600 mV or lag by more than 100 mV for the V_{RC} stage turn-on to operate within specification. Higher spikes in the emitter current of the pass transistor occur if V_{RC33} leads or lags V_{DDSYN} by more than these amounts. The value of that higher spike in current depends on the board power supply circuitry and the amount of board level capacitance.

To avoid this condition, minimize the ramp time of the V_{DD} supply to a time period less than the time required to enable the external circuitry connected to the device outputs.

During initial power ramp-up, when Vstby is 0.6v or above. a typical current of 1-3mA and maximum of 4mA may be seen until V_{DD} is applied. This current will not reoccur until V_{stby} is lowered below V_{stby} min. specification.

Figure 2 shows an approximate interpolation of the I_{STBY} worst-case specification to estimate values at different voltages and temperatures. The vertical lines shown at 25 °C, 60 °C, and 150 °C in Figure 2 are the actual I_{DD_STBY} specifications (27d) listed in Table 9.

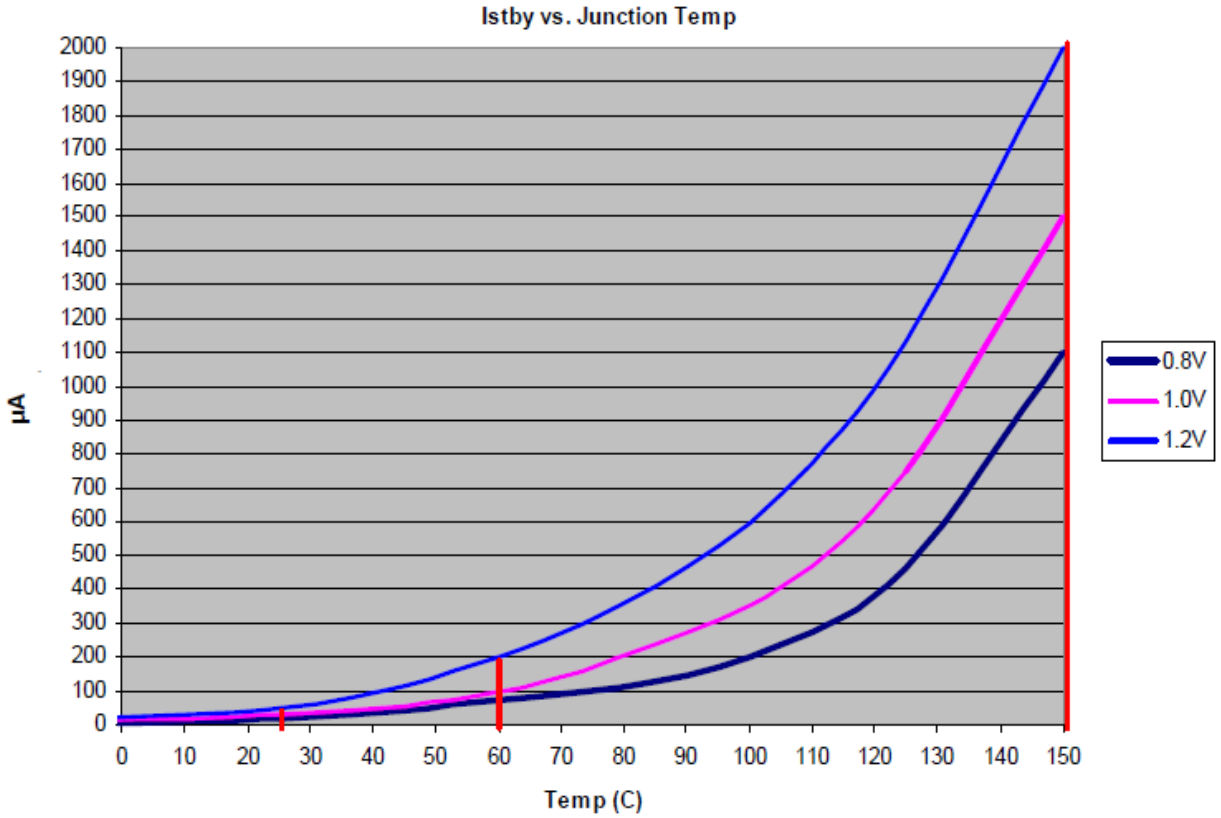


Figure 2. fISTBY Worst-case Specifications

3.7.1 Input Value of Pins During POR Dependent on V_{DD33}

When powering up the device, V_{DD33} must not lag the latest V_{DDSYN} *or* $\overline{\text{RESET}}$ power pin (V_{DDEH6}) by more than the V_{DD33} lag specification listed in Table 6, spec 8. This avoids accidentally selecting the bypass clock mode because the internal versions of PLLCFG[0:1] and $\overline{\text{RSTCFG}}$ are not powered and therefore cannot read the default state when POR negates. V_{DD33} can lag V_{DDSYN} *or* the $\overline{\text{RESET}}$ power pin (V_{DDEH6}), but cannot lag both by more than the V_{DD33} lag specification. This V_{DD33} lag specification applies during power up only. V_{DD33} has no lead or lag requirements when powering down.

3.7.2 Power-Up Sequence (V_{RC33} Grounded)

The 1.5 V V_{DD} power supply must rise to 1.35 V before the 3.3 V V_{DDSYN} power supply and the $\overline{\text{RESET}}$ power supply rises above 2.0 V. This ensures that digital logic in the PLL for the 1.5 V power supply does not begin to operate below the specified operation range lower limit of 1.35 V. Because the internal 1.5 V POR is disabled, the internal 3.3 V POR or the $\overline{\text{RESET}}$ power POR must hold the device in reset. Since they can negate as low as 2.0 V, V_{DD} must be within specification before the 3.3 V POR and the $\overline{\text{RESET}}$ POR negate.

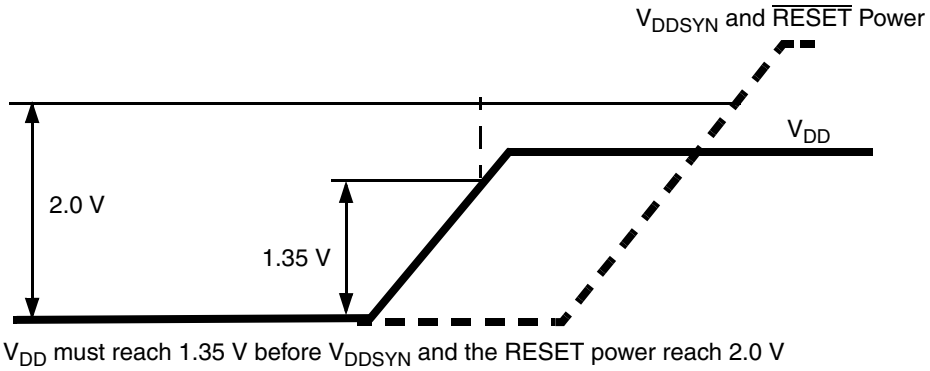


Figure 3. Power-Up Sequence (V_{RC33} Grounded)

3.7.3 Power-Down Sequence (V_{RC33} Grounded)

The only requirement for the power-down sequence with V_{RC33} grounded is if V_{DD} decreases to less than its operating range, V_{DDSYN} or the $\overline{\text{RESET}}$ power must decrease to less than 2.0 V before the V_{DD} power increases to its operating range. This ensures that the digital 1.5 V logic, which is reset only by an ORed POR and can cause the 1.5 V supply to decrease less than its specification value, resets correctly. See Table 6, footnote 1.

3.8 DC Electrical Specifications

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H)

Spec	Characteristic	Symbol	Min	Max.	Unit
1	Core supply voltage (average DC RMS voltage)	V_{DD}	1.35	1.65	V
2	Input/output supply voltage (fast input/output) [1]	V_{DDE}	1.62	3.6	V
3	Input/output supply voltage (slow and medium input/output)	V_{DDEH}	3.0	5.25	V
4	3.3 V input/output buffer voltage	V_{DD33}	3.0	3.6	V
5	Voltage regulator control input voltage	V_{RC33}	3.0	3.6	V
6	Analog supply voltage [2]	V_{DDA}	4.5	5.25	V
8	Flash programming voltage [3]	V_{PP}	4.5	5.25	V
9	Flash read voltage	V_{FLASH}	3.0	3.6	V
10	SRAM standby voltage [4]	V_{STBY}	0.8	1.2	V
11	Clock synthesizer operating voltage	V_{DDSYN}	3.0	3.6	V
12	Fast I/O input high voltage	V_{IH_F}	$0.65 \times V_{DDE}$	$V_{DDE} + 0.3$	V
13	Fast I/O input low voltage	V_{IL_F}	$V_{SS} - 0.3$	$0.35 \times V_{DDE}$	V
14	Medium and slow I/O input high voltage	V_{IH_S}	$0.65 \times V_{DDEH}$	$V_{DDEH} + 0.3$	V
15	Medium and slow I/O input low voltage	V_{IL_S}	$V_{SS} - 0.3$	$0.35 \times V_{DDEH}$	V
16	Fast input hysteresis	V_{HYS_F}	$0.1 \times V_{DDE}$		V
17	Medium and slow I/O input hysteresis	V_{HYS_S}	$0.1 \times V_{DDEH}$		V
18	Analog input voltage	V_{INDC}	$V_{SSA} - 0.3$	$V_{DDA} + 0.3$	V
19	Fast output high voltage (I_{OH_F} = –2.0 mA)	V_{OH_F}	$0.8 \times V_{DDE}$	—	V
20	Slow and medium output high voltage I_{OH_S} = –2.0 mA I_{OH_S} = –1.0 mA	V_{OH_S}	$0.80 \times V_{DDEH}$ $0.85 \times V_{DDEH}$	—	V
21	Fast output low voltage (I_{OL_F} = 2.0 mA)	V_{OL_F}	—	$0.2 \times V_{DDE}$	V
22	Slow and medium output low voltage I_{OL_S} = 2.0 mA I_{OL_S} = 1.0 mA	V_{OL_S}	—	 $0.20 \times V_{DDEH}$ $0.15 \times V_{DDEH}$	V
23	Load capacitance (fast I/O) [5] DSC (SIU_PCR[8:9]) = 0b00 = 0b01 = 0b10 = 0b11	C_L	 — — — —	 10 20 30 50	 pF pF pF pF
24	Input capacitance (digital pins)	C_{IN}	—	7	pF
25	Input capacitance (analog pins)	C_{IN_A}	—	10	pF
26	Input capacitance: (Shared digital and analog pins AN[12]_MA[0]_$\overline{SDS}$, AN[13]_MA[1]_SDO, AN[14]_MA[2]_SDI, and AN[15]_FCK)	C_{IN_M}	—	12	pF

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
30	Operating current V_{DDE} supplies: [12] V_{DDEH1} V_{DDE2} V_{DDE3} V_{DDEH4} V_{DDE5} V_{DDEH6} V_{DDE7} V_{DDEH8} V_{DDEH9}	 I_{DD1} I_{DD2} I_{DD3} I_{DD4} I_{DD5} I_{DD6} I_{DD7} I_{DD8} I_{DD9}	 — — — — — — — — —	 Refer to footnote [12]	 mA mA mA mA mA mA mA mA mA
31	Fast I/O weak pullup current [13] 1.62–1.98 V 2.25–2.75 V 3.00–3.60 V	I_{ACT_F}	 10 20 20	 110 130 170	 µA µA µA
	Fast I/O weak pulldown current [13] 1.62–1.98 V 2.25–2.75 V 3.00–3.60 V		 10 20 20	 100 130 170	 µA µA µA
32	Slow and medium I/O weak pullup/down current [13] 3.0–3.6 V 4.5–5.5 V	I_{ACT_S}	 10 20	 150 170	 µA µA
33	I/O input leakage current [14]	I_{INACT_D}	–2.5	2.5	µA
34	DC injection current (per pin)	I_{IC}	–2.0	2.0	mA
35	Analog input current, channel off [15]	I_{INACT_A}	–150	150	nA
35a	Analog input current, shared analog / digital pins (AN[12], AN[13], AN[14], AN[15])	I_{INACT_AD}	–2.5	2.5	µA
36	V_{SS} to V_{SSA} differential voltage [16]	$V_{SS} - V_{SSA}$	–100	100	mV
37	Analog reference low voltage	V_{RL}	$V_{SSA} - 0.1$	$V_{SSA} + 0.1$	V
38	V_{RL} differential voltage	$V_{RL} - V_{SSA}$	–100	100	mV
39	Analog reference high voltage	V_{RH}	$V_{DDA} - 0.1$	$V_{DDA} + 0.1$	V
40	V_{REF} differential voltage	$V_{RH} - V_{RL}$	4.5	5.25	V
41	V_{SSSYN} to V_{SS} differential voltage	$V_{SSSYN} - V_{SS}$	–50	50	mV
42	V_{RCVSS} to V_{SS} differential voltage	$V_{RCVSS} - V_{SS}$	–50	50	mV
43	V_{DDF} to V_{DD} differential voltage	$V_{DDF} - V_{DD}$	–100	100	mV
43a	V_{RC33} to V_{DDSYN} differential voltage	$V_{RC33} - V_{DDSYN}$	–0.1	0.1 [17]	V
44	Analog input differential signal range (with common mode 2.5 V)	V_{IDIFF}	–2.5	2.5	V
45	Operating temperature range, ambient (packaged)	$T_A = (T_L$ to $T_H)$	T_L	T_H	°C
46	Slew rate on power-supply pins	—	—	50	V/ms

1 V_{DDE2} and V_{DDE3} are limited to 2.25–3.6 V only if SIU_ECCR[EBTS] = 0; V_{DDE2} and V_{DDE3} have a range of 1.6–3.6 V if SIU_ECCR[EBTS] = 1.

[2] $| V_{DDA0} - V_{DDA1} |$ must be < 0.1 V.

[3] V_{PP} can drop to 3.0 V during read operations.

[4] If standby operation is not required, connect V_{STBY} to ground.

[5] Applies to CLKOUT, external bus pins, and Nexus pins.

[6] Maximum average RMS DC current.

[7] Average current measured on automotive benchmark.

[8] Peak currents can be higher on specialized code.

[9] High use current measured while running optimized SPE assembly code with all code and data 100% locked in cache (0% miss rate) with all channels of the eMIOS and eTPU running autonomously, plus the eDMA transferring data continuously from SRAM to SRAM. Higher currents are possible if an “idle” loop that crosses cache lines is run from cache. Write code that avoids this condition.

[10] The current specification relates to average standby operation after SRAM has been loaded with data. For power up current see Section 3.7, “Power-Up/Down Sequencing”, Figure 2.

[11] Power requirements for the V_{DD33} supply depend on the frequency of operation, load of all I/O pins, and the voltages on the I/O segments. Refer to Table 11 for values to calculate the power dissipation for a specific operation.

[12] Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. Refer to Table 10 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

[13] Absolute value of current, measured at V_{IL} and V_{IH}.

[14] Weak pullup/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to pad types: pad_fc, pad_sh, and pad_mh.

[15] Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 ^{o}C to 12 ^{o}C, in the ambient temperature range of 50 ^{o}C to 125 ^{o}C. Applies to pad types: pad_a and pad_ae.

[16] V_{SSA} refers to both V_{SSA0} and V_{SSA1}. $| V_{SSA0} - V_{SSA1} |$ must be < 0.1 V.

[17] Up to 0.6 V during power up and power down.

3.8.1 I/O Pad Current Specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a segment. The output pin current can be calculated from Table 10 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 10.

Table 10. I/O Pad Average DC Current ($T_A = T_L$ to T_H)[1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Drive Select / Slew Rate Control Setting	Current (mA)
1	Slow	I_{DRV_SH}	25	50	5.25	11	8.0
2			10	50	5.25	01	3.2
3			2	50	5.25	00	0.7
4			2	200	5.25	00	2.4
5	Medium	I_{DRV_MH}	50	50	5.25	11	17.3
6			20	50	5.25	01	6.5
7			3.33	50	5.25	00	1.1
8			3.33	200	5.25	00	3.9
9	Fast	I_{DRV_FC}	66	10	3.6	00	2.8
10			66	20	3.6	01	5.2
11			66	30	3.6	10	8.5
12			66	50	3.6	11	11.0
13			66	10	1.98	00	1.6
14			66	20	1.98	01	2.9
15			66	30	1.98	10	4.2
16			66	50	1.98	11	6.7
17			56	10	3.6	00	2.4
18			56	20	3.6	01	4.4
19			56	30	3.6	10	7.2
20			56	50	3.6	11	9.3
21			56	10	1.98	00	1.3
22			56	20	1.98	01	2.5
23			56	30	1.98	10	3.5
24			56	50	1.98	11	5.7
25			40	10	3.6	00	1.7
26			40	20	3.6	01	3.1
27			40	30	3.6	10	5.1
28			40	50	3.6	11	6.6
29			40	10	1.98	00	1.0
30			40	20	1.98	01	1.8
31			40	30	1.98	10	2.5
32			40	50	1.98	11	4.0

1 These values are estimates from simulation and are not tested. Currents apply to output pins only.

2 All loads are lumped.

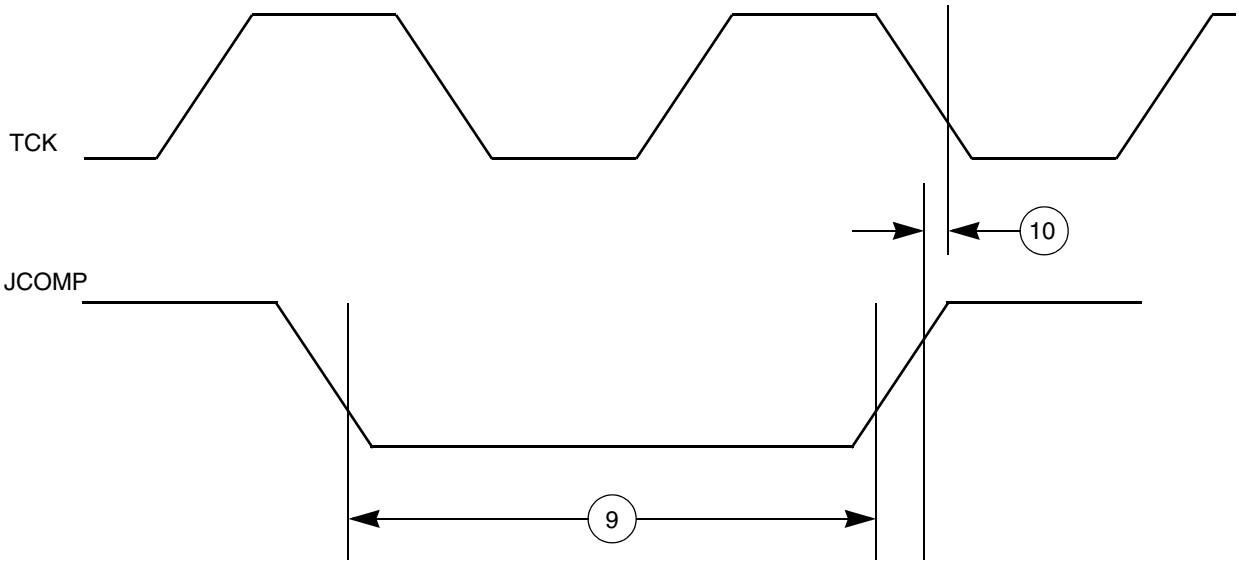


Figure 8. JTAG JCOMP Timing

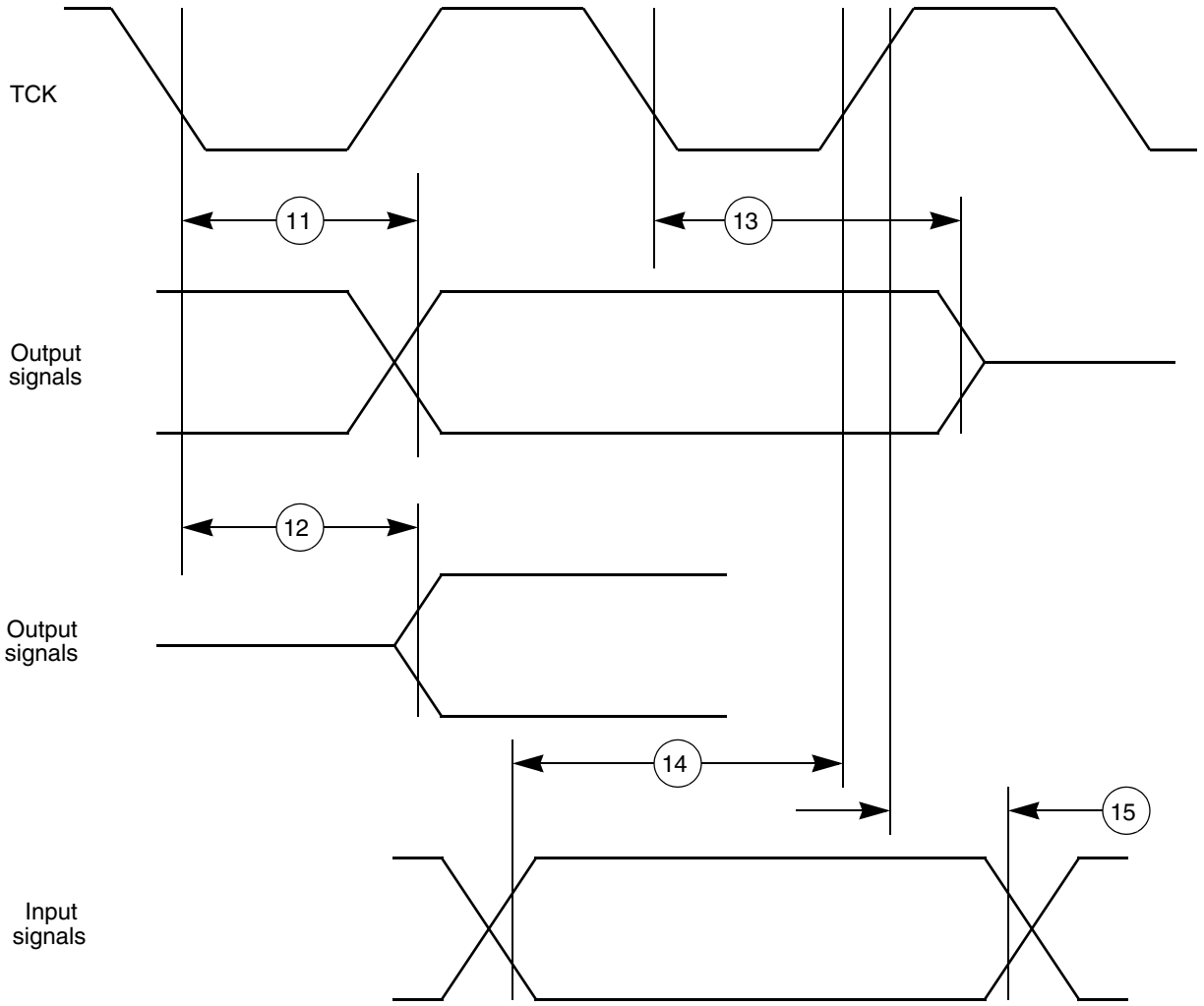


Figure 9. JTAG Boundary Scan Timing

3.13.4 External Bus Interface (EBI) Timing

Table 22 lists the timing information for the external bus interface (EBI).

Table 22. Bus Operation Timing[1]

Spec	Characteristic and Description	Symbol	External Bus Frequency [2, 3]						Unit	Notes
			40 MHz		56 MHz		66 MHz			
			Min.	Max.	Min.	Max.	Min.	Max.		
1	CLKOUT period	T_C	24.4	—	17.5	—	15.2	—	ns	Signals are measured at 50% V_{DDE}.
2	CLKOUT duty cycle	t_{CDC}	45%	55%	45%	55%	45%	55%	T_C	
3	CLKOUT rise time	t_{CRT}	—	—[4]	—	—[4]	—	—[4]	ns	
4	CLKOUT fall time	t_{CFT}	—	—[4]	—	—[4]	—	—[4]	ns	
5	CLKOUT positive edge to output signal *invalid* or Hi-Z (hold time) External bus interface $\overline{BG}$[5] $\overline{BR}$[6] $\overline{BB}$ $\overline{CS}$[0:3] ADDR[8:31] DATA[0:31][7] $\overline{BDIP}$ $\overline{OE}$ RD_$\overline{WR}$ $\overline{TA}$ $\overline{TEA}$[8] $\overline{TS}$ TSIZ[0:1] $\overline{WE}$/$\overline{BE}$[0:3][9]	t_{COH}	1.0[10] 1.5	—	1.0[10] 1.5	—	1.0[10] 1.5	—	ns	EBTS = 0 EBTS = 1 Hold time selectable via SIU_ECCR [EBTS] bit.
6	CLKOUT positive edge to output signal *valid* (output delay) External bus interface $\overline{BG}$[5] $\overline{BR}$[6] $\overline{BB}$ $\overline{CS}$[0:3] ADDR[8:31] DATA[0:31][7] $\overline{BDIP}$ $\overline{OE}$ RD_$\overline{WR}$ $\overline{TA}$ $\overline{TEA}$[8] $\overline{TS}$ TSIZ[0:1] $\overline{WE}$/$\overline{BE}$[0:3][9]	t_{COV}	—	10.0[10] 11.0	—	7.5[10] 8.5	—	6.0[10] 7.0	ns	EBTS = 0 EBTS = 1 Output valid time selectable via SIU_ECCR [EBTS] bit.

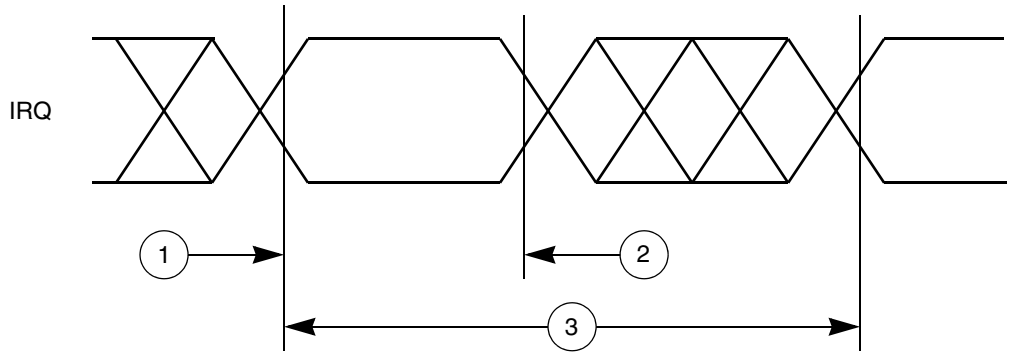


Figure 15. External Interrupt Timing

3.13.6 eTPU Timing

Table 24. eTPU Timing [1]

Spec	Characteristic	Symbol	Min.	Max	Unit
1	eTPU input channel pulse width	t_{ICPW}	4	—	t_{CYC}
2	eTPU output channel pulse width	t_{OCPW}	2 [2]	—	t_{CYC}

1 eTPU timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

2 This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

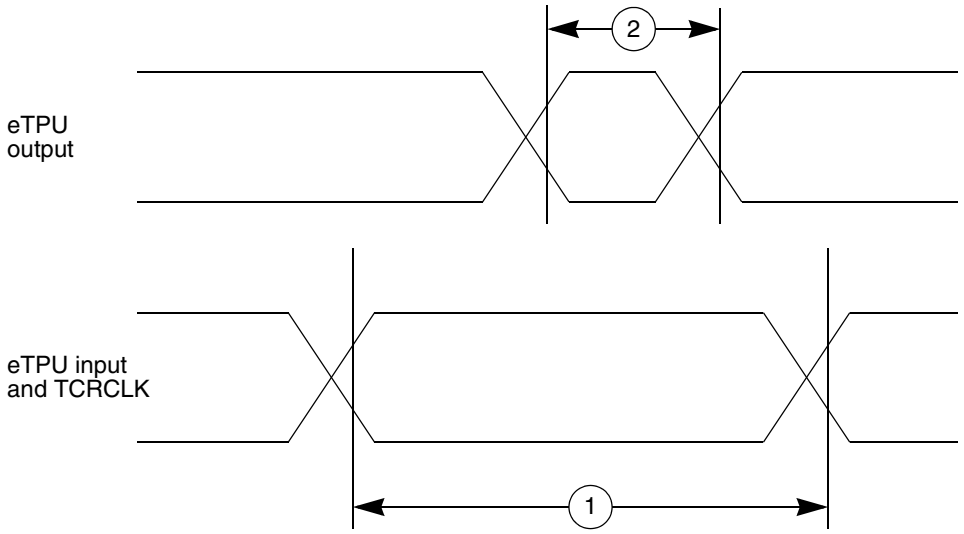


Figure 16. eTPU Timing

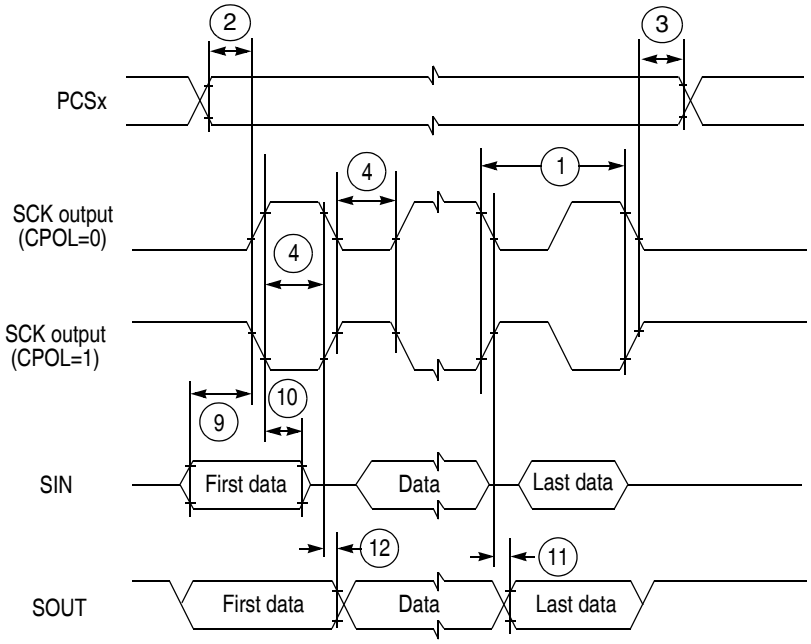


Figure 18. DSPI Classic SPI Timing—Master, CPHA = 0

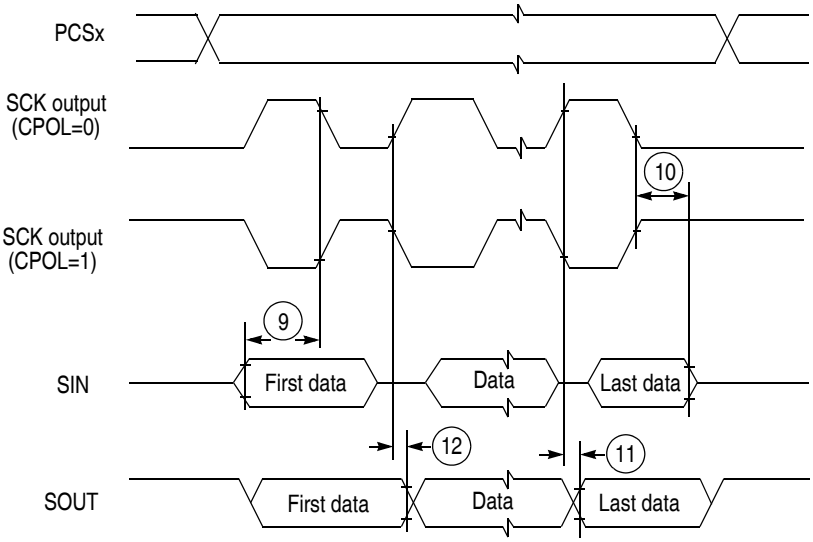


Figure 19. DSPI Classic SPI Timing—Master, CPHA = 1

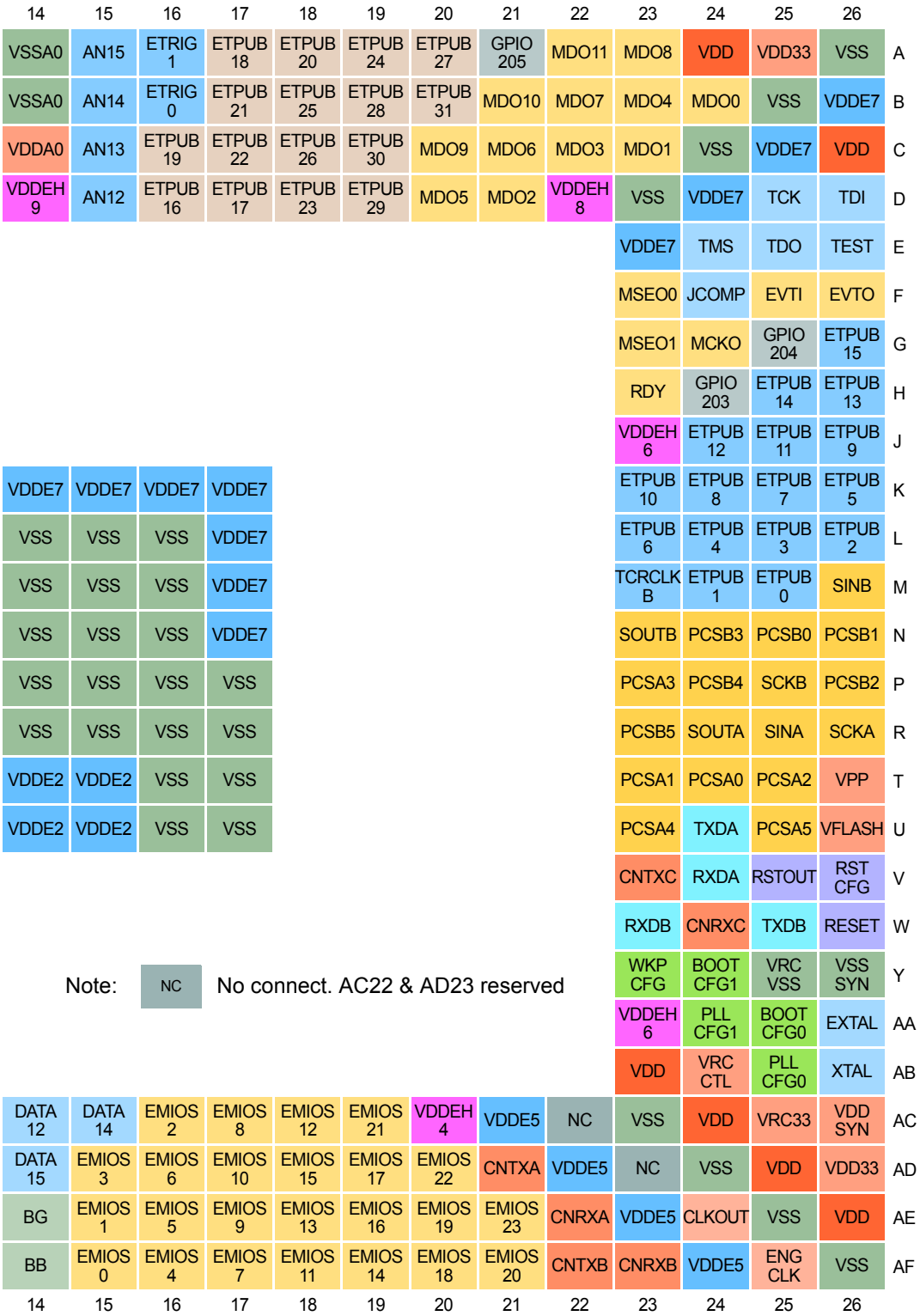
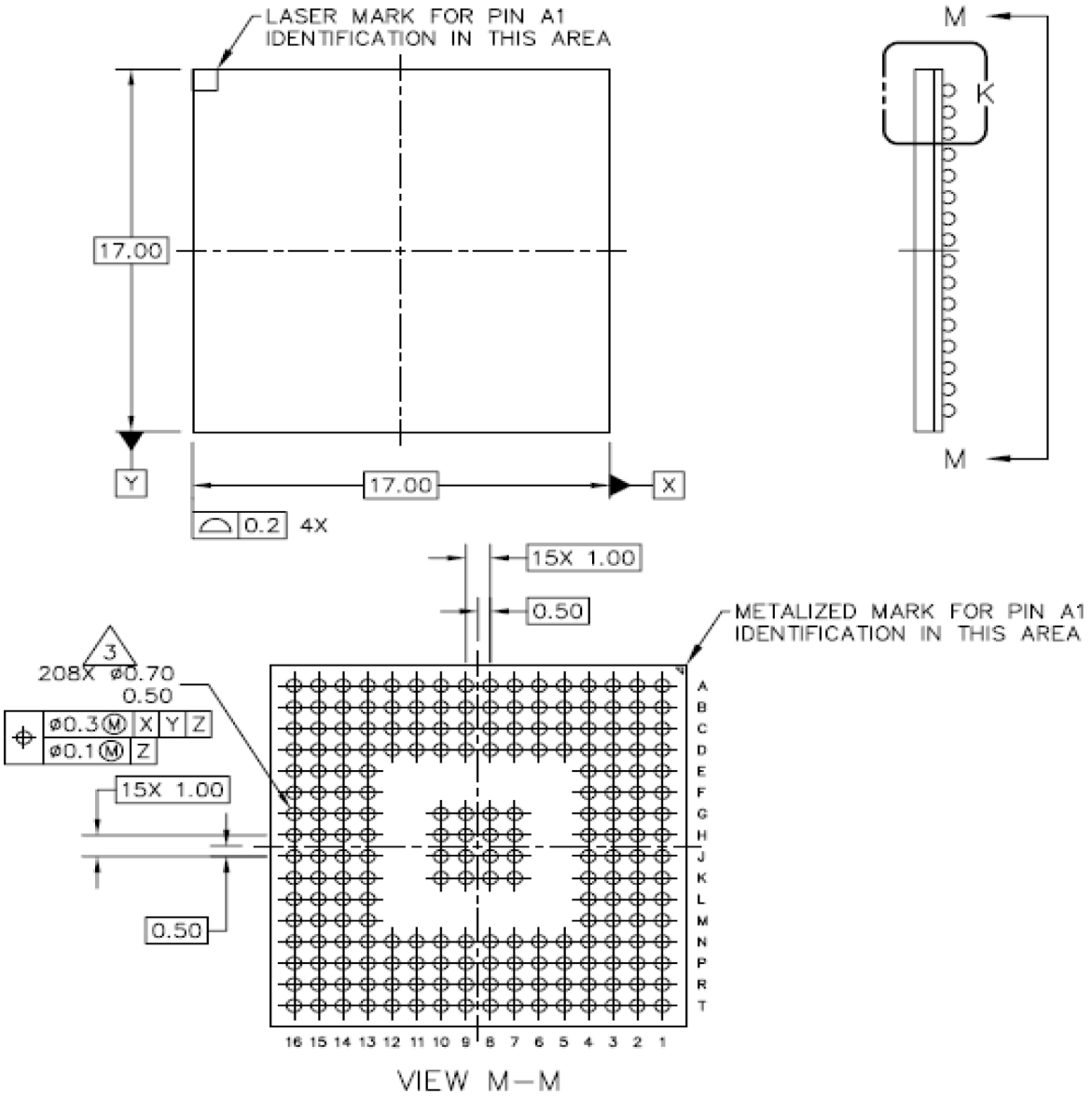


Figure 30. MPC5553546667 416 Package Right Side (view 2 of 2)

Figure 31. MPC5567 416 Package

The package drawings of the MPC55 208-pin MAP BGA are shown below.



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TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	DOCUMENT NO: 98ARS23882W	REV: D
	CASE NUMBER: 1159A–01	02 AUG 2005
	STANDARD: JEDEC MO–151 AAF–1	

Figure 32. 208-Pin Package

4.2 MPC5554 416-Pin Package Dimensions

The package drawings of the MPC5554 416 pin TEPBGA package are shown in Figure 34.

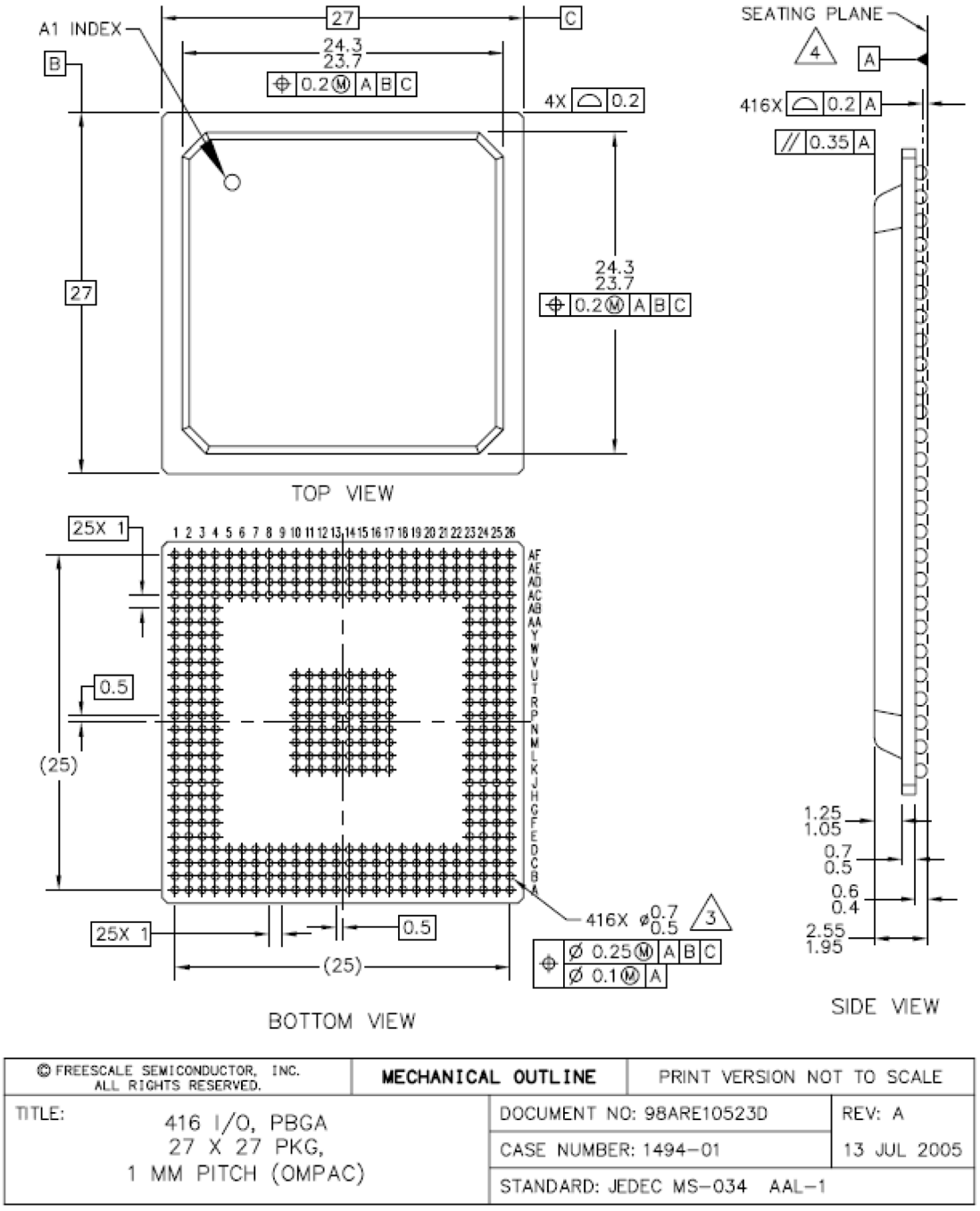

Figure 34. MPC5554 416 TEPBGA Package

Table 28. Changes Between Rev. 2.0 and 3.0 (continued)

Location	Description of Changes
Table 20 (JTAG Pin AC Electrical Characteristics) JTAG Pin AC Electrical Characteristics	• Footnote 1: Removed V_{DD} = 1.35–1.65 V, and V_{DD33} and V_{DDSYN} = 3.0–3.6 V.
Table 22 (Bus Operation Timing) Bus Operation Timing:	• External Bus Frequency in the table heading: Added footnote that reads: Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; and 132 MHz parts allow for 128 MHz system clock + 2% FM. • Specifications 5, 6, 7, and 8: Reordered the EBI signals within each specification. • Specifications 7 and 8: Removed EBI signals $\overline{BDIP}$, $\overline{OE}$, TSIZ[0:1], $\overline{WE}$/$\overline{BE}$[0:3]. • Footnote 1: Removed V_{DD} = 1.35–1.65 V, and V_{DD33} and V_{DDSYN} = 3.0–3.6 V. • Footnote 8: Changed EBTS to SIU_ECCR[EBTS].
Table 23 (External Interrupt Timing) External Interrupt Timing (IRQ Signals)	• Footnote 1: Removed V_{DD} = 1.35–1.65 V; changed V_{DDEH} = 3.0–5.5 V to V_{DDEH} = 3.0–5.25 V.
Table 24 (eTPU Timing) eTPU Timing	• Footnote 1: Changed V_{DDEH} = 3.0–5.5 V to V_{DDEH} = 3.0–5.25 V.
Table 25 (eMIOS Timing) eMIOS Timing	• Footnote 1: Changed V_{DDEH} = 3.0–5.5 V to V_{DDEH} = 3.0–5.25 V.
Table 26 (DSPI Timing') DSPI Timing:	• Footnote 1, changed 'V_{DDEH} = 3.0–5.5 V;' to 'V_{DDEH} = 3.0–5.25 V;' • Table Title: Added footnote that reads: Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; and 132 MHz parts allow for 128 MHz system clock + 2% FM. • Spec 1: SCK cycle time; Changed to 80 MHz minimum column from 25 to 24.4; 112 MHz minimum column from 17.9 to 17.5; 112 MHz maximum column from 2.0 to 2.1.
Table 27 (EQADC SSI Timing Characteristics) EQADC SSI Timing Characteristics	• Footnote 1: Changed V_{DDEH} = 3.0–5.5 V to V_{DDEH} = 3.0–5.25 V.

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