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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A53
Number of Cores/Bus Width	2 Core, 64-Bit
Speed	1.5GHz
Co-Processors/DSP	ARM® Cortex®-M4
RAM Controllers	DDR3L, DDR4, LPDDR4
Graphics Acceleration	Yes
Display & Interface Controllers	eDP, HDMI, MIPI-CSI, MIPI-DSI
Ethernet	GbE
SATA	-
USB	USB 3.0 (2)
Voltage - I/O	-
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, CAAM, HAB, RDC, RTC, SJC, SNVS
Package / Case	621-FBGA, FCBGA
Supplier Device Package	621-FCPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mimx8md6dvajzaa

3 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX 8M Dual / 8M QuadLite / 8M Quad processors.

3.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See Table 4 for a quick reference to the individual tables and sections.

Table 4. i.MX 8M Dual / 8M QuadLite / 8M Quad chip-level conditions

For these characteristics, …	Topic appears …
Absolute maximum ratings	on page 13
FPBGA package thermal resistance	on page 14
Operating ranges	on page 15
External clock sources	on page 17
Maximum supply currents	on page 18
Power modes	on page 19
USB PHY Suspend current consumption	on page 22

3.1.1 Absolute maximum ratings

CAUTION

Stresses beyond those listed under Table 5 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operating ranges or parameters tables is not implied.

Table 5. Absolute maximum ratings

Parameter description	Symbol	Min	Max	Unit	Notes
Core supply voltages	VDD_ARM VDD_SOC	0	1.1	V	1.1 V is for VDD_ARM overdrive
Power supply for GPU	VDD_GPU	0	1.1	V	1.1 V is for overdrive
Power supply for VPU	VDD_VPU	0	1.1	V	Nominal mode
		0	1.1	V	Overdrive mode

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

3.1.3 Operating ranges

Table 7 provides the operating ranges of the i.MX 8M Dual / 8M QuadLite / 8M Quad processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processor Reference Manual* (IMX8MDQLQRM).

Table 7. Operating ranges

Parameter description	Symbol	Min	Typ	Max[1]	Unit	Comment
Power supply for Quad-A53	VDD_ARM	0.81	0.9	1.05	V	Nominal mode—the maximum Arm core frequency supported in this mode is 1000 MHz.
		0.9	1.0	1.05	V	Overdrive mode—the maximum Arm core frequency supported in this mode is defined in Table 2.
Power supply for SoC logic	VDD_SOC	0.81	0.9	0.99	V	—
Power supply for GPU	VDD_GPU	0.81	0.9	1.05	V	Nominal mode—the maximum GPU frequency supported in this mode is 800 MHz.
		0.9	1.0	1.05	V	Overdrive mode—the maximum GPU frequency supported in this mode is 1 GHz.
Power supply for VPU	VDD_VPU	0.81	0.9	1.05	V	Nominal mode—the maximum VPU frequency supported in this mode is 550/500/588 MHz.
		0.9	1.0	1.05	V	Overdrive mode—the maximum VPU G2/G1/AXI Bus frequency supported in this mode is 660/600/800 MHz.
Core voltage	VDD_DRAM	0.81	0.9	1.05	V	Nominal mode—the maximum DRAM working frequency supported in this mode is 933 MHz.
		0.99	1.0	1.05	V	Overdrive mode—the maximum DRAM working frequency supported in this mode is 1600 MHz
Power Supply Analog Domain	VDDA_1P8	1.62	1.8	1.98	V	Power for internal analog blocks—must match the range of voltages that the rechargeable backup battery supports.
PLL 1.8 V supply voltage	VDDA_DRAM	1.71	1.8	1.89	V	—
Backup battery supply range	VDD_SNVS	0.81	0.9	0.99	V	—

Table 11. The power supply states (continued)

Power rail	OFF	SNVS	SUSPEND	IDLE	RUN
VDD_GPU	OFF	OFF	OFF	OFF	ON/OFF
VDD_VPU	OFF	OFF	OFF	OFF	ON/OFF
VDD_DRAM	OFF	OFF	OFF	ON	ON
VDDA_0P9	OFF	OFF	ON	ON	ON
VDDA_1P8	OFF	OFF	ON	ON	ON
VDDA_DRAM	OFF	OFF	ON	ON	ON
VDD_SNVS	OFF	ON	ON	ON	ON
NVCC_SNVS	OFF	ON	ON	ON	ON
NVCC_<XXX>	OFF	OFF	ON	ON	ON
NVCC_DRAM	OFF	OFF	ON	ON	ON
DRAM_VREF	OFF	OFF	OFF	ON	ON

Table 15. PCIe recommended operating conditions (continued)

Parameter	Description	Min	Max	Unit
T_A	Commercial Temperature Range	0	70	°C
T_J	Simulation Junction Temperature Range	-40	125	°C

Note: V_{DD} should have no more than 40 mVpp AC power supply noise superimposed on the high power supply voltage for the PHY core (1.8 V nominal DC value). At the same time, VDD should have no more than 20 mVpp AC power supply noise superimposed on the low power supply voltage for the PHY core (1.0 V nominal value or 1.1 V overdrive DC value).
The power supply voltage variation for the PHY core should have less than ±5% including the board-level power supply variation and on-chip power supply variation due to the finite impedances in the package.

Table 16. PCIe DC electrical characteristics

Parameter	Description		Min	Typ	Max	Unit
PCIE1_VP, PCIE2_VP	Power Supply Voltage		0.9 - 7%	0.9	0.9 + 10%	V
PD	Power Consumption	Normal	—	40	—	mW
		Partial Mode	—	27	—	mW
		Slumber Mode	—	7	—	mW
		Full Powerdown	—	0.2	—	mW

Table 17. PCIe PHY high-speed characteristics

High Speed I/O Characteristics						
Description	**Symbol**	**Speed**	**Min.**	**Typ.**	**Max.**	**Unit**
Unit Interval	UI	2.5 Gbps	—	400	—	ps
		5.0 Gbps	—	200	—	
TX Serial output rise time (20% to 80%)	T_{TXRISE}	2.5 Gbps	100	—	—	ps
		5.0 Gbps	100	—	—	
TX Serial output fall time (80% to 20%)	T_{TXFALL}	2.5 Gbps	100	—	—	ps
		5.0 Gbps	100	—	—	
TX Serial data output voltage (Differential, pk–pk)	ΔV_{TX}	2.5 Gbps	800	—	1100	mVp–p
		5.0 Gbps	600	—	900	
PCIe Tx deterministic jitter < 1.5 MHz	TRJ	2.5 Gbps	3	—	—	ps, rms
		5.0 Gbps	3	—	—	
PCIe Tx deterministic jitter > 1.5 MHz	TDJ	2.5 Gbps	—	—	20	ps, pk–pk
		5.0 Gbps	—	—	10	

Table 23 shows the input clock specifications.

Table 23. Input clock specification

Parameter	Min	Typ	Max	Unit
Clock Frequency in OSC mode	20	—	40	MHz
Input Clock Frequency in Bypass mode	—	—	50	MHz
Input Clock Rise/Fall Time in Bypass mode	—	—	1	ns
Input Clock Duty Cycle in Bypass mode	47.50	50	52.50	%

Table 24 shows core output clock specification.

Table 24. Core output clock specification

Parameter	Min	Typ	Max	Unit
Output Clock Frequency in OSC mode	20	—	40	MHz
Output Clock Duty Cycle in OSC mode	45	50	55	%
Output Clock Frequency in Bypass mode	—	—	50	MHz
Capacitive Loading on Outputs Clock	—	150	500	fF
Output Clock Rise/Fall Time in Bypass mode	—	0.1	0.5	ns
Output Clock Duty Cycle in Bypass mode	40	50	60	%

Table 25 shows VIL/VIH specification at EXTAL.

Table 25. Transconductance specification of oscillator

Parameter	Condition	Min	Max	Unit
$V_{ILEXTAL}$	V_{REF} = 0.5 x avdd (xosc HV supply)	0	V_{REF} - 0.5	V
$V_{IHEXTAL}$		V_{REF} + 0.5	avdd	

3.5 I/O DC parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR4, DDR4, and DDR3L modes
- Differential I/O (CLKx)

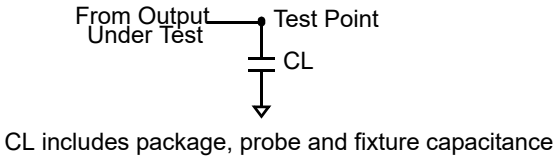

Figure 3. Load circuit for output

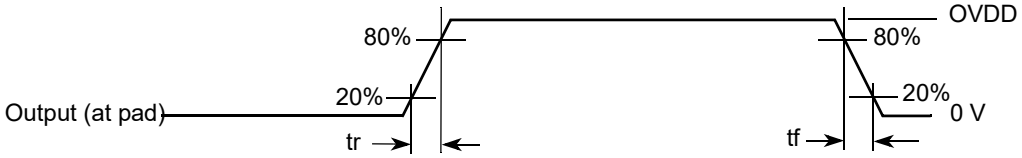

Figure 4. Output transition time waveform

3.6.1 General purpose I/O AC parameters

This section presents the I/O AC parameters for GPIO in different modes. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 31. Maximum input cell delay time

Cell name	Max Delay PAD → Y (ns)		
	V_{DD} = 1.62 V T = 125°C WCS model	—	V_{DD} = 3.0V T = 125°C WCS model
PBIJGTOV36PUD_MCLAMP_LVGPIO_EW	1.54	—	1.3

Table 32. Output cell delay time for fixed load

Parameter			Simulated Cell Delay A → PAD (ns)	
			VDD = 1.62 V, T = 125°C	VDD = 2.97 V, T = 125°C
dse[2:0]	fsel[1:0]	Driver Type	CL = 15 pF	CL = 15 pF
011	00	3 x Slow Slew	3.1	3.3
011	11	3 x Fast Slew	2.1	2.6
100	00	4 x Slow Slew	3.7	3.9
100	11	4 x Fast Slew	2.3	2.8
101	00	5 x Slow Slew	3.1	3.5
101	11	5 x Fast Slew	2.1	2.5

Table 34 shows the AC parameters for clock I/O.

Table 34. I/O AC parameters of LVDS pad

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Notes
Tphld	Output Differential propagation delay high to low	Rload = 100 Ω between padp and padn, Cload = 2pF, at 125 °C, TYP, 1.62 V OVDD, and 0.9 V VDDI	—	—	0.92	ns	1
Tplhd	Output Differential propagation delay low to high		—	—	0.92		
Ttlh	Output Transition time low to high		—	—	0.58		2
Tthl	Output Transition time high to low		—	—	0.73		
Tphlr	Input Differential propagation delay high to low	Rload = 100 Ω between padp and padn, at 125 °C, TYP, 1.62 V OVDD, and 0.9 V VDDI	—	—	0.83	ns	3
Tplhr	Input Differential propagation delay low to high		—	—	0.83		
Ttx	Transmitter startup time (ipp-obe low to high)	—	—	—	40	ns	4
F	Operating frequency	—	—	600	1000	MHz	—

1 At TYP, 125 °C, 1.62 V OVDD, and 0.9 V VDDI. Measurement levels are 50 - 50%. Output differential signal measured.

2 At TYP, 125 °C, 1.62 V OVDD, and 0.9 V VDDI. Measurement levels are 20 - 80%. Output differential signal measured.

3 At TYP, 125 °C, 1.62 V OVDD, and 0.9 V VDDI. Measurement levels are 50 - 50%.

4 TX startup time is defined as the time taken by transmitter for settling after its ipp_obe has been asserted. It is to stabilize the current reference. Functionality is guaranteed only after the startup time.

3.7 Output buffer impedance parameters

This section defines the I/O impedance parameters of the i.MX 8M Dual / 8M QuadLite / 8M Quad processors for the following I/O types:

- Double Data Rate I/O (DDR) for LPDDR4, DDR4, and DDR3L modes
- Differential I/O (CLKx)
- USB battery charger detection open-drain output (USB_OTG1_CHD_B)

NOTE

DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 6).

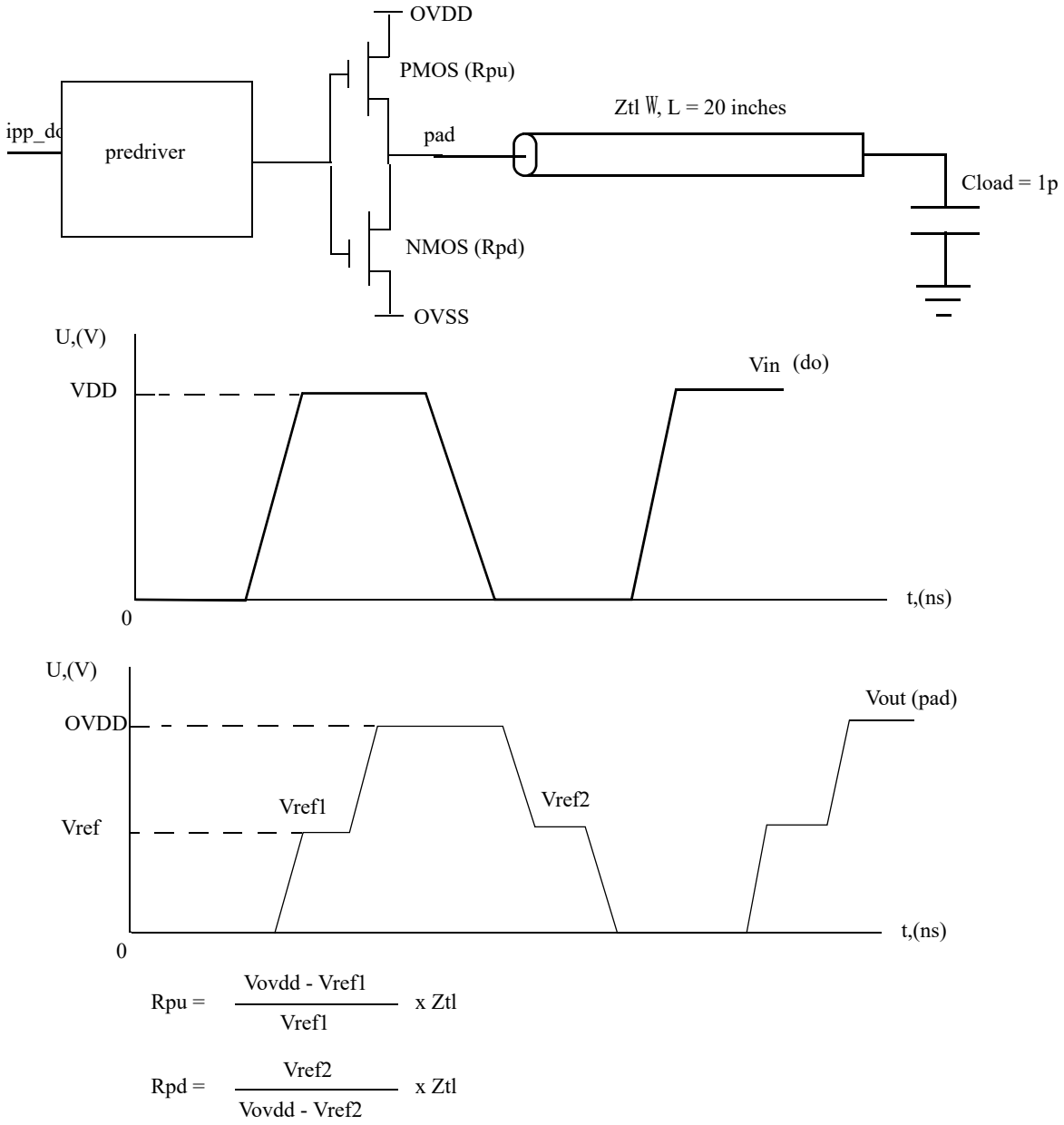

Figure 6. Impedance matching load for measurement

3.8.1 Reset timings parameters

Figure 7 shows the reset timing and Table 36 lists the timing parameters.

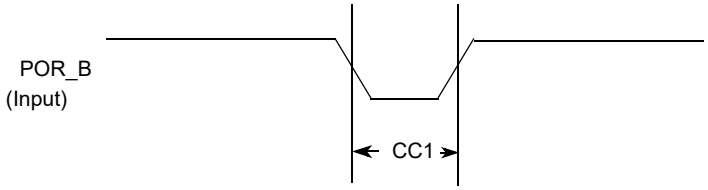

Figure 7. Reset timing diagram

Table 36. Reset timing parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid.	1	—	RTC_XTALI cycle

3.8.2 WDOG Reset timing parameters

Figure 8 shows the WDOG reset timing and Table 37 lists the timing parameters.

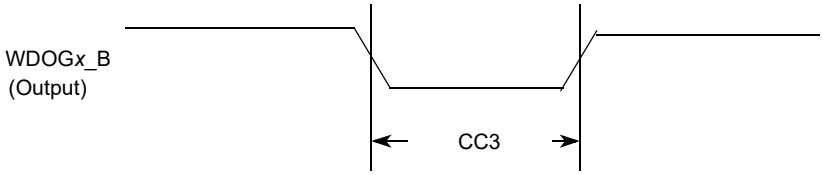

Figure 8. WDOG*x*_B timing diagram

Table 37. WDOG*x*_B timing parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG1_B Assertion	1	—	RTC_XTALI cycle

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 ms.

NOTE

WDOG*x*_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUXC chapter of the *i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processor Reference Manual* (IMX8MDQLQRM) for detailed information.

3.9 External peripheral interface parameters

The following subsections provide information on external peripheral interfaces.

3.9.1 ECSPI timing parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

3.9.1.1 ECSPI Master mode timing

Figure 9 depicts the timing of ECSPI in master mode. Table 38 lists the ECSPI master mode timing characteristics.

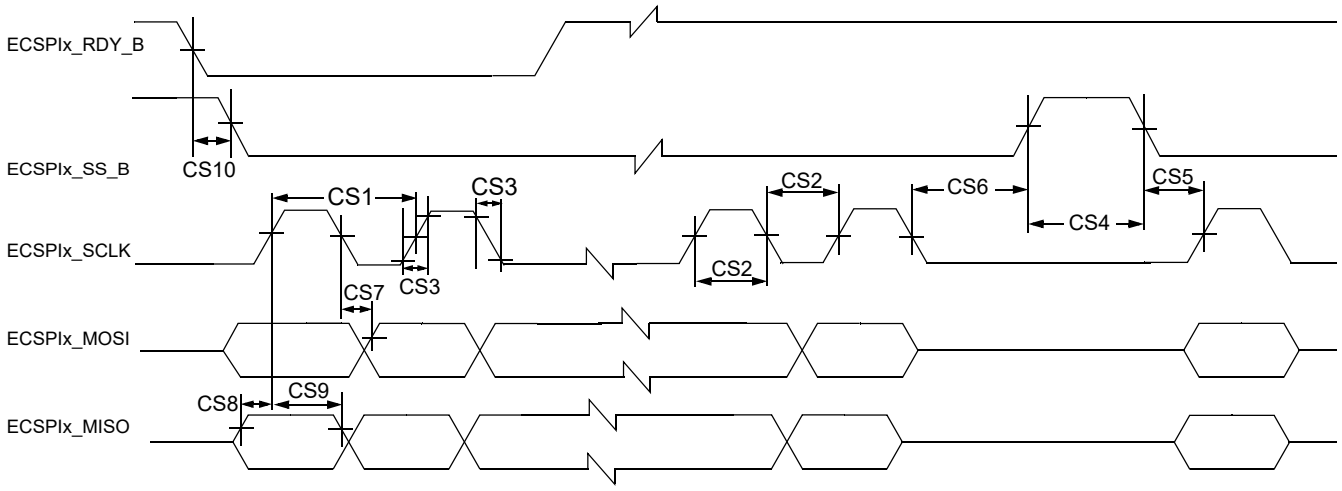

Figure 9. ECSPI Master mode timing diagram

Table 38. ECSPI Master mode timing parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time	t_{Smiso}	18	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to ECSPIx_SS_B Time[2]	t_{SDRY}	5	—	ns

1 See specific I/O AC parameters Section 3.6, “I/O AC parameters.”

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

Table 41. eMMC4.4/4.41 interface timing specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD3	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.3	—	ns

3.9.2.3 HS400 DDR AC timing–eMMC5.0 only

Figure 13 depicts the timing of HS400 mode, and Table 42 lists the HS400 timing characteristics. Be aware that only data is sampled on both edges of the clock (not applicable to CMD). The CMD input/output timing for HS400 mode is the same as CMD input/output timing for SDR104 mode. Check SD5, SD6, and SD7 parameters in Table 44 SDR50/SDR104 Interface Timing Specification for CMD input/output timing for HS400 mode.

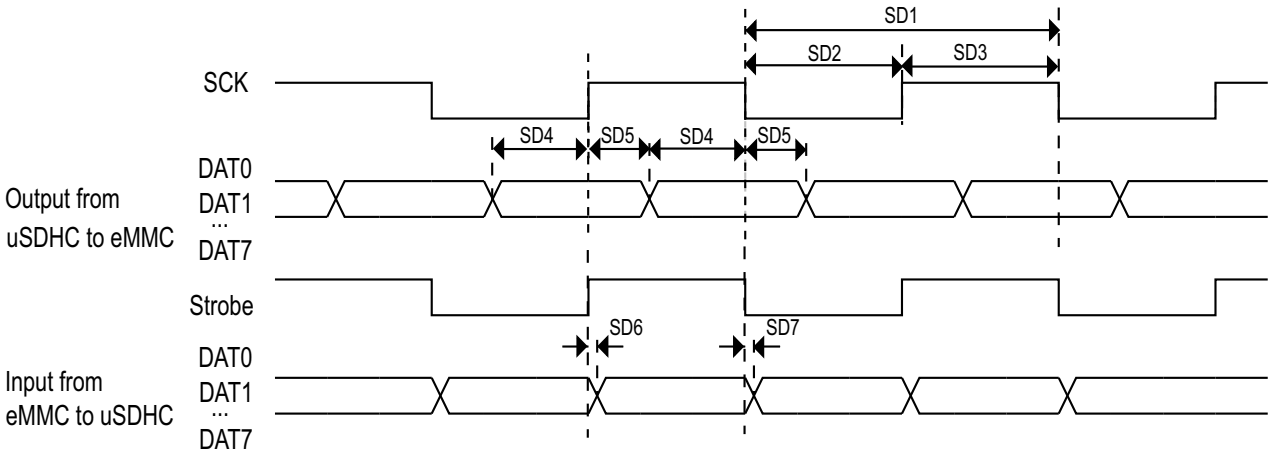

Figure 13. HS400 Mode timing

Table 42. HS400 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock frequency	f_{PP}	0	200	MHz
SD2	Clock low time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock high time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs DAT (Reference to SCK)					
SD4	Output skew from data of edge of SCK	t_{OSkew1}	0.45	—	ns
SD5	Output skew from edge of SCk to data	t_{OSkew2}	0.45	—	ns
uSDHC Input/Card Outputs DAT (Reference to Strobe)					

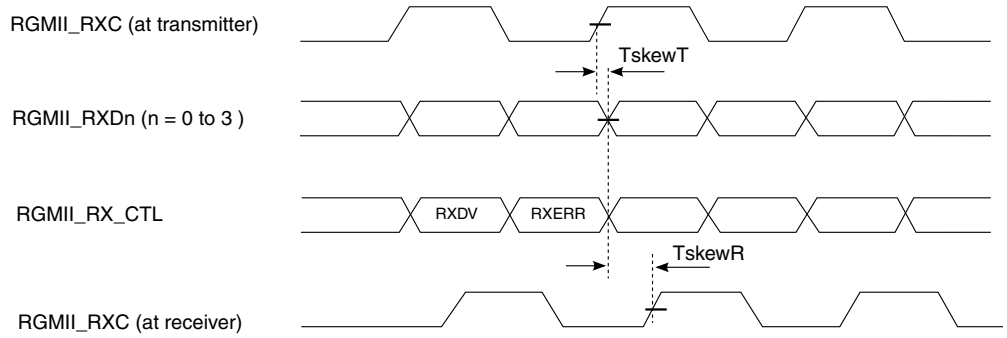

Figure 18. RGMII receive signal timing diagram original

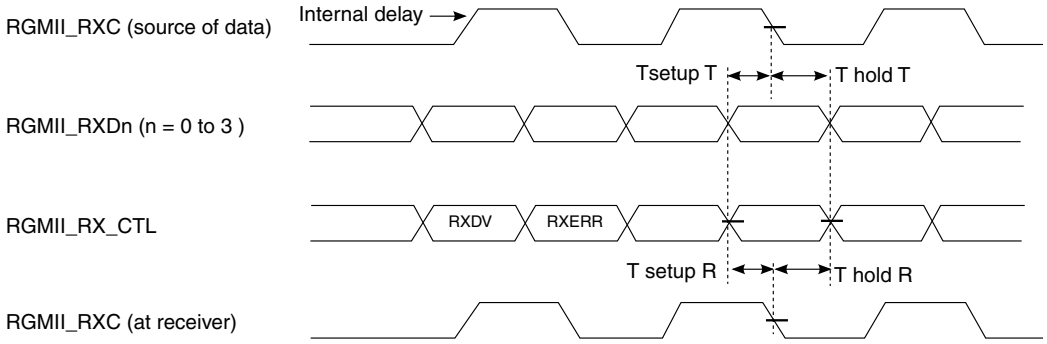

Figure 19. RGMII receive signal timing diagram with internal delay

3.9.4 General-purpose media interface (GPMI) timing

The GMPI controller of the i.MX 8M Dual / 8M QuadLite / 8M Quad processor is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous Timing mode, Source Synchronous Timing mode and Toggle Timing mode separately, as described in the following subsections.

3.9.4.1 Asynchronous mode AC timing (ONFI 1.0 compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 20 through Figure 23 depicts the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 47 describes the timing parameters (NF1–NF17) that are shown in the figures.

Table 52. MIPI high-speed transmitter AC specifications

Symbol	Parameter	Min	Typ	Max	Unit
$\Delta V_{CMTX(HF)}$	Common-level variations above 450 MHz	—	—	8	mV_{RMS}
$\Delta V_{CMTX(LF)}$	Common-level variation between 50-450 MHz	—	—	10	mV_{PEAK}
t_R and t_F[1]	Rise Time and Fall Time (20% to 80%)	160	—	0.3 UI	ps

1 UI is the long-term average unit interval.

3.9.7.2 MIPI LP-TX specifications

Table 53. MIPI low-power transmitter DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}[1]	Thevenin Output High Level	1.1	1.2	1.3	V
V_{OL}	Thevenin Output Low Level	-50	—	50	mV
Z_{OLP}[2]	Output Impedance of Low Power Transmitter	110	—	—	Ω

1 This specification can only be met when limiting the core supply variation from 1.1 V to 1.3 V.

2 Although there is no specified maximum for Z_{OLP}, the LP transmitter output impedance ensures the T_{RLP}/T_{FLP} specification is met.

Table 54. MIPI low-power transmitter AC specifications

Symbol	Parameter	Min	Typ	Max	Unit
T_{RLP}/T_{FLP}[1]	15% to 85% Rise Time and Fall Time	—	—	25	ns
T_{REOT}[1,2,3]	30% to 85% Rise Time and Fall Time	—	—	35	ns
$T_{LP-PULSE-TX}$[4]	Pulse width of the LP exclusive-OR clock: First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40	—	—	ns
	Pulse width of the LP exclusive-OR clock: All other pulses	20	—	—	ns
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock	90	—	—	ns
$\delta V/\delta t_{SR}$[1,5,6,7]	Slew Rate @ C_{LOAD} = 0 pF	30	—	500	mV/ns
	Slew Rate @ C_{LOAD} = 5 pF	30	—	200	mV/ns
	Slew Rate @ C_{LOAD} = 20 pF	30	—	150	mV/ns
	Slew Rate @ C_{LOAD} = 70 pF	30	—	100	mV/ns
C_{LOAD}	Load Capacitance	0	—	70	pF

1 C_{LOAD} includes the low equivalent transmission line capacitance of TX and RX are assumed to always be < 10 pF. The distributed line capacitance can be up to 50 pF for a transmission line with 2 ns delay.

2 The rise-time of T_{REOT} starts from the HS common-level at the moment when the differential amplitude drops below 70 mV, due to stopping of the differential drive.

3 With an additional load capacitance CCM between 0 to 60 pF on the termination center, tap at RX side of the lane.

4 This parameter value can be lower than TLPX, due to differences in rise vs. fall signal slopes, trip levels, and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior as described in Low-Power Receiver section.

3.9.10.2 DDR mode

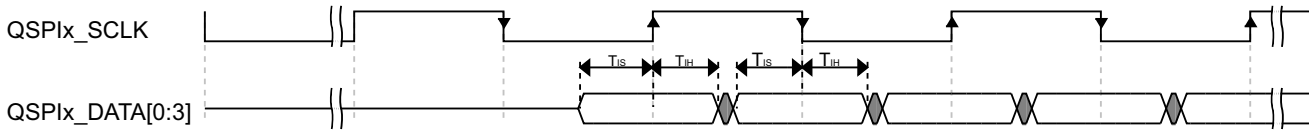

Figure 35. QuadSPI input/read timing (DDR mode with internal sampling)

Table 63. QuadSPI input/read timing (DDR mode with internal sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time requirement for incoming data	0	—	ns

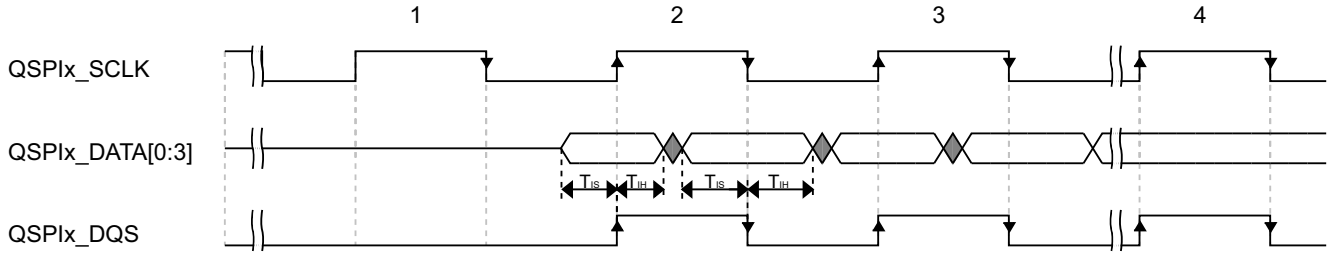

Figure 36. QuadSPI input/read timing (DDR mode with loopback DQS sampling)

Table 64. QuadSPI input/read timing (DDR mode with loopback DQS sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	2	—	ns
T_{IH}	Hold time requirement for incoming data	1	—	ns

NOTE

- For internal sampling, the timing values assume using sample point 0, that is QuadSPIx_SMPR[SDRSMP] = 0.

Table 66. Master mode SAI timing (continued)

Num	Characteristic	Min	Max	Unit
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period
S5	SAI_BCLK to SAI_FS output valid	—	15	ns
S6	SAI_BCLK to SAI_FS output invalid	0	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	15	ns
S8	SAI_BCLK to SAI_TXD invalid	0	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	15	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

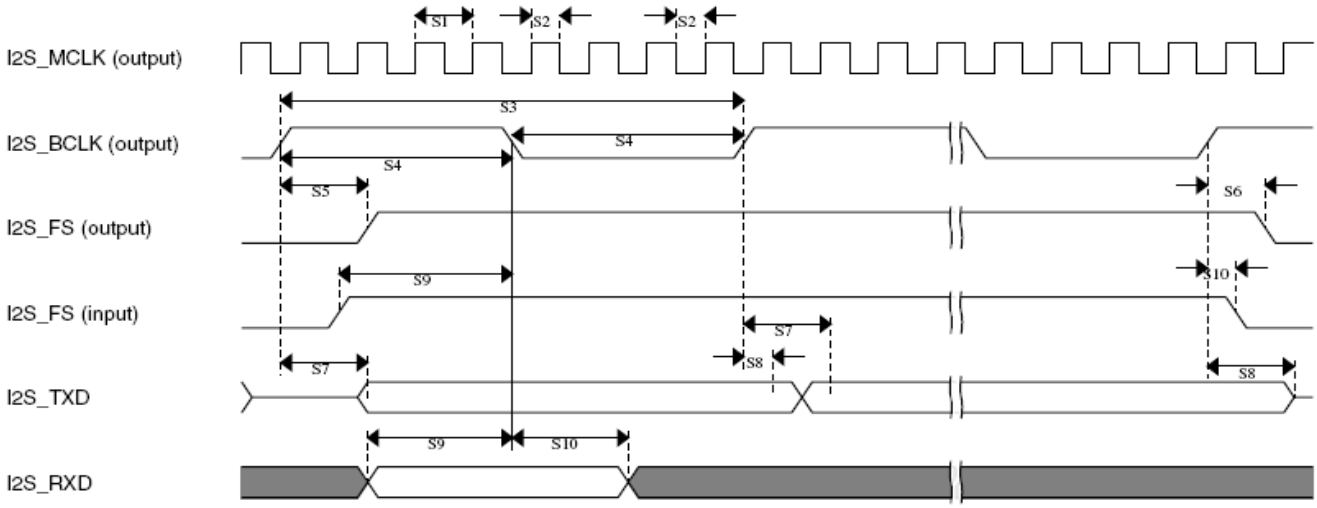

Figure 38. SAI timing—Master modes

Table 67. Slave mode SAI timing

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	40	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	—	ns
S14	SAI_FA input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	20	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns
S17	SAI_RXD setup before SAI_BCLK	10	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

Table 76. USB power pin supplies (continued)

Pin Name	Description	Value
USB1/2_VPTX	PHY transmit supply	0.9 V (+22.2%, -7%)
USB1/2_VDD33	High supply for high-speed operation IO	3.3 V (+10%, -7%)
USB1/2_VPH	High supply for SuperSpeed operation IO	3.3 V (+10%, -7%)

Table 77 shows the external component values.

Table 77. External component values

Component	Pin Name	Value
External resistor (resref)	USB1_RESREF/USB2_RESREF	200 Ω (±1%)

Table 78 shows the minimum ESD protection target levels.

Table 78. Minimum ESD protection target levels

ESD Category	Minimum Protection Level	JEDEC Class
Human Body Model (HBM) (JS-001-2014)	2 KV	2
Charged Device Model (CDM) (JESD22-C101F)	6 A peak discharge current	C2/C1 (500 V/ 250 V)[1]
Machine Model (MM) (JESD22_A115C)	100 V	N/A

1 Support for either 500 V or 250 V CDM target level is dependent on maximum discharge current generated in final SoC/package implementation.

Table 79 shows the supply impedance requirements.

Table 79. Supply impedance requirements

$L_{gd} + L_{vp}$(nH)	L_{VSSA}<#> + L_{DVDD}(nH)	$L_{gd} + L_{vptx}$<#>(nH)	L_{VSSA}<#> + L_{VDD33} <#>(nH)	$L_{gd} + L_{vph}$(nH)
< 2.4	< 2.4	< 2.4	< 2.8	< 2.8

Table 83. i.MX 8M Dual / 8M QuadLite / 8M Quad 17 x 17 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type[1]	Reset condition[2]			
				Default mode (Reset mode)	Default function (Signal name)	Input/ Output	Value
ECSPI2_SCLK	C5	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[10]	Input	PD (90 K)
ECSPI2_SS0	A5	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[13]	Input	PD (90 K)
ENET_MDC	N20	NVCC_ENET	GPIO	ALT5	GPIO1.IO[16]	Input	PD (90 K)
ENET_MDIO	N19	NVCC_ENET	GPIO	ALT5	GPIO1.IO[17]	Input	PD (90 K)
ENET_RD0	U19	NVCC_ENET	GPIO	ALT5	GPIO1.IO[26]	Input	PD (90 K)
ENET_RD1	U21	NVCC_ENET	GPIO	ALT5	GPIO1.IO[27]	Input	PD (90 K)
ENET_RD2	U20	NVCC_ENET	GPIO	ALT5	GPIO1.IO[28]	Input	PD (90 K)
ENET_RD3	V19	NVCC_ENET	GPIO	ALT5	GPIO1.IO[29]	Input	PD (90 K)
ENET_RXC	T20	NVCC_ENET	GPIO	ALT5	GPIO1.IO[25]	Input	PD (90 K)
ENET_RX_CTL	T21	NVCC_ENET	GPIO	ALT5	GPIO1.IO[24]	Input	PD (90 K)
ENET_TD0	R20	NVCC_ENET	GPIO	ALT5	GPIO1.IO[21]	Input	PD (90 K)
ENET_TD1	R21	NVCC_ENET	GPIO	ALT5	GPIO1.IO[20]	Input	PD (90 K)
ENET_TD2	R19	NVCC_ENET	GPIO	ALT5	GPIO1.IO[19]	Input	PD (90 K)
ENET_TD3	P20	NVCC_ENET	GPIO	ALT5	GPIO1.IO[18]	Input	PD (90 K)
ENET_TXC	T19	NVCC_ENET	GPIO	ALT5	GPIO1.IO[23]	Input	PD (90 K)
ENET_TX_CTL	P19	NVCC_ENET	GPIO	ALT5	GPIO1.IO[22]	Input	PD (90 K)
GPIO1_IO00	T6	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[0]	Input	PD (90 K)
GPIO1_IO01[3]	T7	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[1]	Input	PD (90 K)
GPIO1_IO02	R4	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[2]	Input	PD (27 K)
GPIO1_IO03	P4	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[3]	Input	PD (90 K)
GPIO1_IO04	P5	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[4]	Input	PD (90 K)
GPIO1_IO05[4]	P7	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[5]	Input	PU (27 K)
GPIO1_IO06	N5	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[6]	Input	PD (90 K)
GPIO1_IO07	N6	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[7]	Input	PD (90 K)
GPIO1_IO08	N7	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[8]	Input	PD (90 K)
GPIO1_IO09	M6	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[9]	Input	PD (90 K)
GPIO1_IO10	M7	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[10]	Input	PD (90 K)
GPIO1_IO11	L6	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[11]	Input	PD (90 K)
GPIO1_IO12	L7	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[12]	Input	PD (90 K)
GPIO1_IO13	K6	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[13]	Input	PD (90 K)

Table 83. i.MX 8M Dual / 8M QuadLite / 8M Quad 17 x 17 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type[1]	Reset condition[2]			
				Default mode (Reset mode)	Default function (Signal name)	Input/ Output	Value
JTAG_TDO	U5	NVCC_JTAG	GPIO	ALT0	cjtag_wrapper.TDO	Input	PU (27 K)
JTAG_TMS	V5	NVCC_JTAG	GPIO	ALT0	cjtag_wrapper.TMS	Input	PU (27 K)
JTAG_TRST_B	U6	NVCC_JTAG	GPIO	ALT0	cjtag_wrapper.TRST_B	Input	PU (27 K)
MIPI_CSI1_CLK_N	A22	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI1_CLK_P	B22	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI1_D0_N	A23	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI1_D0_P	B23	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI1_D1_N	C22	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI1_D1_P	D22	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI1_D2_N	B24	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI1_D2_P	C23	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI1_D3_N	C21	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI1_D3_P	D21	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI2_CLK_N	A19	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI2_CLK_P	B19	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI2_D0_N	C20	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI2_D0_P	D20	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI2_D1_N	A20	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI2_D1_P	B20	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI2_D2_N	A21	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI2_D2_P	B21	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI2_D3_N	C19	MIPI_VDDHA	PHY	—	—	—	—
MIPI_CSI2_D3_P	D19	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_CLK_N	C16	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_CLK_P	D16	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_D0_N	A17	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_D0_P	B17	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_D1_N	A16	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_D1_P	B16	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_D2_N	A18	MIPI_VDDHA	PHY	—	—	—	—

Table 83. i.MX 8M Dual / 8M QuadLite / 8M Quad 17 x 17 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type[1]	Reset condition[2]			
				Default mode (Reset mode)	Default function (Signal name)	Input/ Output	Value
MIPI_DSI_D2_P	B18	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_D3_N	A15	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_D3_P	B15	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_REXT	C17	MIPI_VDDHA	PHY	—	—	—	—
NAND_ALE	G19	NVCC_NAND	GPIO	ALT5	GPIO3.IO[0]	Input	PD (90 K)
NAND_CE0_B	H19	NVCC_NAND	GPIO	ALT5	GPIO3.IO[1]	Input	PD (90 K)
NAND_CE1_B	G21	NVCC_NAND	GPIO	ALT5	GPIO3.IO[2]	Input	PD (90 K)
NAND_CE2_B	F21	NVCC_NAND	GPIO	ALT5	GPIO3.IO[3]	Input	PD (90 K)
NAND_CE3_B	H20	NVCC_NAND	GPIO	ALT5	GPIO3.IO[4]	Input	PD (90 K)
NAND_CLE	H21	NVCC_NAND	GPIO	ALT5	GPIO3.IO[5]	Input	PD (90 K)
NAND_DATA00	G20	NVCC_NAND	GPIO	ALT5	GPIO3.IO[6]	Input	PD (90 K)
NAND_DATA01	J20	NVCC_NAND	GPIO	ALT5	GPIO3.IO[7]	Input	PD (90 K)
NAND_DATA02	H22	NVCC_NAND	GPIO	ALT5	GPIO3.IO[8]	Input	PD (90 K)
NAND_DATA03	J21	NVCC_NAND	GPIO	ALT5	GPIO3.IO[9]	Input	PD (90 K)
NAND_DATA04	L20	NVCC_NAND	GPIO	ALT5	GPIO3.IO[10]	Input	PD (90 K)
NAND_DATA05	J22	NVCC_NAND	GPIO	ALT5	GPIO3.IO[11]	Input	PD (90 K)
NAND_DATA06	L19	NVCC_NAND	GPIO	ALT5	GPIO3.IO[12]	Input	PD (90 K)
NAND_DATA07	M19	NVCC_NAND	GPIO	ALT5	GPIO3.IO[13]	Input	PD (90 K)
NAND_DQS	M20	NVCC_NAND	GPIO	ALT5	GPIO3.IO[14]	Input	PD (90 K)
NAND_RE_B	K19	NVCC_NAND	GPIO	ALT5	GPIO3.IO[15]	Input	PD (90 K)
NAND_READY_B	K20	NVCC_NAND	GPIO	ALT5	GPIO3.IO[16]	Input	PD (90 K)
NAND_WE_B	K22	NVCC_NAND	GPIO	ALT5	GPIO3.IO[17]	Input	PD (90 K)
NAND_WP_B	K21	NVCC_NAND	GPIO	ALT5	GPIO3.IO[18]	Input	PD (90 K)
ONOFF	W21	NVCC_SNVS	GPIO	ALT0	snvsmix.ONOFF	Input	PU (27 K)
PCIE1_REF_PAD_CLK_N	K24	PCIE_VPH	PHY	—	—	—	—
PCIE1_REF_PAD_CLK_P	K25	PCIE_VPH	PHY	—	—	—	—
PCIE1_RESREF	G25	PCIE_VPH	PHY	—	—	—	—
PCIE1_RXN_N	H24	PCIE_VPH	PHY	—	—	—	—

Table 83. i.MX 8M Dual / 8M QuadLite / 8M Quad 17 x 17 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type[1]	Reset condition[2]			
				Default mode (Reset mode)	Default function (Signal name)	Input/ Output	Value
SAI1_TXD0[5]	F2	NVCC_SAI1	GPIO	ALT5	GPIO4.IO[12]	Input	PD (90 K)
SAI1_TXD1[5]	E2	NVCC_SAI1	GPIO	ALT5	GPIO4.IO[13]	Input	PD (90 K)
SAI1_TXD2[5]	B2	NVCC_SAI1	GPIO	ALT5	GPIO4.IO[14]	Input	PD (90 K)
SAI1_TXD3[5]	D1	NVCC_SAI1	GPIO	ALT5	GPIO4.IO[15]	Input	PD (90 K)
SAI1_TXD4[5]	D2	NVCC_SAI1	GPIO	ALT5	GPIO4.IO[16]	Input	PD (90 K)
SAI1_TXD5[5]	C2	NVCC_SAI1	GPIO	ALT5	GPIO4.IO[17]	Input	PD (90 K)
SAI1_TXD6[5]	B3	NVCC_SAI1	GPIO	ALT5	GPIO4.IO[18]	Input	PD (90 K)
SAI1_TXD7[5]	C1	NVCC_SAI1	GPIO	ALT5	GPIO4.IO[19]	Input	PD (90 K)
SAI1_TXFS	H1	NVCC_SAI1	GPIO	ALT5	GPIO4.IO[10]	Input	PD (90 K)
SAI2_MCLK	H5	NVCC_SAI2	GPIO	ALT5	GPIO4.IO[27]	Input	PD (90 K)
SAI2_RXC	H3	NVCC_SAI2	GPIO	ALT5	GPIO4.IO[22]	Input	PD (90 K)
SAI2_RXD0	H6	NVCC_SAI2	GPIO	ALT5	GPIO4.IO[23]	Input	PD (90 K)
SAI2_RXFS	J4	NVCC_SAI2	GPIO	ALT5	GPIO4.IO[21]	Input	PD (90 K)
SAI2_TXC	J5	NVCC_SAI2	GPIO	ALT5	GPIO4.IO[25]	Input	PD (90 K)
SAI2_TXD0	G5	NVCC_SAI2	GPIO	ALT5	GPIO4.IO[26]	Input	PD (90 K)
SAI2_TXFS	H4	NVCC_SAI2	GPIO	ALT5	GPIO4.IO[24]	Input	PD (90 K)
SAI3_MCLK	D3	NVCC_SAI3	GPIO	ALT5	GPIO5.IO[2]	Input	PD (90 K)
SAI3_RXC	F4	NVCC_SAI3	GPIO	ALT5	GPIO4.IO[29]	Input	PD (90 K)
SAI3_RXD	F3	NVCC_SAI3	GPIO	ALT5	GPIO4.IO[30]	Input	PD (90 K)
SAI3_RXFS	G4	NVCC_SAI3	GPIO	ALT5	GPIO4.IO[28]	Input	PD (90 K)
SAI3_TXC	C4	NVCC_SAI3	GPIO	ALT5	GPIO5.IO[0]	Input	PD (90 K)
SAI3_TXD	C3	NVCC_SAI3	GPIO	ALT5	GPIO5.IO[1]	Input	PD (90 K)
SAI3_TXFS	G3	NVCC_SAI3	GPIO	ALT5	GPIO4.IO[31]	Input	PD (90 K)
SAI5_MCLK	K4	NVCC_SAI5	GPIO	ALT5	GPIO3.IO[25]	Input	PD (90 K)
SAI5_RXC	L5	NVCC_SAI5	GPIO	ALT5	GPIO3.IO[20]	Input	PD (90 K)
SAI5_RXD0	M5	NVCC_SAI5	GPIO	ALT5	GPIO3.IO[21]	Input	PD (90 K)
SAI5_RXD1	L4	NVCC_SAI5	GPIO	ALT5	GPIO3.IO[22]	Input	PD (90 K)
SAI5_RXD2	M4	NVCC_SAI5	GPIO	ALT5	GPIO3.IO[23]	Input	PD (90 K)
SAI5_RXD3	K5	NVCC_SAI5	GPIO	ALT5	GPIO3.IO[24]	Input	PD (90 K)
SAI5_RXFS	N4	NVCC_SAI5	GPIO	ALT5	GPIO3.IO[19]	Input	PD (90 K)