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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A53
Number of Cores/Bus Width	4 Core, 64-Bit
Speed	1.5GHz
Co-Processors/DSP	ARM® Cortex®-M4
RAM Controllers	DDR3L, DDR4, LPDDR4
Graphics Acceleration	Yes
Display & Interface Controllers	eDP, HDMI, MIPI-CSI, MIPI-DSI
Ethernet	GbE
SATA	-
USB	USB 3.0 (2)
Voltage - I/O	-
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, CAAM, HAB, RDC, RTC, SJC, SNVS
Package / Case	621-FBGA, FCBGA
Supplier Device Package	621-FCPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mimx8mq5dvajzaa

2 Modules list

The i.MX 8M Dual / 8M QuadLite / 8M Quad of processors contain a variety of digital and analog modules. Table 3 describes these modules in alphabetical order.

Table 3. i.MX 8M Dual / 8M QuadLite / 8M Quad modules list

Block mnemonic	Block name	Brief description
APBH-DMA	NAND Flash and BCH ECC DMA Controller	DMA controller used for GPMI2 operation.
Arm	Arm Platform	The Arm Core Platform includes a quad Cortex-A53 core and a Cortex-M4 core. The Cortex-A53 core includes associated sub-blocks, such as the Level 2 Cache Controller, Snoop Control Unit (SCU), General Interrupt Controller (GIC), private timers, watchdog, and CoreSight debug modules. The Cortex-M4 core is used as a customer microcontroller.
BCH	Binary-BCH ECC Processor	The BCH module provides up to 62-bit ECC encryption/decryption for NAND Flash controller (GPMI)
CAAM	Cryptographic accelerator and assurance module	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, entropy source generator, and a Pseudo Random Number Generator (PRNG). The PRNG is certifiable by the Cryptographic Algorithm Validation Program (CAVP) of the National Institute of Standards and Technology (NIST). CAAM also implements a Secure Memory mechanism. In i.MX 8M Dual / 8M QuadLite / 8M Quad processors, the secure memory provided is 32 KB.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSU	Central Security Unit	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 8M Dual / 8M QuadLite / 8M Quad platform.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interface	Cross Trigger Interface (CTI) allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A53 core platform.
DAP	Debug Access Port	The DAP provides real-time access for the debugger without halting the core to access: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains.
DC	Display Controller	Dual display controller
DDRC	Double Data Rate Controller	The DDR Controller has the following features: • Supports 32/16-bit LPDDR4-3200, DDR4-2400, and DDR3L-1600 • Supports up to 8 Gbyte DDR memory space
eCSPI1 eCSPI2 eCSPI3	Configurable SPI	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. Configurable to support Master/Slave modes, four chip selects to support multiple peripherals.

Table 5. Absolute maximum ratings (continued)

Parameter description	Symbol	Min	Max	Unit	Notes
GPIO supply voltage	NVCC_JTAG, NVCCGPIO1, NVCC_ENT, NVCC_SD1, NVCC_SD2, NVCC_NAND, NVCC_SA1, NVCC_SAI2, NVCC_SAI3, NVCC_SAI5, NVCC_ECSPI, NVCC_I2C, NVCC_UART	0	3.6	V	1.8 V mode/3.3 V mode
SNVS IO supply voltage	NVCC_SNVS	0	3.6	V	3.3 V mode only
VDD_SNVS supply voltage	VDD_SNVS	0	0.99	V	—
USB high supply voltage	USB1_VDD33, USB1_VPH, USB2_VDD33, USB2_VPH	0	3.63	V	—
USB_VBUS input detected	USB1_VBUS, USB2_VBUS	0	5.25	V	—
Input voltage on USB*_DP, USB*_DN pins	USB1_DP/USB1_DN USB2_DP/USB2_DN	0	USB1_VDD33 USB2_VDD33	V	—
Input/output voltage range	V_{in}/V_{out}	0	OVDD[1]+0.3	V	—
ESD damage immunity: • Human Body Model (HBM) • Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V	—
Storage temperature range	$T_{STORAGE}$	–40	150	°C	—

1 OVDD is the I/O supply voltage.

3.1.2 Thermal resistance

3.1.2.1 FPBGA package thermal resistance

Table 6 displays the thermal resistance data.

Table 6. Thermal resistance data

Rating	Test conditions	Symbol	17 x 17 pkg value	Unit
Junction to Ambient[1]	Single-layer board (1s); natural convection[2] Four-layer board (2s2p); natural convection[2]	$R_{\theta JA}$ $R_{\theta JA}$	Bare die: 16.4	°C/W °C/W
Junction to Ambient[1]	Single-layer board (1s); airflow 200 ft/min[2,3] Four-layer board (2s2p); airflow 200 ft/min[2,3]	$R_{\theta JA}$ $R_{\theta JA}$	Bare die: 13.9	°C/W °C/W
Junction to Board[1,4]	—	$R_{\theta JB}$	Bare die: 4.6	°C/W
Junction to Case[1,5]	—	$R_{\theta JC}$	Bare die: 0.1	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-2 with the single layer board horizontal. Thermal test board meets JEDEC specification for the specified package.

Table 7. Operating ranges (continued)

Parameter description	Symbol	Min	Typ	Max[1]	Unit	Comment
MIPI supply voltage	MIPI_VDDA	0.81	0.9/1.0	1.1	V	Analog core power supply
	MIPI_VDDHA	1.62	1.8	1.98	V	Analog IO power supply
	MIPI_VDD	0.81	0.9/1.0	1.1	V	Digital core power supply
	MIPI_VDDPLL	0.81	0.9/1.0	1.1	V	Analog supply for MIPI PLL
Voltage rails supplied from 1.8 V PHY	PCIE_VPH	1.674 3.069	1.8 3.3	1.98 3.63	V	Supplied from PMIC
	PCIE_VP, PCIE_VPTX	0.837	0.9	0.99	V	Supplied from PMIC
Temperature sensor accuracy	T_{delta}	—	±3	—	°C	Typical accuracy over the range –40°C to 125°C
Fuse power	EFUSE_VQPS	1.71	1.8	1.98	V	Power supply for internal use
Junction temperature, consumer	T_J	0	—	+95	°C	See Table 2 for complete list of junction temperature capabilities.

1 Applying the maximum voltage results in maximum power consumption and heat generation. A voltage set point = (Vmin + the supply tolerance) is recommended. This result in an optimized power/speed ratio.

3.1.4 External clock sources

A 25 MHz oscillator is used as the primary clock source for the PLLs to generate the clock for CPU, BUS, and high-speed interfaces. For fractional PLLs, the 25 MHz clock from the oscillator can be directly used as the PLL reference clock.

A 27 MHz oscillator is used as the reference clock for HDMI PHY. Also it can be used as the alternative source for the fractional PLLs.

A 32 kHz clock input pin is used as the RTC clock source. It is expected to be supplied by an external 32.768 kHz oscillator. When an external RTC clock input is not present, the 32 kHz clock for internal logic is generated by the 25 MHz oscillator. The frequency of the internal 32 kHz clock will be 31.25 kHz.

Two pairs of differential clock inputs, named as CLK1P and CLK1N, can be used as the reference clock for the PLL. This is mainly used for a high-speed clock input during testing.

Four clock inputs to the CCM from normal GPIO pads via IOMUX can be used as the clock sources in the CCM.

Table 8 shows the interface frequency requirements.

Table 8. External input clock frequency

Parameter description	Symbol	Min	Typ	Max	Unit
RTC[1,2]	f_{ckil}	—	32.768[3]	—	kHz
XTALI_25M/XTALO_25M[2]	f_{xtal}	20	25	40	MHz
XTALI_27M/XTALO_27M[2]	f_{xtal}	20	27	40	MHz

1 External oscillator or a crystal with internal oscillator amplifier.

- SNVS Mode: This mode is also called RTC mode. Only the power for the SNVS domain remains on to keep RTC and SNVS logic alive.
- OFF Mode: All power rails are off.

Table 10. Chip power in different LP mode

Mode	Supply	Max.[1]	Unit
SNVS	VDD_SNVS (1.0 V)	1.39	mA
	NVCC_SNVS (3.6 V)	4.25	
	Total[2]	17	mW
Deep Sleep Mode (DSM)	VDD_SOC (1.0 V)	148.50	mA
	VDDA_1P8 (2.0 V)	12.82	
	VDDA_0P9 (1.0 V)	0.30	
	VDDA_DRAM (1.8 V)	0.50	
	VDD_SNVS (1.0 V)	0.25	
	NVCC_SNVS (3.3 V)	4.80	
	NVCC_DRAM (1.17 V)	4.51	
	Total[2]	197	mW
IDLE	VDD_ARM (1.0 V)	152.10	mA
	VDD_SOC (1.0 V)	132.90	
	VDD_DRAM (1.0 V)	44.10	
	VDDA_1P8 (2.0 V)	13.53	
	VDDA_0P9 (1.0 V)	0.30	
	VDDA_DRAM (1.8 V)	1.32	
	VDD_SNVS (1.0 V)	0.25	
	NVCC_SNVS (3.3 V)	4.34	
	NVCC_DRAM (1.17 V)	13.12	
	Total[2]	389	mW
RUN	Total	1 to 4	mW

1 All the power numbers defined in the table are based on typical silicon at 25°C. Use case dependent

2 Sum of the listed supply rails.

Table 11 summarizes the external power supply states in all the power modes.

Table 11. The power supply states

Power rail	OFF	SNVS	SUSPEND	IDLE	RUN
VDD_ARM	OFF	OFF	OFF	ON	ON
VDD_SOC	OFF	OFF	ON	ON	ON

Table 11. The power supply states (continued)

Power rail	OFF	SNVS	SUSPEND	IDLE	RUN
VDD_GPU	OFF	OFF	OFF	OFF	ON/OFF
VDD_VPU	OFF	OFF	OFF	OFF	ON/OFF
VDD_DRAM	OFF	OFF	OFF	ON	ON
VDDA_0P9	OFF	OFF	ON	ON	ON
VDDA_1P8	OFF	OFF	ON	ON	ON
VDDA_DRAM	OFF	OFF	ON	ON	ON
VDD_SNVS	OFF	ON	ON	ON	ON
NVCC_SNVS	OFF	ON	ON	ON	ON
NVCC_<XXX>	OFF	OFF	ON	ON	ON
NVCC_DRAM	OFF	OFF	ON	ON	ON
DRAM_VREF	OFF	OFF	OFF	ON	ON

3.1.7 USB PHY Suspend current consumption

3.1.7.1 Low power Suspend Mode

The VBUS Valid comparators and their associated bandgap circuits are enabled by default. Table 12 shows the USB interface current consumption in Suspend mode with default settings.

Table 12. USB PHY current consumption in Suspend mode[1]

	USB1_VDD33	USB2_VDD33
Current	154 µA	154 µA

1 Low Power Suspend is enabled by setting USBx_PORTSC1 [PHCD]=1 [Clock Disable (PLPSCD)].

3.1.7.2 Power-Down modes

Table 13 shows the USB interface current consumption with only the OTG block powered down.

Table 13. USB PHY current consumption in Sleep mode[1]

	USB1_VDD33	USB2_VD33
Current	520 µA	520 µA

1 VBUS Valid comparators can be disabled through software by setting USBNC_OTG*_PHY_CFG2[OTGDISABLE0] to 1. This signal powers down only the VBUS Valid comparator, and does not control power to the Session Valid Comparator, ADP Probe and Sense comparators, or ID detection circuitry.

In Power-Down mode, everything is powered down, including the USB_VBUS valid comparators and their associated bandgap circuity in typical condition. Table 14 shows the USB interface current consumption in Power-Down mode.

Table 14. USB PHY current consumption in Power-Down mode[1]

	USB1_VDD33	USB2_VDD33
Current	146 µA	146 µA

1 The VBUS Valid Comparators and their associated bandgap circuits can be disabled through software by setting USBNC_OTG*_PHY_CFG2[OTGDISABLE0] to 1 and USBNC_OTG*_PHY_CFG2[DRVVBUS0] to 0, respectively.

3.1.8 PCIe PHY 2.1 DC electrical characteristics

Table 15. PCIe recommended operating conditions

Parameter	Description		Min	Max	Unit
PCIE_VP	Low Power Supply Voltage for PHY Core	—	0.837	0.99	V
PCIE_VPTX	PHY transmit supply	—	0.837	0.99	
PCIE_VPH	High Power Supply Voltage for PHY Core	1.8	1.674	1.98	
		3.3	3.069	3.63	

Table 15. PCIe recommended operating conditions (continued)

Parameter	Description	Min	Max	Unit
T_A	Commercial Temperature Range	0	70	°C
T_J	Simulation Junction Temperature Range	-40	125	°C

Note: V_{DD} should have no more than 40 mVpp AC power supply noise superimposed on the high power supply voltage for the PHY core (1.8 V nominal DC value). At the same time, VDD should have no more than 20 mVpp AC power supply noise superimposed on the low power supply voltage for the PHY core (1.0 V nominal value or 1.1 V overdrive DC value).
The power supply voltage variation for the PHY core should have less than ±5% including the board-level power supply variation and on-chip power supply variation due to the finite impedances in the package.

Table 16. PCIe DC electrical characteristics

Parameter	Description		Min	Typ	Max	Unit
PCIE1_VP, PCIE2_VP	Power Supply Voltage		0.9 - 7%	0.9	0.9 + 10%	V
PD	Power Consumption	Normal	—	40	—	mW
		Partial Mode	—	27	—	mW
		Slumber Mode	—	7	—	mW
		Full Powerdown	—	0.2	—	mW

Table 17. PCIe PHY high-speed characteristics

High Speed I/O Characteristics						
Description	**Symbol**	**Speed**	**Min.**	**Typ.**	**Max.**	**Unit**
Unit Interval	UI	2.5 Gbps	—	400	—	ps
		5.0 Gbps	—	200	—	
TX Serial output rise time (20% to 80%)	T_{TXRISE}	2.5 Gbps	100	—	—	ps
		5.0 Gbps	100	—	—	
TX Serial output fall time (80% to 20%)	T_{TXFALL}	2.5 Gbps	100	—	—	ps
		5.0 Gbps	100	—	—	
TX Serial data output voltage (Differential, pk–pk)	ΔV_{TX}	2.5 Gbps	800	—	1100	mVp–p
		5.0 Gbps	600	—	900	
PCIe Tx deterministic jitter < 1.5 MHz	TRJ	2.5 Gbps	3	—	—	ps, rms
		5.0 Gbps	3	—	—	
PCIe Tx deterministic jitter > 1.5 MHz	TDJ	2.5 Gbps	—	—	20	ps, pk–pk
		5.0 Gbps	—	—	10	

Table 17. PCIe PHY high-speed characteristics (continued)

High Speed I/O Characteristics						
Description	**Symbol**	**Speed**	**Min.**	**Typ.**	**Max.**	**Unit**
RX Serial data input voltage (Differential pk–pk)	ΔV_{RX}	2.5 Gbps	120	—	1200	mVp–p
		5.0 Gbps	120	—	1200	

Table 18. PCIe PHY reference clock timing requirements (vp is PIE_VP, 0.9 V power supply)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
FREF_OFFSET	Reference clock frequency offset	-300	—	30	ppm	—
DJREF_CLK	Reference clock cycle to cycle jitter	—	—	35	ps	DJ across all frequencies
DCREF_CLK	Duty cycle	40	—	60	%	—
VCMREF_CLK	Common mode input level	0	—	vp	V	Differential inputs
VDREF_CLK	Differential input swing	-0.3	—	—	V_{PP}	Differential inputs
VOLREF_CLK	Single-ended input logic low	-0.3	—	-0.3	V	If single-ended input is used.
VOHREF_CLK	Single-ended input logic high	vp - 0.3	—	vp + 0.3	V	If single-ended input is used.
SWREF_CLK	Input edge rate	—	—	—	V/ns	—
REF_CLK_SKEW	Reference clock skew (±)	—	—	200	ps	—

PCIe PHY interface is compliant with PCIe Express GEN2.

3.2 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

3.2.1 Power-up sequence

The i.MX 8M Dual / 8M QuadLite / 8M Quad processors have the following power-up sequence requirements:

- Turn on NVCC_SNVS
- Turn on VDD_SNVS
- RTC_RESET_B release
- Turn on VDD_SOC and VDDA_0P9

Table 20. PLL electrical parameters (continued)

PLL type	Parameter	Value
GPU_PLL	Clock output range	800 MHz ~1.6 GHz
	Reference clock	25 MHz
	Lock time	50 µs
VPU_PLL	Clock output range	400 MHz ~ 800 MHz
	Reference clock	25 MHz
	Lock time	50 µs

3.4 On-chip oscillators

3.4.1 OSC25M and OSC27M

A 25 MHz oscillator is used as the primary clock source for the PLLs to generate the clock for the CPU, BUS, and high-speed interfaces. For fractional PLLs, the 25 MHz clock from the oscillator can be used as the PLL reference clock directly.

A 27 MHz oscillator is used as the reference clock for HDMI PHY. It can also be used as the alternative source for the fractional PLLs.

Table 21 lists the electrical specifications of this oscillator when loaded with an NX5032GA 40 MHz crystal unit at 40 MHz frequency. All values are valid only for the device TJ operating specification of -40 ^{o}C to 125 ^{o}C.

Table 21. Electrical specification of oscillator @ 1.8 V

Parameter	Min	Typ	Max	Unit
Voltage swing on external pin[1]	250	—	800	mV
Power consumption (analog supply RMS current in OSC mode)[2, 3]	—	—	4	mA
Start-up time[1, 2]	—	—	2	ms

1 The start-up time is dependent upon crystal characteristics, board leakage, etc.; high ESR and excessive capacitive loads can cause long start-up time.

2 Electrical parameters are subject to change.

3 Maximum current is observed during startup. After oscillation is stable, the current from HV supply comes down.

Table 22 shows the transconductance specification of the oscillator (in mA/V).

Table 22. Transconductance specification of oscillator

GM_sel	Min	Max
111	10	25

3.5.2.1 LPDDR4 mode I/O DC parameters

Table 30. LPDDR4 I/O DC electrical parameters

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1 mA	0.9 x OVDD	—	V
Low-level output voltage	VOL	Iol= 0.1 mA	—	0.1 x OVDD	V
Input Reference Voltage	Vref	—	0.49 x OVDD	0.51 x OVDD	V
DC High-Level input voltage	Vih_DC	—	VRef + 0.100	OVDD	V
DC Low-Level input voltage	Vil_DC	—	OVSS	VRef – 0.100	V
Differential Input Logic High	Vih_diff	—	0.26	See note[1]	—
Differential Input Logic Low	Vil_diff	—	See note	-0.26	—
Pull-up/Pull-down Impedance Mismatch	Mmpupd	—	–15	15	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper Circuit Resistance	Rkeep	—	110	175	KΩ
Input current (no pull-up/down)	Iin	VI = 0, VI = OVDD	-2.5	2.5	µA

[1] The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

3.5.3 Differential I/O port (CLKx_P/N)

The clock I/O interface is designed to be compatible with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits* (2001), for details.

The CLK1_P/CLK1_N is input only, while CLK2_P/CLK2_N is output only.

3.6 I/O AC parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for DDR3L/DDR4/LPDDR4 modes
- Differential I/O (CLKx)

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 3 and Figure 4.

3.9.2 Ultra-high-speed SD/SDIO/MMC host interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (single data rate) timing, eMMC4.4/4.41 (dual data rate) timing and SDR104/50 (SD3.0) timing.

3.9.2.1 SD/eMMC4.3 (single data rate) AC timing

Figure 11 depicts the timing of SD/eMMC4.3, and Table 40 lists the SD/eMMC4.3 timing characteristics.

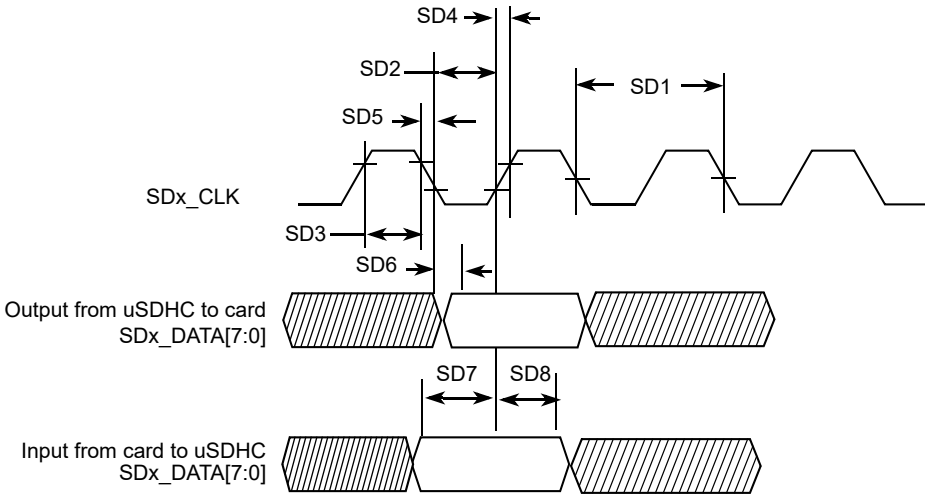

Figure 11. SD/eMMC4.3 timing

Table 40. SD/eMMC4.3 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	6.6	3.6	ns

3.9.2.5 SDR50/SDR104 AC timing

Figure 15 depicts the timing of SDR50/SDR104, and Table 44 lists the SDR50/SDR104 timing characteristics.

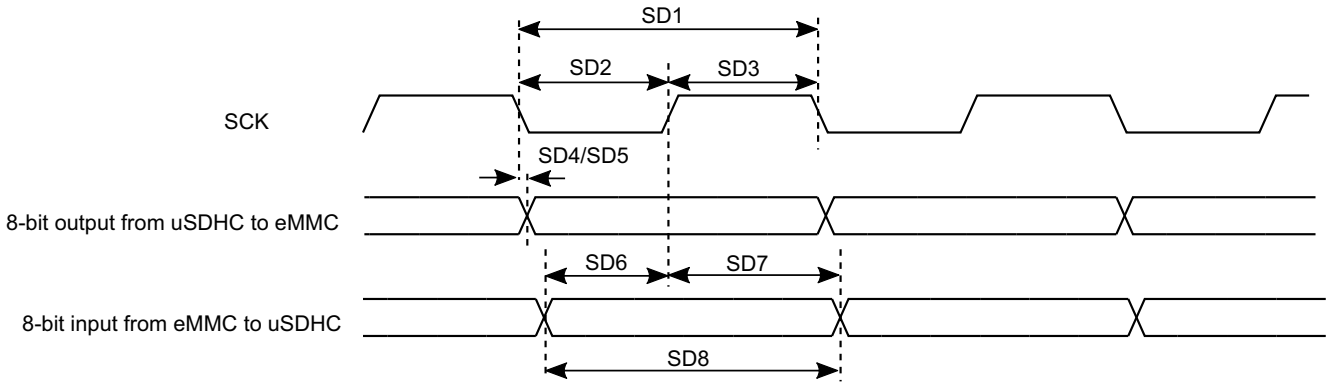

Figure 15. SDR50/SDR104 timing

Table 44. SDR50/SDR104 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5	—	ns
SD2	Clock Low Time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	-3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	-1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in DDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.4	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	uSDHC Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

[1] Data window in SDR100 mode is variable.

3.9.2.6 Bus operation condition for 3.3 V and 1.8 V signaling

Signaling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1, NVCC_SD2 and NVCC_SD3 supplies are identical to those shown in Table 26, "GPIO DC parameters," on page 29.

3.9.3.2 RGMII signal switching specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 46. RGMII signal switching specifications[1]

Symbol	Description	Min.	Max.	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-500	500	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	85	%
Duty_T[4]	Duty cycle for 10/100T	40	90	%
Tr/Tf	Rise/fall time (20–80%)	—	0.98	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; this implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

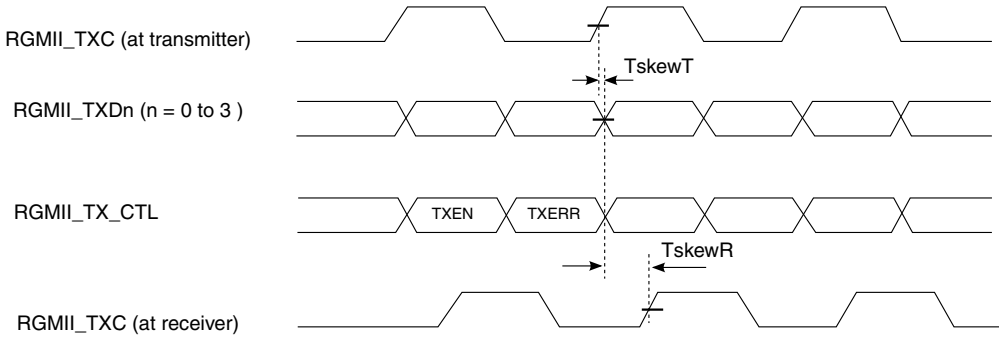

Figure 17. RGMII transmit signal timing diagram original

In EDO mode (Figure 23), NF16/NF17 are different from the definition in non-EDO mode (Figure 22). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical values for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI samples NAND_DATAxx at the rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the *i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processor Reference Manual* [IMX8MDQLQRM]). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

3.9.4.2 Source synchronous mode AC timing (ONFI 2.x compatible)

Figure 25 to Figure 27 show the write and read timing of Source Synchronous mode.

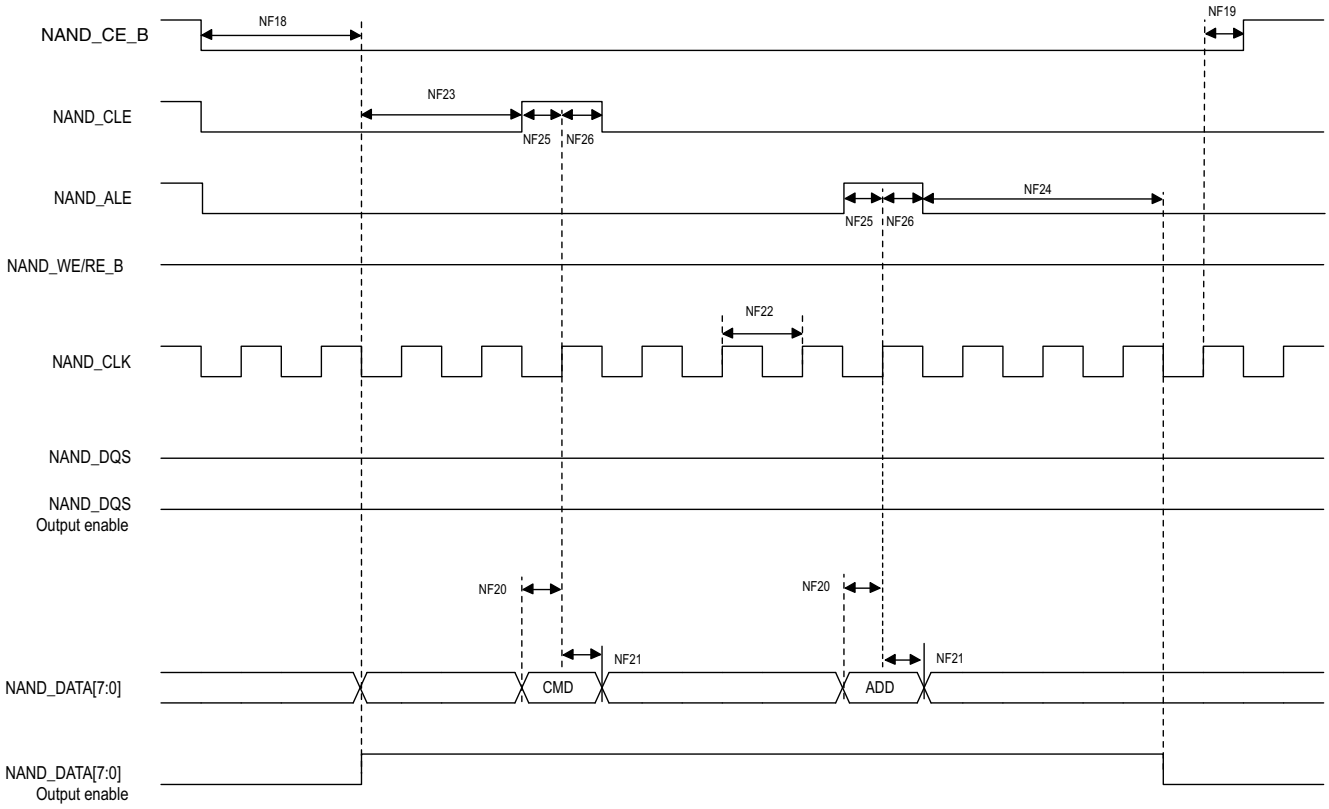

Figure 25. Source Synchronous mode command and address timing diagram

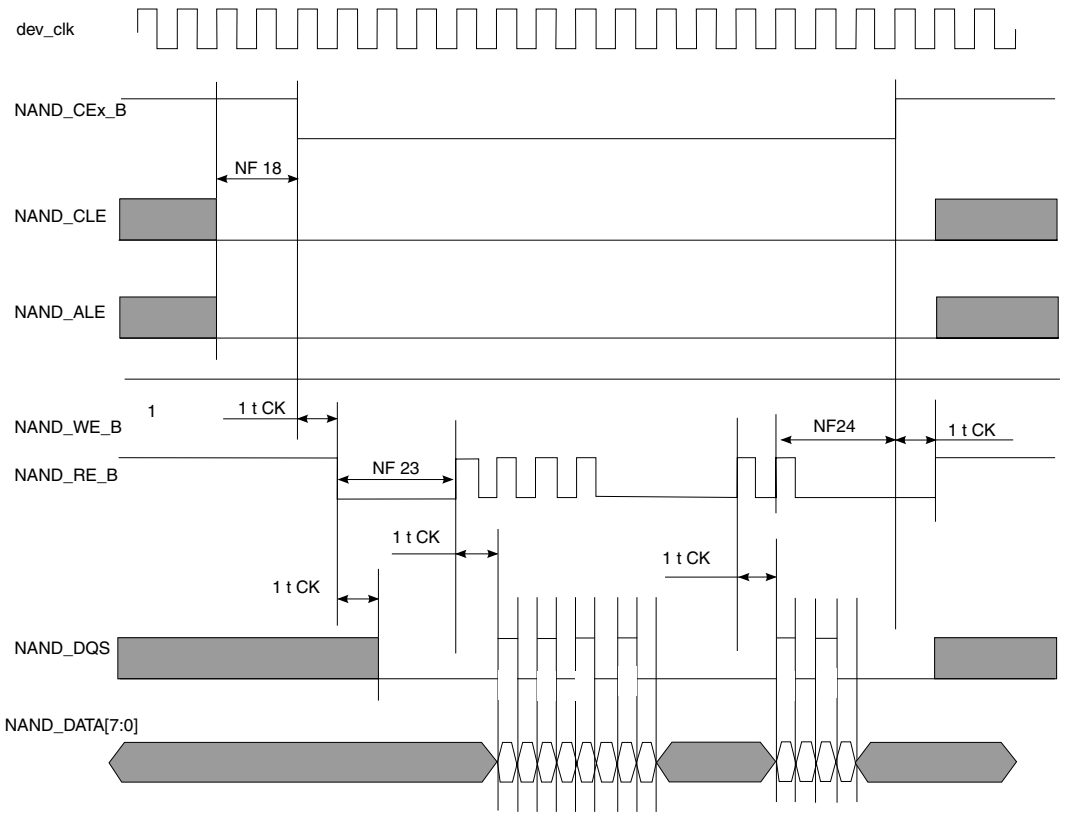

Figure 30. Toggle mode data read timing

Table 49. Toggle mode timing parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see note[2]s,[3]]		
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see note[2]]		
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see notes,[2]]		
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see note[2]]		
NF5	NAND_WE_B pulse width	tWP	DS × T [see note[2]]		
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see notes,[2]]		
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see note[2]]		
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see note[2]]		
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see note[2]]		
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see notes[4,2]]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	PRE_DELAY × T [see notes[5,2]]	—	ns

— HBR2: 1.62 x4 x 8 / 10 = 17.28 Gbps

Bandwidth required per resolution (CEA-861-F):

— 1920 x 1080 (24 b/px) 60 fps: 3.56 Gbps

— 3840 x 2160 (24 b/px) 30 fps: 7.13 Gbps

— 3840 x 2160 (24 b/px) 30 fps: 14.26 Gbps

- Embedded DisplayPort 1.4 standard (VESA.org)
  - — eDP link rates: R216 (2.16 Gbps), R243 (2.43 Gbps), R324 (3.24 Gbps), and R432 (4.32 Gbps)
  - — Fast Link Training is also supported

DDC link requires external pull-up resistors to be connected to a 5 V supply. The following table provides the range for those pull-ups.

Table 50. Pull-up resistors for DDC link

Ball Name	Min	Typ	Max	Unit
HDMI_TX0_DDC_SCL	1.5	—	2	KΩ
HDMI_TX0_DDC_SDA	1.5	—	2	KΩ

3.9.6 I^2C bus characteristics

The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave. The I2C is designed to be compatible with the I2C Bus Specification, version 2.1, by Philips Semiconductor (now NXP Semiconductors).

3.9.7 MIPI D-PHY timing parameters

This section describes MIPI D-PHY electrical specifications.

3.9.7.1 MIPI HS-TX specifications

Table 51. MIPI high-speed transmitter DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{CMTX}[1]	High Speed Transmit Static Common Mode Voltage	150	200	250	mV
$\|\Delta V_{CMTX}\|_{(1,0)}$	V_{CMTX} mismatch when Output is Differential-1 or Differential-0	—	—	3	mV
$\|V_{OD}\|$[1]	High Speed Transmit Differential Voltage	140	200	270	mV
$\|\Delta V_{OD}\|$	V_{OD} mismatch when Output is Differential-1 or Differential-0	—	—	12	mV
V_{OHHS}[1]	High Speed Output High Voltage	—	—	360	mV
Z_{OS}	Single Ended Output Impedance	40	50	62.5	Ω
ΔZ_{OS}	Single Ended Output Impedance Mismatch	—	—	10	%

[1] Value when driving into load impedance anywhere in the Z_{ID} range.

Measurement is with a load of 35 pF on SCK and SIO pins and an input slew rate of 1 V/ns.

3.9.10.1 SDR Mode

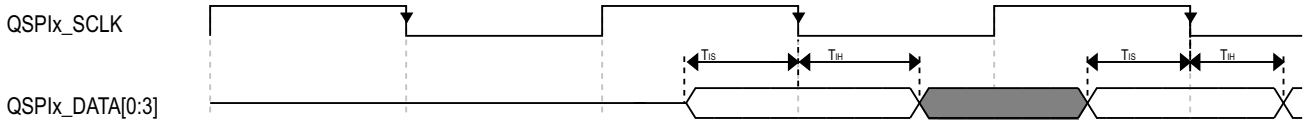

Figure 32. QuadSPI input/read timing (SDR mode with internal sampling)

Table 60. QuadSPI input timing (SDR mode with internal sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time requirement for incoming data	0	—	ns

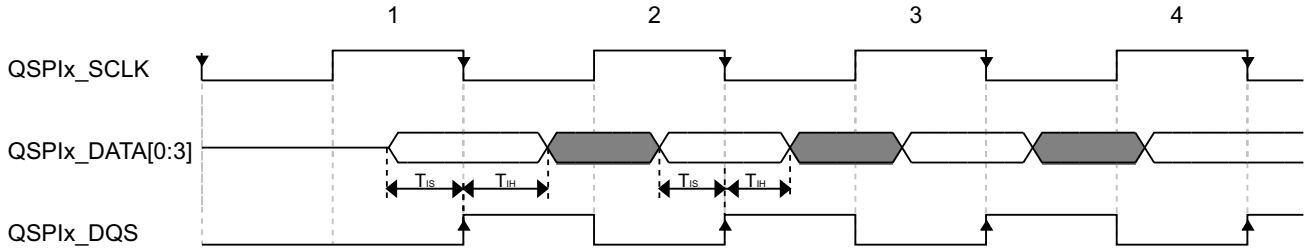

Figure 33. QuadSPI input/read timing (SDR mode with loopback DQS sampling)

Table 61. QuadSPI input/read timing (SDR mode with loopback DQS sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	2	—	ns
T_{IH}	Hold time requirement for incoming data	1	—	ns

NOTE

- For internal sampling, the timing values assume using sample point 0, that is QuadSPIx_SMPR[SDRSMP] = 0.

4.2 Boot device interface allocation

Table 81 lists the interfaces that can be used by the boot process in accordance with the specific Boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 81. Interface allocation during boot

Interface	IP Instance	Allocated Pads During Boot	Comment
NAND Flash	GPMI	NAND_ALE, NAND_CE0_B, NAND_CLE, NAND_DATA00, NAND_DATA01, NAND_DATA02, NAND_DATA03, NAND_DATA04, NAND_DATA05, NAND_DATA06, NAND_DATA07, NAND_DQS, NAND_RE_B, NAND_READY_B, NAND_WE_B, NAND_WP_B	8-bit, only CS0 is supported.
SD/MMC	USDHC-1	GPIO1_IO03, GPIO1_IO06, GPIO1_IO07, SD1_RESET_B, SD1_CLK, SD1_CMD, SD1_STROBE, SD1_DATA0, SD1_DATA1, SD1_DATA2, SD1_DATA3, SD1_DATA4, SD1_DATA5, SD1_DATA6, SD1_DATA7	1, 4, or 8-bit
SD/MMC	USDHC-2	GPIO1_IO04, GPIO1_IO08, GPIO1_IO07, SD2_RESET_B, SD2_CD_B, SD2_WP, SD2_CLK, SD2_CMD, SD2_DATA0, SD2_DATA1, SD2_DATA2, SD2_DATA3	1 or 4-bit
USB	USB_OTG PHY	—	—

Table 83. i.MX 8M Dual / 8M QuadLite / 8M Quad 17 x 17 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type[1]	Reset condition[2]			
				Default mode (Reset mode)	Default function (Signal name)	Input/ Output	Value
MIPI_DSI_D2_P	B18	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_D3_N	A15	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_D3_P	B15	MIPI_VDDHA	PHY	—	—	—	—
MIPI_DSI_REXT	C17	MIPI_VDDHA	PHY	—	—	—	—
NAND_ALE	G19	NVCC_NAND	GPIO	ALT5	GPIO3.IO[0]	Input	PD (90 K)
NAND_CE0_B	H19	NVCC_NAND	GPIO	ALT5	GPIO3.IO[1]	Input	PD (90 K)
NAND_CE1_B	G21	NVCC_NAND	GPIO	ALT5	GPIO3.IO[2]	Input	PD (90 K)
NAND_CE2_B	F21	NVCC_NAND	GPIO	ALT5	GPIO3.IO[3]	Input	PD (90 K)
NAND_CE3_B	H20	NVCC_NAND	GPIO	ALT5	GPIO3.IO[4]	Input	PD (90 K)
NAND_CLE	H21	NVCC_NAND	GPIO	ALT5	GPIO3.IO[5]	Input	PD (90 K)
NAND_DATA00	G20	NVCC_NAND	GPIO	ALT5	GPIO3.IO[6]	Input	PD (90 K)
NAND_DATA01	J20	NVCC_NAND	GPIO	ALT5	GPIO3.IO[7]	Input	PD (90 K)
NAND_DATA02	H22	NVCC_NAND	GPIO	ALT5	GPIO3.IO[8]	Input	PD (90 K)
NAND_DATA03	J21	NVCC_NAND	GPIO	ALT5	GPIO3.IO[9]	Input	PD (90 K)
NAND_DATA04	L20	NVCC_NAND	GPIO	ALT5	GPIO3.IO[10]	Input	PD (90 K)
NAND_DATA05	J22	NVCC_NAND	GPIO	ALT5	GPIO3.IO[11]	Input	PD (90 K)
NAND_DATA06	L19	NVCC_NAND	GPIO	ALT5	GPIO3.IO[12]	Input	PD (90 K)
NAND_DATA07	M19	NVCC_NAND	GPIO	ALT5	GPIO3.IO[13]	Input	PD (90 K)
NAND_DQS	M20	NVCC_NAND	GPIO	ALT5	GPIO3.IO[14]	Input	PD (90 K)
NAND_RE_B	K19	NVCC_NAND	GPIO	ALT5	GPIO3.IO[15]	Input	PD (90 K)
NAND_READY_B	K20	NVCC_NAND	GPIO	ALT5	GPIO3.IO[16]	Input	PD (90 K)
NAND_WE_B	K22	NVCC_NAND	GPIO	ALT5	GPIO3.IO[17]	Input	PD (90 K)
NAND_WP_B	K21	NVCC_NAND	GPIO	ALT5	GPIO3.IO[18]	Input	PD (90 K)
ONOFF	W21	NVCC_SNVS	GPIO	ALT0	snvsmix.ONOFF	Input	PU (27 K)
PCIE1_REF_PAD_CLK_N	K24	PCIE_VPH	PHY	—	—	—	—
PCIE1_REF_PAD_CLK_P	K25	PCIE_VPH	PHY	—	—	—	—
PCIE1_RESREF	G25	PCIE_VPH	PHY	—	—	—	—
PCIE1_RXN_N	H24	PCIE_VPH	PHY	—	—	—	—

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