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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A53
Number of Cores/Bus Width	4 Core, 64-Bit
Speed	1.5GHz
Co-Processors/DSP	ARM® Cortex®-M4
RAM Controllers	DDR3L, DDR4, LPDDR4
Graphics Acceleration	Yes
Display & Interface Controllers	eDP, HDMI, MIPI-CSI, MIPI-DSI
Ethernet	GbE
SATA	-
USB	USB 3.0 (2)
Voltage - I/O	-
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, CAAM, HAB, RDC, RTC, SJC, SNVS
Package / Case	621-FBGA, FCBGA
Supplier Device Package	621-FCPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mimx8mq6dvajzaa

Table 3. i.MX 8M Dual / 8M QuadLite / 8M Quad modules list (continued)

Block mnemonic	Block name	Brief description
MIPI CSI2 (four-lane)	MIPI Camera Serial Interface	This module provides two four-lane MIPI camera serial interfaces, each of them can operate up to a maximum bit rate of 1.5 Gbps.
MIPI DSI (four-lane)	MIPI Display Serial Interface	This module provides a four-lane MIPI display serial interface operating up to a maximum bit rate of 1.5 Gbps.
OCOTP_CTRL	OTP Controller	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent non volatility.
OCRAM	On-Chip Memory controller	The On-Chip Memory controller (OCRAM) module is designed as an interface between the system's AXI bus and the internal (on-chip) SRAM memory module. In i.MX 8M Dual / 8M QuadLite / 8M Quad processors, the OCRAM is used for controlling the 128 KB multimedia RAM through a 64-bit AXI bus.
PCIe1 PCIe2	2x PCI Express 2.0	The PCIe IP provides PCI Express Gen 2.0 functionality.
PMU	Power Management Unit	Integrated power management unit. Used to provide power to various SoC domains.
PWM1 PWM2 PWM3 PWM4	Pulse Width Modulation	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
QSPI	Quad SPI	The Quad SPI module acts as an interface to external serial flash devices. This module contains the following features: • Flexible sequence engine to support various flash vendor devices • Single pad/Dual pad/Quad pad mode of operation • Single Data Rate/Double Data Rate mode of operation • Parallel Flash mode • DMA support • Memory mapped read access to connected flash devices • Multi master access with priority and flexible and configurable buffer for each master
SAI1 SAI2 SAI3 SAI4 SAI5 SAI6	Synchronous Audio Interface	The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

Table 3. i.MX 8M Dual / 8M QuadLite / 8M Quad modules list (continued)

Block mnemonic	Block name	Brief description
uSDHC1 uSDHC2	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	The i.MX 8M Dual / 8M QuadLite / 8M Quad SoC characteristics: All the MMC/SD/SDIO controller IPs are based on the uSDHC IP. They are designed to support: • SD/SDIO standard, up to version 3.0. • MMC standard, up to version 5.0. • 1.8 V and 3.3 V operation, but do not support 1.2 V operation. • 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit/8-bit MMC mode. One uSDHC controller (SD1) can support up to an 8-bit interface, the other controller (SD2) can only support up to a 4-bit interface.
USB 3.0/2.0	2x USB 3.0/2.0 controllers and PHYs	Two USB controllers and PHYs that support USB 3.0 and USB 2.0. Each USB instance contains: • USB 3.0 core, which can operate in both 3.0 and 2.0 mode
VPU	Video Processing Unit	A high performing video processing unit (VPU), which covers many SD-level and HD-level video decoders. See the *i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processor Reference Manual* (IMX8MDQLQRM) for a complete list of the VPU's decoding and encoding capabilities.
WDOG1 WDOG2 WDOG3	Watchdog	The watchdog (WDOG) timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.
XTALOSC	Crystal Oscillator interface	The XTALOSC module enables connectivity to an external crystal oscillator device.

2.1 Recommended connections for unused interfaces

The recommended connections for unused analog interfaces can be found in the Section, "Unused Input/Output Terminations," in the hardware development guide for the device.

Table 9. Maximum supply currents[1] (continued)

Power rail	Max current	Unit
USB2_VPTX	21.2	mA
USB1_VDD33	24.5	mA
USB2_VDD33	24.5	mA
USB1_VPH	20.3	mA
USB2_VPH	20.3	mA
PCIE_VP (PCIE1)	38.1	mA
PCIE_VP (PCIE2)	38.1	mA
PCIE_VPH (PCIE1)	43	mA
PCIE_VPH (PCIE2)	43	mA
PCIE_VPTX (PCIE1)	14.3	mA
PCIE_VPTX (PCIE2)	14.3	mA
HDMI_AVDDCLK	95.89	mA
HDMI_AVDDCORE		
HDMI_AVDDIO	6.551	mA
MIPI_VDDA (DSI)	17.1	mA
MIPI_VDDHA (DSI)	4.2	mA
MIPI_VDD (DSI)	14.4	mA
MIPI_VDDPLL (DSI)	3.8	mA
MIPI_VDDA (CSI1/2)	18.79	mA
MIPI_VDDHA (CSI1/2)	2.97	mA
EFUSE_VQPS	96.35	mA

1 Use case dependent

3.1.6 Power modes

The i.MX 8M Dual / 8M QuadLite / 8M Quad processors support the following power modes:

- RUN Mode: All external power rails are on, CPU is active and running; other internal modules can be on/off based on application.
- IDLE Mode: When there is no thread running and all high-speed devices are not active, the CPU can automatically enter this mode. The CPU can be in the power-gated state but with L2 data retained, DRAM and the bus clock are reduced. Most of the internal logic is clock gated but still remains powered. The M4 core can remain running. Compared with RUN mode, all the external power rails from the PMIC remain the same, and most of the modules still remain in their state.
- Deep Sleep Mode (DSM): The most efficient power saving mode where all the clocks are off and all the unnecessary power supplies are off.

- SNVS Mode: This mode is also called RTC mode. Only the power for the SNVS domain remains on to keep RTC and SNVS logic alive.
- OFF Mode: All power rails are off.

Table 10. Chip power in different LP mode

Mode	Supply	Max.[1]	Unit
SNVS	VDD_SNVS (1.0 V)	1.39	mA
	NVCC_SNVS (3.6 V)	4.25	
	Total[2]	17	mW
Deep Sleep Mode (DSM)	VDD_SOC (1.0 V)	148.50	mA
	VDDA_1P8 (2.0 V)	12.82	
	VDDA_0P9 (1.0 V)	0.30	
	VDDA_DRAM (1.8 V)	0.50	
	VDD_SNVS (1.0 V)	0.25	
	NVCC_SNVS (3.3 V)	4.80	
	NVCC_DRAM (1.17 V)	4.51	
	Total[2]	197	mW
IDLE	VDD_ARM (1.0 V)	152.10	mA
	VDD_SOC (1.0 V)	132.90	
	VDD_DRAM (1.0 V)	44.10	
	VDDA_1P8 (2.0 V)	13.53	
	VDDA_0P9 (1.0 V)	0.30	
	VDDA_DRAM (1.8 V)	1.32	
	VDD_SNVS (1.0 V)	0.25	
	NVCC_SNVS (3.3 V)	4.34	
	NVCC_DRAM (1.17 V)	13.12	
	Total[2]	389	mW
RUN	Total	1 to 4	mW

1 All the power numbers defined in the table are based on typical silicon at 25°C. Use case dependent

2 Sum of the listed supply rails.

Table 11 summarizes the external power supply states in all the power modes.

Table 11. The power supply states

Power rail	OFF	SNVS	SUSPEND	IDLE	RUN
VDD_ARM	OFF	OFF	OFF	ON	ON
VDD_SOC	OFF	OFF	ON	ON	ON

3.1.7 USB PHY Suspend current consumption

3.1.7.1 Low power Suspend Mode

The VBUS Valid comparators and their associated bandgap circuits are enabled by default. Table 12 shows the USB interface current consumption in Suspend mode with default settings.

Table 12. USB PHY current consumption in Suspend mode[1]

	USB1_VDD33	USB2_VDD33
Current	154 µA	154 µA

1 Low Power Suspend is enabled by setting USBx_PORTSC1 [PHCD]=1 [Clock Disable (PLPSCD)].

3.1.7.2 Power-Down modes

Table 13 shows the USB interface current consumption with only the OTG block powered down.

Table 13. USB PHY current consumption in Sleep mode[1]

	USB1_VDD33	USB2_VD33
Current	520 µA	520 µA

1 VBUS Valid comparators can be disabled through software by setting USBNC_OTG*_PHY_CFG2[OTGDISABLE0] to 1. This signal powers down only the VBUS Valid comparator, and does not control power to the Session Valid Comparator, ADP Probe and Sense comparators, or ID detection circuitry.

In Power-Down mode, everything is powered down, including the USB_VBUS valid comparators and their associated bandgap circuity in typical condition. Table 14 shows the USB interface current consumption in Power-Down mode.

Table 14. USB PHY current consumption in Power-Down mode[1]

	USB1_VDD33	USB2_VDD33
Current	146 µA	146 µA

1 The VBUS Valid Comparators and their associated bandgap circuits can be disabled through software by setting USBNC_OTG*_PHY_CFG2[OTGDISABLE0] to 1 and USBNC_OTG*_PHY_CFG2[DRVVBUS0] to 0, respectively.

3.1.8 PCIe PHY 2.1 DC electrical characteristics

Table 15. PCIe recommended operating conditions

Parameter	Description		Min	Max	Unit
PCIE_VP	Low Power Supply Voltage for PHY Core	—	0.837	0.99	V
PCIE_VPTX	PHY transmit supply	—	0.837	0.99	
PCIE_VPH	High Power Supply Voltage for PHY Core	1.8	1.674	1.98	
		3.3	3.069	3.63	

- Turn on VDD_ARM, VDD_GPU, VDD_VPU, and VDD_DRAM (no sequence between these four rails)
- Turn on VDDA_1P8_XXX, VDDA_DRAM (no sequence between these rails)
- Turn on NVCC_XXX and NVCC_DRAM (no sequence between these rails)
- POR_B release (it should be asserted during the entire power up sequence)

If the GPU/VPU is not used during the ROM boot sequence, VDD_GPU/VDD_VPU can stay off to reduce the power during boot, and then turned on by software afterwards.

During the chip power up, the power of the PCIe PHY, USB PHY, HDMI PHY, and MIPI PHY could stay off. After chip power up, the power of these PHys should be turned on. If any of the PHY power are turned on during the power up sequence, the POR_B can be released after the PHY power is stable.

3.2.2 Power-down sequence

The i.MX 8M Dual / 8M QuadLite / 8M Quad processors have the following power-down sequence requirements:

- Turn off NVCC_SNVS and VDD_SNVS last
- Turn off VDD_SOC after the other power rails or at the same time as other rails
- No sequence for other power rails during power down

3.2.3 Power supplies usage

I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about the I/O power supply of each pin, see “Power Rail” columns in the pin list tables of Section 5, “Package information and contact assignments.”

Table 19 lists the modules in each power domain.

Table 19. The modules in the power domains

Power Domain	Modules in the domain
VDD_ARM	Arm A53
VDD_GPU	GC7000L GPU
VDD_VPU	G1 and G2 VPU
VDD_DRAM	DRAM controller and PHY
VDD_SNVS	SNVS_LP
VDD_SOC	All the other modules

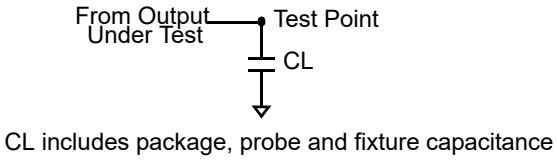

Figure 3. Load circuit for output

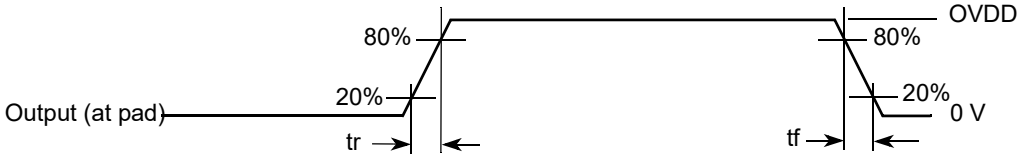

Figure 4. Output transition time waveform

3.6.1 General purpose I/O AC parameters

This section presents the I/O AC parameters for GPIO in different modes. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 31. Maximum input cell delay time

Cell name	Max Delay PAD → Y (ns)		
	V_{DD} = 1.62 V T = 125°C WCS model	—	V_{DD} = 3.0V T = 125°C WCS model
PBIJGTOV36PUD_MCLAMP_LVGPIO_EW	1.54	—	1.3

Table 32. Output cell delay time for fixed load

Parameter			Simulated Cell Delay A → PAD (ns)	
			VDD = 1.62 V, T = 125°C	VDD = 2.97 V, T = 125°C
dse[2:0]	fsel[1:0]	Driver Type	CL = 15 pF	CL = 15 pF
011	00	3 x Slow Slew	3.1	3.3
011	11	3 x Fast Slew	2.1	2.6
100	00	4 x Slow Slew	3.7	3.9
100	11	4 x Fast Slew	2.3	2.8
101	00	5 x Slow Slew	3.1	3.5
101	11	5 x Fast Slew	2.1	2.5

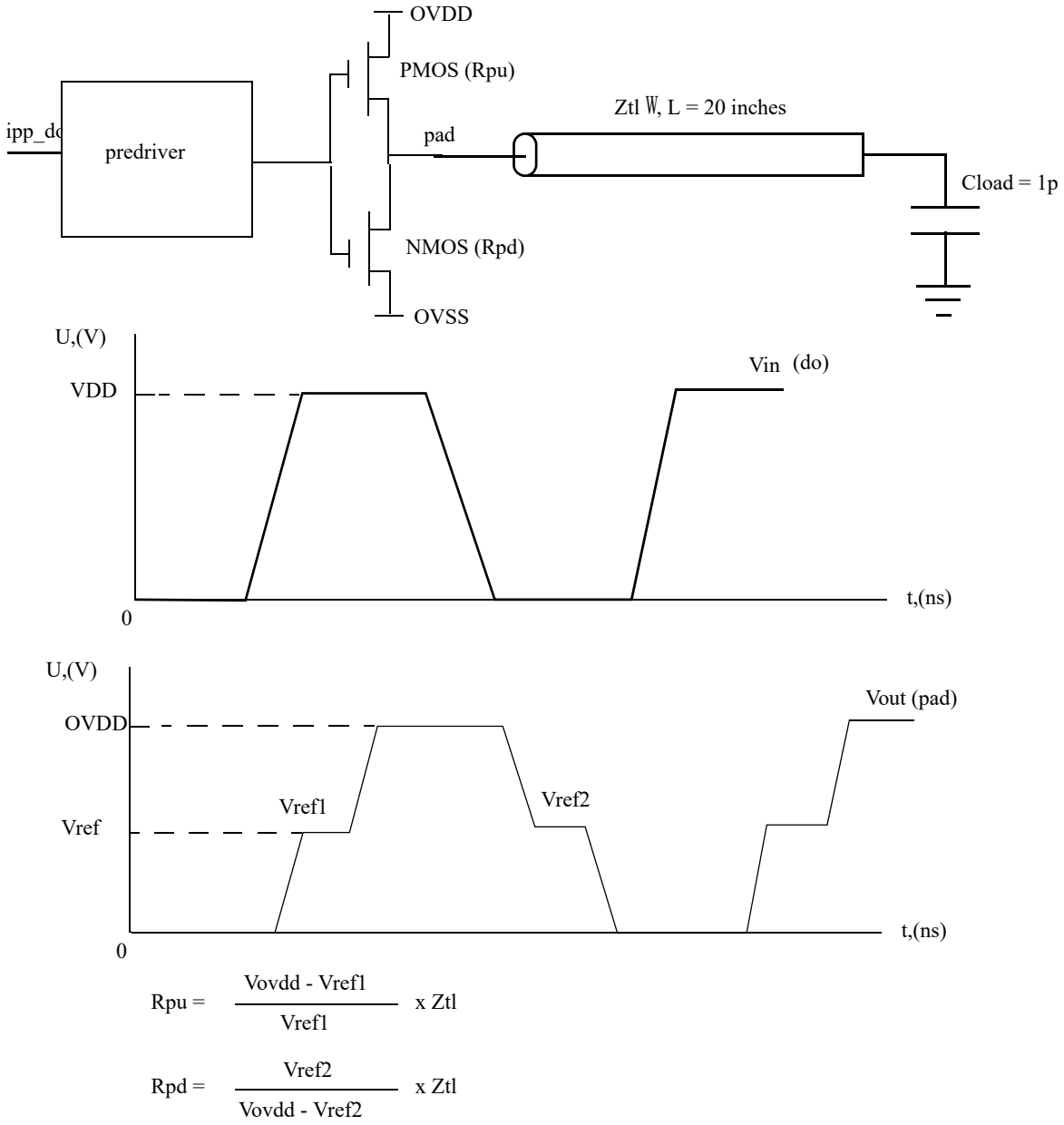

Figure 6. Impedance matching load for measurement

3.9.1.2 ECSPI Slave mode timing

Figure 10 depicts the timing of ECSPI in Slave mode. Table 39 lists the ECSPI Slave mode timing characteristics.

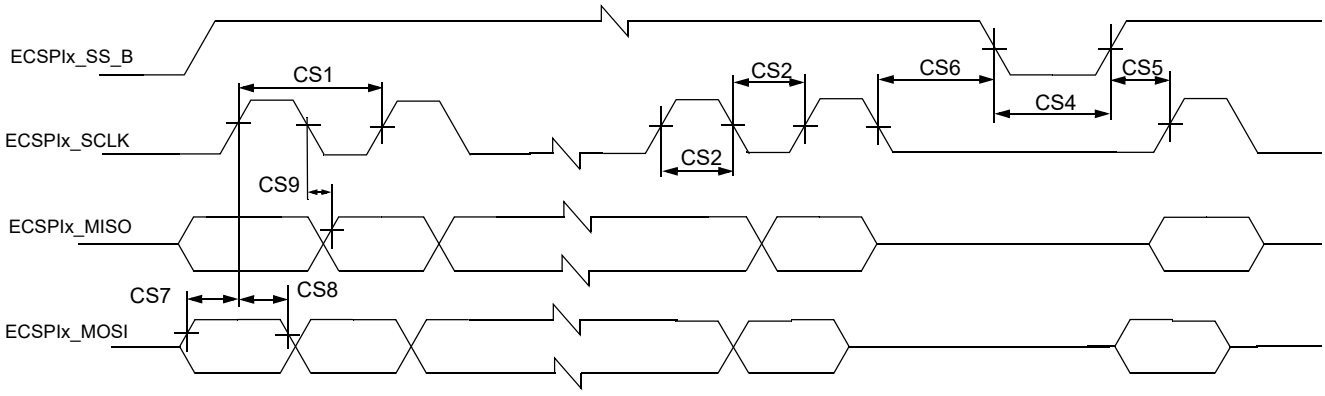

Figure 10. ECSPI Slave mode timing diagram

Table 39. ECSPI Slave mode timing parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPI_SCLK Cycle Time–Write	t_{clk}	15 43	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	7 21.5	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	19	ns

3.9.2 Ultra-high-speed SD/SDIO/MMC host interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (single data rate) timing, eMMC4.4/4.41 (dual data rate) timing and SDR104/50 (SD3.0) timing.

3.9.2.1 SD/eMMC4.3 (single data rate) AC timing

Figure 11 depicts the timing of SD/eMMC4.3, and Table 40 lists the SD/eMMC4.3 timing characteristics.

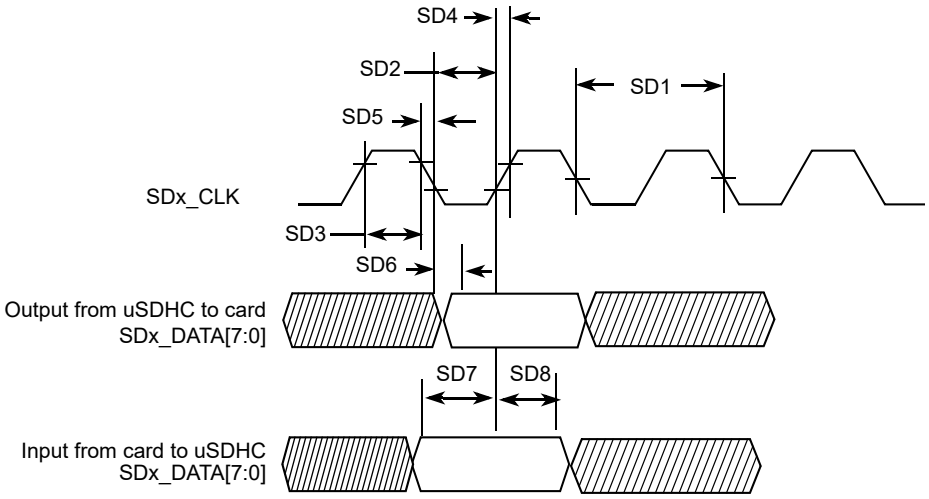

Figure 11. SD/eMMC4.3 timing

Table 40. SD/eMMC4.3 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	6.6	3.6	ns

3.9.3.2 RGMII signal switching specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 46. RGMII signal switching specifications[1]

Symbol	Description	Min.	Max.	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-500	500	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	85	%
Duty_T[4]	Duty cycle for 10/100T	40	90	%
Tr/Tf	Rise/fall time (20–80%)	—	0.98	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; this implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

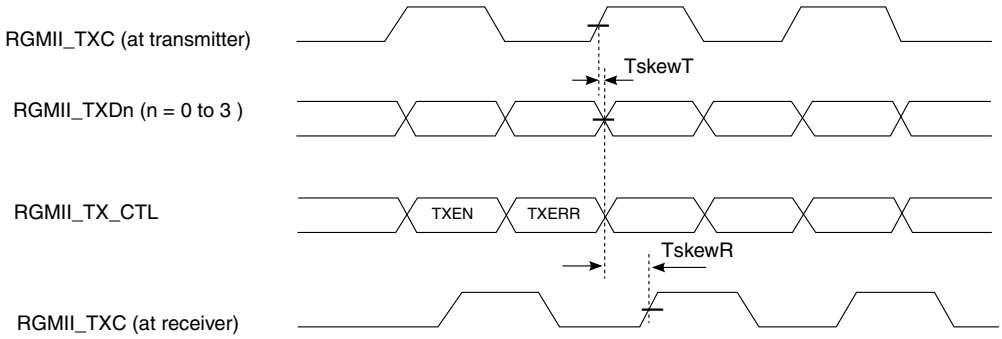

Figure 17. RGMII transmit signal timing diagram original

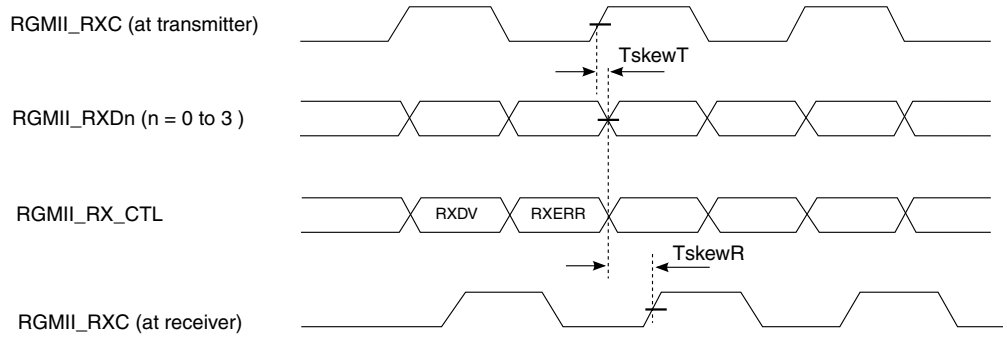

Figure 18. RGMII receive signal timing diagram original

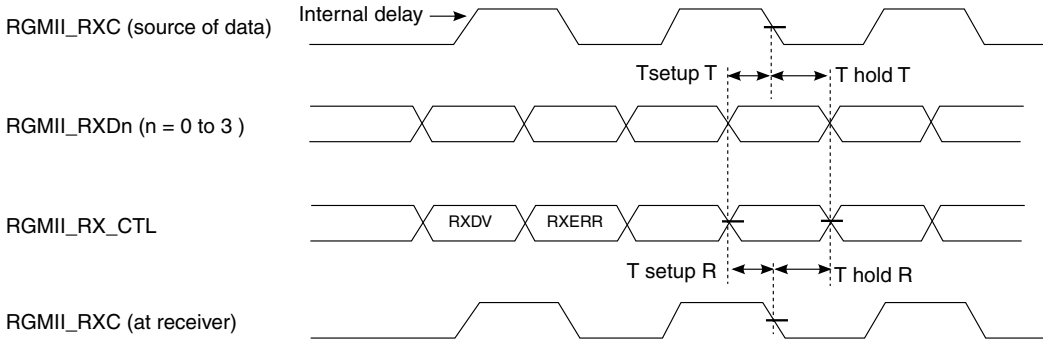

Figure 19. RGMII receive signal timing diagram with internal delay

3.9.4 General-purpose media interface (GPMI) timing

The GMPI controller of the i.MX 8M Dual / 8M QuadLite / 8M Quad processor is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous Timing mode, Source Synchronous Timing mode and Toggle Timing mode separately, as described in the following subsections.

3.9.4.1 Asynchronous mode AC timing (ONFI 1.0 compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 20 through Figure 23 depicts the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 47 describes the timing parameters (NF1–NF17) that are shown in the figures.

5 When the output voltage is between 15% and 85% of the fully settled LP signal levels.
6 Measured as average across any 50 mV segment of the output signal transition.
7 This value represents a corner point in a piecewise linear curve.

3.9.7.3 MIPI LP-RX specifications

Table 55. MIPI low power receiver DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Logic 1 input voltage	880	—	1.3	mV
V_{IL}	Logic 0 input voltage, not in ULP state	—	—	550	mV
$V_{IL-ULPS}$	Logic 0 input voltage, ULP state	—	—	300	mV
V_{HYST}	Input hysteresis	25	—	—	mV

Table 56. MIPI low power receiver AC specifications

Symbol	Parameter	Min	Typ	Max	Unit
e_{SPIKE}[1,2]	Input pulse rejection	—	—	300	V.ps
T_{MIN-RX}[3]	Minimum pulse width response	20	0	0	ns
V_{INT}	Peak Interference amplitude	—	—	200	mV
f_{INT}	Interference frequency	450	—	—	MHz

1 Time-voltage integration of a spike above V_{IL} when in LP-0 state or below V_{IH} when in LP-1 state.
2 An impulse below this value will not change the receiver state.
3 An input pulse greater than this value shall toggle the output.

3.9.7.4 MIPI LP-CD specifications

Table 57. MIPI contention detector DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{IHCD}	Logic 1 contention threshold	450	—	—	mV
V_{ILCD}	Logic 0 contention threshold	—	—	200	mV

3.9.7.5 MIPI DC specifications

Table 58. MIPI input characteristics DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{PIN}	Pad signal voltage range	-50	—	1350	mV
I_{LEAK}[1]	Pin leakage current	-30	—	30	µA
V_{GNDSH}	Ground shift	-50	—	50	mV

Table 58. MIPI input characteristics DC specifications (continued)

$V_{PIN(absmax)}$[2]	Maximum pin voltage level	-0.15	—	1.45	V
$T_{VPIN(absmax)}$[3]	Maximum transient time above $V_{PIN(max)}$ or below $V_{PIN(min)}$	—	—	20	ns

1 When the pad voltage is within the signal voltage range between $V_{GNDSH(min)}$ to $V_{OH} + V_{GNDSH(max)}$ and the Lane Module is in LP receive mode.

2 This value includes ground shift.

3 The voltage overshoot and undershoot beyond the V_{PIN} is only allowed during a single 20 ns window after any LP-0 to LP-1 transition or vice versa. For all other situations it must stay within the V_{PIN} range.

3.9.8 PCIe PHY parameters

The PCIe interface is designed to be compatible with PCIe specification Gen2 x1 lane and supports the PCI Express 1.1/2.0 standard.

3.9.8.1 PCIEx_RESREF reference resistor connection

The impedance calibration process requires connection of reference resistor 200 Ω. 1% precision resistor on PCIEx_RESREF pads to ground. It is used for termination impedance calibration.

3.9.9 Pulse width modulator (PWM) timing parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 31 depicts the timing of the PWM, and Table 59 lists the PWM timing parameters.

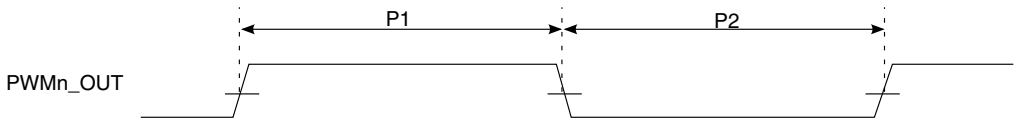

Figure 31. PWM timing

Table 59. PWM output timing parameters

ID	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	ipg_clk (66 MHz)	MHz
P1	PWM output pulse width high	15	—	ns
P2	PWM output pulse width low	15	—	ns

3.9.10 Quad SPI (QSPI) timing parameters

This section describes the electrical information for QSPI.

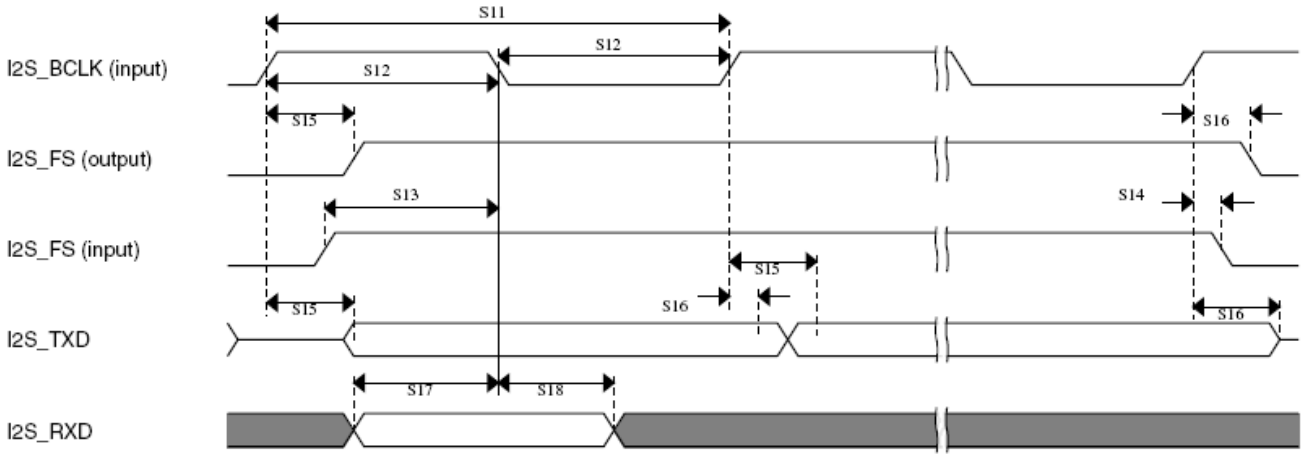

Figure 39. SAI Timing — Slave Modes

3.9.12 SPDIF timing parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 68 and Figure 40 and Figure 41 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 68. SPDIF timing parameters

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50 pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT output (Load = 30 pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

Table 76. USB power pin supplies (continued)

Pin Name	Description	Value
USB1/2_VPTX	PHY transmit supply	0.9 V (+22.2%, -7%)
USB1/2_VDD33	High supply for high-speed operation IO	3.3 V (+10%, -7%)
USB1/2_VPH	High supply for SuperSpeed operation IO	3.3 V (+10%, -7%)

Table 77 shows the external component values.

Table 77. External component values

Component	Pin Name	Value
External resistor (resref)	USB1_RESREF/USB2_RESREF	200 Ω (±1%)

Table 78 shows the minimum ESD protection target levels.

Table 78. Minimum ESD protection target levels

ESD Category	Minimum Protection Level	JEDEC Class
Human Body Model (HBM) (JS-001-2014)	2 KV	2
Charged Device Model (CDM) (JESD22-C101F)	6 A peak discharge current	C2/C1 (500 V/ 250 V)[1]
Machine Model (MM) (JESD22_A115C)	100 V	N/A

1 Support for either 500 V or 250 V CDM target level is dependent on maximum discharge current generated in final SoC/package implementation.

Table 79 shows the supply impedance requirements.

Table 79. Supply impedance requirements

$L_{gd} + L_{vp}$(nH)	L_{VSSA}<#> + L_{DVDD}(nH)	$L_{gd} + L_{vptx}$<#>(nH)	L_{VSSA}<#> + L_{VDD33} <#>(nH)	$L_{gd} + L_{vph}$(nH)
< 2.4	< 2.4	< 2.4	< 2.8	< 2.8

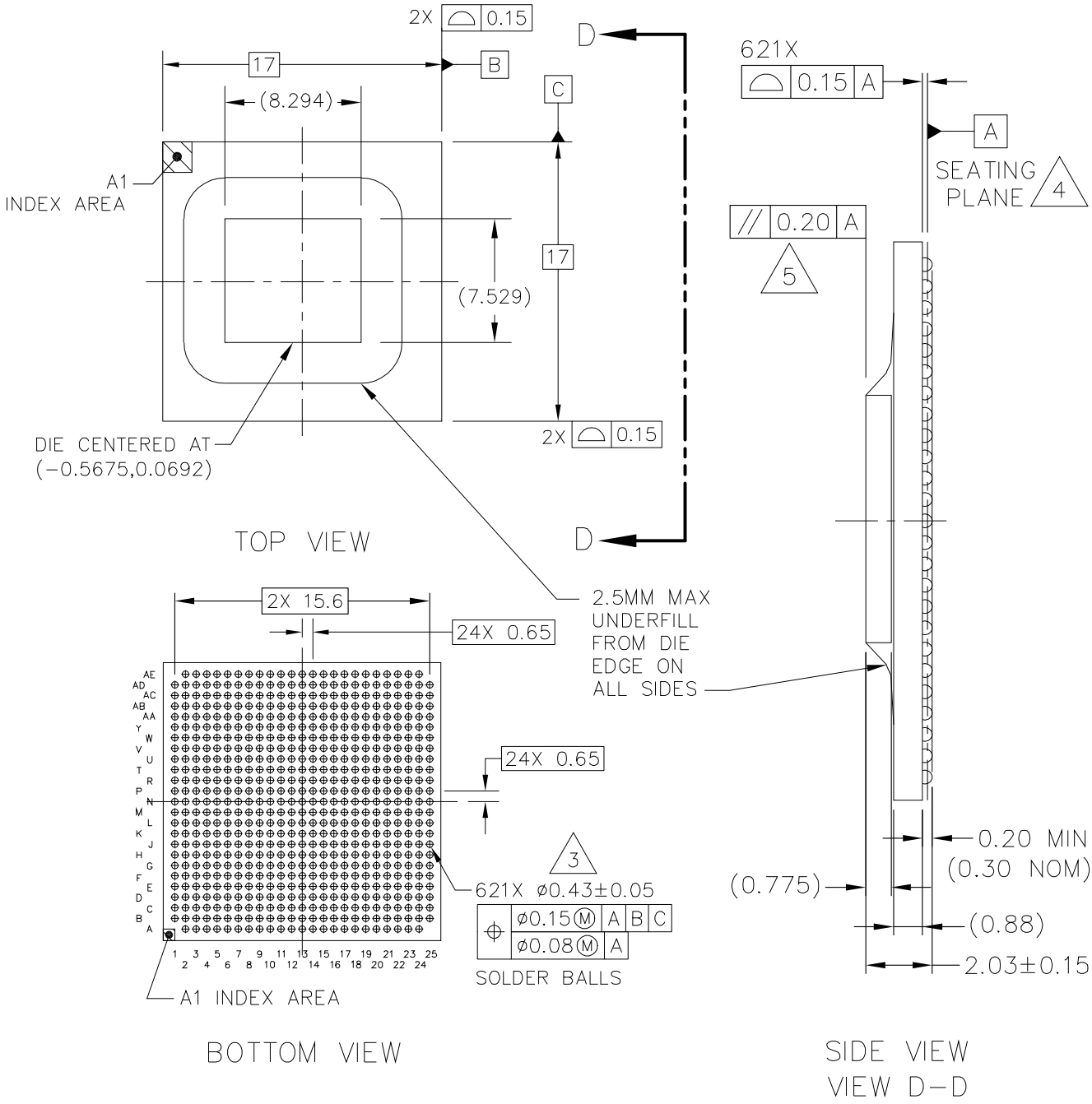

Figure 44. 17 x 17 mm BGA, package top, bottom, and side Views

Table 83. i.MX 8M Dual / 8M QuadLite / 8M Quad 17 x 17 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type[1]	Reset condition[2]			
				Default mode (Reset mode)	Default function (Signal name)	Input/ Output	Value
ECSPI2_SCLK	C5	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[10]	Input	PD (90 K)
ECSPI2_SS0	A5	NVCC_ECSPI	GPIO	ALT5	GPIO5.IO[13]	Input	PD (90 K)
ENET_MDC	N20	NVCC_ENET	GPIO	ALT5	GPIO1.IO[16]	Input	PD (90 K)
ENET_MDIO	N19	NVCC_ENET	GPIO	ALT5	GPIO1.IO[17]	Input	PD (90 K)
ENET_RD0	U19	NVCC_ENET	GPIO	ALT5	GPIO1.IO[26]	Input	PD (90 K)
ENET_RD1	U21	NVCC_ENET	GPIO	ALT5	GPIO1.IO[27]	Input	PD (90 K)
ENET_RD2	U20	NVCC_ENET	GPIO	ALT5	GPIO1.IO[28]	Input	PD (90 K)
ENET_RD3	V19	NVCC_ENET	GPIO	ALT5	GPIO1.IO[29]	Input	PD (90 K)
ENET_RXC	T20	NVCC_ENET	GPIO	ALT5	GPIO1.IO[25]	Input	PD (90 K)
ENET_RX_CTL	T21	NVCC_ENET	GPIO	ALT5	GPIO1.IO[24]	Input	PD (90 K)
ENET_TD0	R20	NVCC_ENET	GPIO	ALT5	GPIO1.IO[21]	Input	PD (90 K)
ENET_TD1	R21	NVCC_ENET	GPIO	ALT5	GPIO1.IO[20]	Input	PD (90 K)
ENET_TD2	R19	NVCC_ENET	GPIO	ALT5	GPIO1.IO[19]	Input	PD (90 K)
ENET_TD3	P20	NVCC_ENET	GPIO	ALT5	GPIO1.IO[18]	Input	PD (90 K)
ENET_TXC	T19	NVCC_ENET	GPIO	ALT5	GPIO1.IO[23]	Input	PD (90 K)
ENET_TX_CTL	P19	NVCC_ENET	GPIO	ALT5	GPIO1.IO[22]	Input	PD (90 K)
GPIO1_IO00	T6	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[0]	Input	PD (90 K)
GPIO1_IO01[3]	T7	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[1]	Input	PD (90 K)
GPIO1_IO02	R4	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[2]	Input	PD (27 K)
GPIO1_IO03	P4	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[3]	Input	PD (90 K)
GPIO1_IO04	P5	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[4]	Input	PD (90 K)
GPIO1_IO05[4]	P7	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[5]	Input	PU (27 K)
GPIO1_IO06	N5	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[6]	Input	PD (90 K)
GPIO1_IO07	N6	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[7]	Input	PD (90 K)
GPIO1_IO08	N7	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[8]	Input	PD (90 K)
GPIO1_IO09	M6	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[9]	Input	PD (90 K)
GPIO1_IO10	M7	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[10]	Input	PD (90 K)
GPIO1_IO11	L6	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[11]	Input	PD (90 K)
GPIO1_IO12	L7	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[12]	Input	PD (90 K)
GPIO1_IO13	K6	NVCC_GPIO1	GPIO	ALT0	GPIO1.IO[13]	Input	PD (90 K)

Table 83. i.MX 8M Dual / 8M QuadLite / 8M Quad 17 x 17 mm functional contact assignments (continued)

Ball name	Ball	Power group	Ball type[1]	Reset condition[2]			
				Default mode (Reset mode)	Default function (Signal name)	Input/ Output	Value
SD1_CLK	L25	NVCC_SD1	GPIO	ALT5	GPIO2.IO[0]	Input	PD (90 K)
SD1_CMD	L24	NVCC_SD1	GPIO	ALT5	GPIO2.IO[1]	Input	PD (90 K)
SD1_DATA0	M25	NVCC_SD1	GPIO	ALT5	GPIO2.IO[2]	Input	PD (90 K)
SD1_DATA1	M24	NVCC_SD1	GPIO	ALT5	GPIO2.IO[3]	Input	PD (90 K)
SD1_DATA2	N25	NVCC_SD1	GPIO	ALT5	GPIO2.IO[4]	Input	PD (90 K)
SD1_DATA3	P25	NVCC_SD1	GPIO	ALT5	GPIO2.IO[5]	Input	PD (90 K)
SD1_DATA4	N24	NVCC_SD1	GPIO	ALT5	GPIO2.IO[6]	Input	PD (90 K)
SD1_DATA5	P24	NVCC_SD1	GPIO	ALT5	GPIO2.IO[7]	Input	PD (90 K)
SD1_DATA6	R25	NVCC_SD1	GPIO	ALT5	GPIO2.IO[8]	Input	PD (90 K)
SD1_DATA7	T25	NVCC_SD1	GPIO	ALT5	GPIO2.IO[9]	Input	PD (90 K)
SD1_RESET_B	R24	NVCC_SD1	GPIO	ALT5	GPIO2.IO[10]	Input	PD (90 K)
SD1_STROBE	T24	NVCC_SD1	GPIO	ALT5	GPIO2.IO[11]	Input	PD (90 K)
SD2_CD_B	L21	NVCC_SD2	GPIO	ALT5	GPIO2.IO[12]	Input	PD (90 K)
SD2_CLK	L22	NVCC_SD2	GPIO	ALT5	GPIO2.IO[13]	Input	PD (90 K)
SD2_CMD	M22	NVCC_SD2	GPIO	ALT5	GPIO2.IO[14]	Input	PD (90 K)
SD2_DATA0	N22	NVCC_SD2	GPIO	ALT5	GPIO2.IO[15]	Input	PD (90 K)
SD2_DATA1	N21	NVCC_SD2	GPIO	ALT5	GPIO2.IO[16]	Input	PD (90 K)
SD2_DATA2	P22	NVCC_SD2	GPIO	ALT5	GPIO2.IO[17]	Input	PD (90 K)
SD2_DATA3	P21	NVCC_SD2	GPIO	ALT5	GPIO2.IO[18]	Input	PD (90 K)
SD2_RESET_B	R22	NVCC_SD2	GPIO	ALT5	GPIO2.IO[19]	Input	PD (90 K)
SD2_WP	M21	NVCC_SD2	GPIO	ALT5	GPIO2.IO[20]	Input	PD (90 K)
SPDIF_EXT_CLK	E6	NVCC_SAI3	GPIO	ALT5	GPIO5.IO[5]	Input	PD (90 K)
SPDIF_RX	G6	NVCC_SAI3	GPIO	ALT5	GPIO5.IO[4]	Input	PD (90 K)
SPDIF_TX	F6	NVCC_SAI3	GPIO	ALT5	GPIO5.IO[3]	Input	PD (90 K)
TEST_MODE	V7	NVCC_JTAG	GPIO	ALT0	tcu.TEST_MODE	Input	PD (90 K)
UART1_RXD	C7	NVCC_UART	GPIO	ALT5	GPIO5.IO[22]	Input	PD (90 K)
UART1_TXD	A7	NVCC_UART	GPIO	ALT5	GPIO5.IO[23]	Input	PD (90 K)
UART2_RXD	B6	NVCC_UART	GPIO	ALT5	GPIO5.IO[24]	Input	PD (90 K)
UART2_TXD	D6	NVCC_UART	GPIO	ALT5	GPIO5.IO[25]	Input	PD (90 K)
UART3_RXD	A6	NVCC_UART	GPIO	ALT5	GPIO5.IO[26]	Input	PD (90 K)

6 Revision history

Table 86 provides a revision history for this data sheet.

Table 86. Revision history

Rev. number	Date	Substantive change(s)
Rev. 0.1	05/2018	• Added a note in the Table 2, "Orderable part numbers" • Updated the Table 3, "i.MX 8M Dual / 8M QuadLite / 8M Quad modules list" • Updated teh Table 7, "Operating ranges" • Updated the Table 9, "Maximum supply currents" • Updated the Table 10, "Chip power in different LP mode" • Added the Table 11, "The power supply states" • Updated the PCIe parameters in the Table 15, "PCIe recommended operating conditions" • Updated and added a leakage limit note in the Table 26, "GPIO DC parameters" • Added a leakage limit note in the Table 29, "Input DC current" • Updated the timing parameters in the Table 38, "ECSPI Master mode timing parameters" and Table 39, "ECSPI Slave mode timing parameters" • Updated the Section 3.9.8.1, “PCIEx_RESREF reference resistor connection • Updated the Table 58, "MIPI input characteristics DC specifications" • Removed the SPI interfaces from the Table 81, "Interface allocation during boot" • Updated the PCIe and MIPI power group in the Table 83, "i.MX 8M Dual / 8M QuadLite / 8M Quad 17 x 17 mm functional contact assignments" • Updated the Table 84, "17 x 17 mm, 0.65 mm pitch ball map"
Rev. 0	01/2018	• Initial version