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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I <sup>2</sup> C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/efm8bb10f2g-a-qfn20r">https://www.e-xfl.com/product-detail/silicon-labs/efm8bb10f2g-a-qfn20r</a>

## 2. Ordering Information

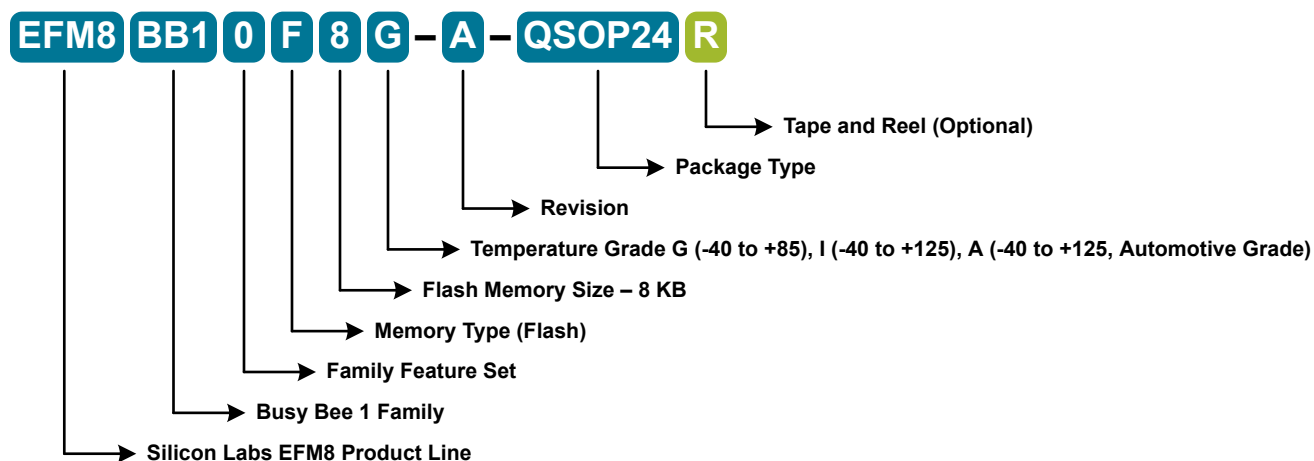


Figure 2.1. EFM8BB1 Part Numbering

All EFM8BB1 family members have the following features:

- CIP-51 Core running up to 25 MHz
- Two Internal Oscillators (24.5 MHz and 80 kHz)
- SMBus / I2C
- SPI
- UART
- 3-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- 4 16-bit Timers
- 2 Analog Comparators
- 12-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, and temperature sensor
- 16-bit CRC Unit
- AEC-Q100 qualified
- Pre-loaded UART bootloader

In addition to these features, each part number in the EFM8BB1 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB10F8G-A-QSOP24	8	512	18	16	8	8	Yes	-40 to +85 C	QSOP24
EFM8BB10F8G-A-QFN20	8	512	16	15	8	7	Yes	-40 to +85 C	QFN20
EFM8BB10F8G-A-SOIC16	8	512	13	12	6	6	Yes	-40 to +85 C	SOIC16
EFM8BB10F4G-A-QFN20	4	512	16	15	8	7	Yes	-40 to +85 C	QFN20
EFM8BB10F2G-A-QFN20	2	256	16	15	8	7	Yes	-40 to +85 C	QFN20
EFM8BB10F8I-A-QSOP24	8	512	18	16	8	8	Yes	-40 to +125 C	QSOP24

### 3. System Overview

#### 3.1 Introduction

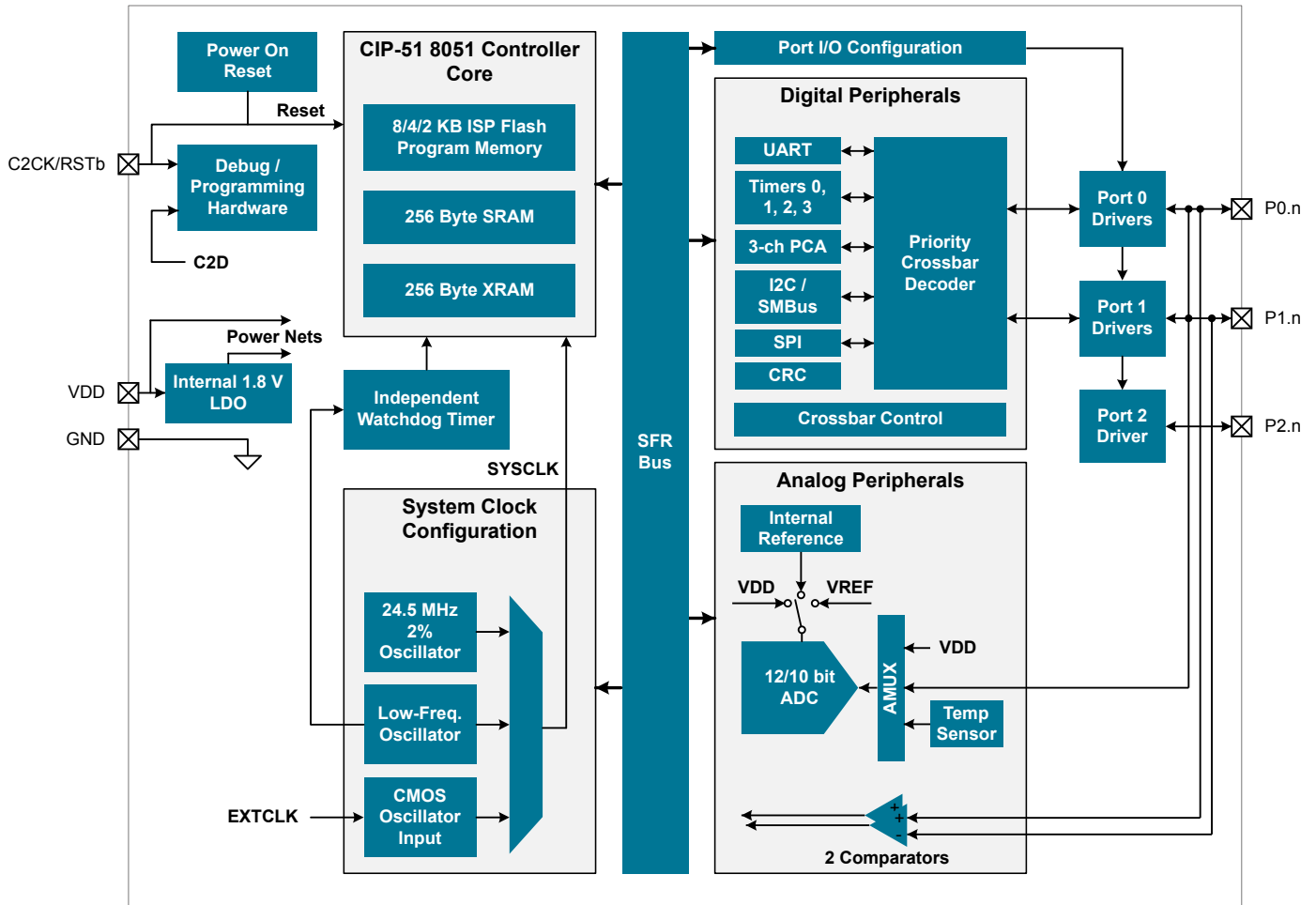


Figure 3.1. Detailed EFM8BB1 Block Diagram

This section describes the EFM8BB1 family at a high level. For more information on each module including register definitions, see the EFM8BB1 Reference Manual.

### 3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

**Table 3.1. Power Modes**

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational	—	—
Idle	<ul style="list-style-type: none"> <li>Core halted</li> <li>All peripherals clocked and fully operational</li> <li>Code resumes execution on wake event</li> </ul>	Set IDLE bit in PCON0	Any interrupt
Stop	<ul style="list-style-type: none"> <li>All internal power nets shut down</li> <li>Pins retain state</li> <li>Exit on any reset source</li> </ul>	<ol style="list-style-type: none"> <li>Clear STOPCF bit in REG0CN</li> <li>Set STOP bit in PCON0</li> </ol>	Any reset source
Shutdown	<ul style="list-style-type: none"> <li>All internal power nets shut down</li> <li>Pins retain state</li> <li>Exit on pin or power-on reset</li> </ul>	<ol style="list-style-type: none"> <li>Set STOPCF bit in REG0CN</li> <li>Set STOP bit in PCON0</li> </ol>	<ul style="list-style-type: none"> <li>RSTb pin reset</li> <li>Power-on reset</li> </ul>

### 3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P1.7 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.0 and P2.1 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P2.0.

- Up to 18 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 16 direct-pin interrupt sources with shared interrupt vector (Port Match).

### 3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

- Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to  $\pm 2\%$  over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External CMOS clock input (EXTCLK).
- Clock divider with eight settings for flexible clock scaling: Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.

### 3.10 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in the code security page, which is the last last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website ([www.silabs.com/8bit-appnotes](http://www.silabs.com/8bit-appnotes)) or within Simplicity Studio by using the [Application Notes] tile.

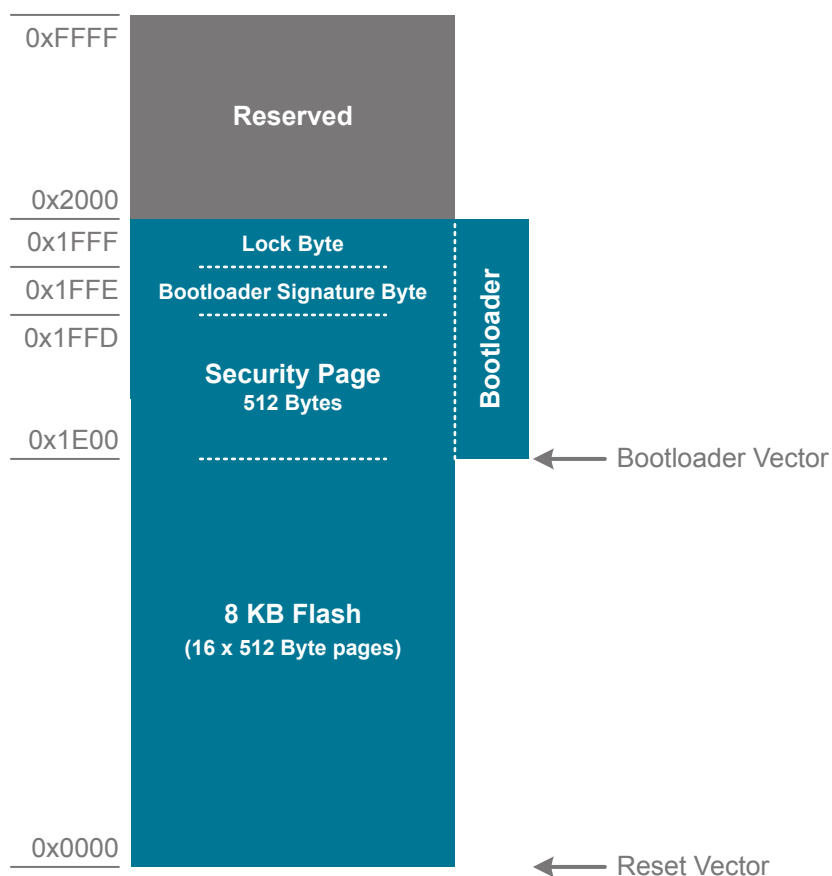


Figure 3.2. Flash Memory Map with Bootloader—8 KB Devices

Table 3.2. Summary of Pins for Bootloader Communication

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC0 Always-on <sup>4</sup>	I <sub>ADC</sub>	800 ksps, 10-bit conversions or 200 ksps, 12-bit conversions Normal bias settings V <sub>DD</sub> = 3.0 V	—	845	1200	μA
		250 ksps, 10-bit conversions or 62.5 ksps 12-bit conversions Low power bias settings V <sub>DD</sub> = 3.0 V	—	425	580	μA
ADC0 Burst Mode, 10-bit single conversions, external reference	I <sub>ADC</sub>	200 ksps, V <sub>DD</sub> = 3.0 V	—	370	—	μA
		100 ksps, V <sub>DD</sub> = 3.0 V	—	185	—	μA
		10 ksps, V <sub>DD</sub> = 3.0 V	—	19	—	μA
ADC0 Burst Mode, 10-bit single conversions, internal reference, Low power bias settings	I <sub>ADC</sub>	200 ksps, V <sub>DD</sub> = 3.0 V	—	490	—	μA
		100 ksps, V <sub>DD</sub> = 3.0 V	—	245	—	μA
		10 ksps, V <sub>DD</sub> = 3.0 V	—	23	—	μA
ADC0 Burst Mode, 12-bit single conversions, external reference	I <sub>ADC</sub>	100 ksps, V <sub>DD</sub> = 3.0 V	—	530	—	μA
		50 ksps, V <sub>DD</sub> = 3.0 V	—	265	—	μA
		10 ksps, V <sub>DD</sub> = 3.0 V	—	53	—	μA
ADC0 Burst Mode, 12-bit single conversions, internal reference	I <sub>ADC</sub>	100 ksps, V <sub>DD</sub> = 3.0 V, Normal bias	—	950	—	μA
		50 ksps, V <sub>DD</sub> = 3.0 V, Low power bias	—	420	—	μA
		10 ksps, V <sub>DD</sub> = 3.0 V, Low power bias	—	85	—	μA
Internal ADC0 Reference, Always-on <sup>5</sup>	I <sub>VREFFS</sub>	Normal Power Mode	—	680	790	μA
		Low Power Mode	—	160	210	μA
Temperature Sensor	I <sub>TSENSE</sub>		—	75	120	μA
Comparator 0 (CMP0), Comparator 1 (CMP1)	I <sub>CMP</sub>	CPMD = 11	—	0.5	—	μA
		CPMD = 10	—	3	—	μA
		CPMD = 01	—	10	—	μA
		CPMD = 00	—	25	—	μA
Voltage Supply Monitor (VMON0)	I <sub>VMON</sub>		—	15	20	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Slope Error	$E_M$	12 Bit Mode	—	±0.02	±0.1	%
		10 Bit Mode	—	±0.06	±0.24	%
<b>Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, Max throughput, using AGND pin</b>						
Signal-to-Noise	SNR	12 Bit Mode	61	66	—	dB
		10 Bit Mode	53	60	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	61	66	—	dB
		10 Bit Mode	53	60	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	71	—	dB
		10 Bit Mode	—	70	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	-79	—	dB
		10 Bit Mode	—	-74	—	dB
<b>Note:</b>						
1. Absolute input pin voltage is limited by the $V_{DD}$ supply.						

#### 4.1.8 Voltage Reference

**Table 4.8. Voltage Reference**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Internal Fast Settling Reference</b>						
Output Voltage (Full Temperature and Supply Range)	$V_{REFFS}$	1.65 V Setting	1.62	1.65	1.68	V
		2.4 V Setting, $V_{DD} \geq 2.6$ V	2.35	2.4	2.45	V
Temperature Coefficient	$TC_{REFFS}$		—	50	—	ppm/°C
Turn-on Time	$t_{REFFS}$		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REF FS}$		—	400	—	ppm/V
<b>External Reference</b>						
Input Current	$I_{EXTREF}$	Sample Rate = 800 ksps; $V_{REF} = 3.0$ V	—	5	—	µA

#### 4.1.9 Temperature Sensor

**Table 4.9. Temperature Sensor**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	$V_{OFF}$	$T_A = 0\text{ }^{\circ}\text{C}$	—	757	—	mV
Offset Error <sup>1</sup>	$E_{OFF}$	$T_A = 0\text{ }^{\circ}\text{C}$	—	17	—	mV
Slope	M		—	2.85	—	mV/ $^{\circ}\text{C}$
Slope Error <sup>1</sup>	$E_M$		—	70	—	$\mu\text{V}/^{\circ}\text{C}$
Linearity			—	0.5	—	$^{\circ}\text{C}$
Turn-on Time			—	1.8	—	$\mu\text{s}$

**Note:**

1. Represents one standard deviation from the mean.

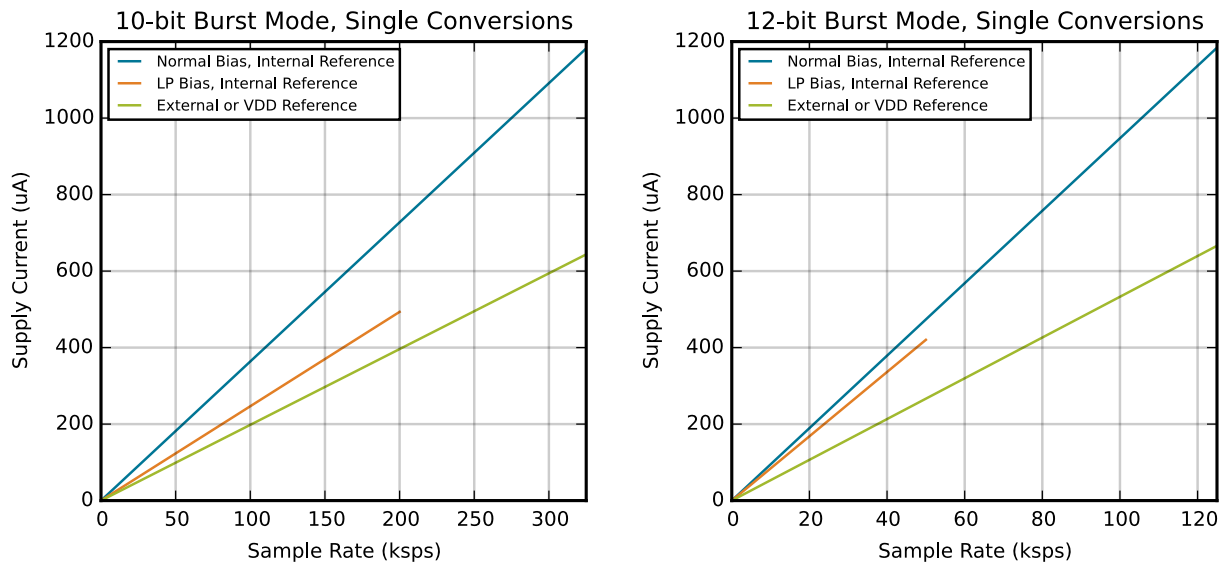
#### 4.1.10 1.8 V Internal LDO Voltage Regulator

**Table 4.10. 1.8V Internal LDO Voltage Regulator**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage	$V_{OUT\_1.8V}$		1.74	1.8	1.85	V



Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative Hysteresis Mode 3 (CPMD = 11)	HYS <sub>CP-</sub>	CPHYN = 00	—	-1.5	—	mV
		CPHYN = 01	—	-4	—	mV
		CPHYN = 10	—	-8	—	mV
		CPHYN = 11	—	-16	—	mV
Input Range (CP+ or CP-)	V <sub>IN</sub>		-0.25	—	V <sub>DD</sub> +0.25	V
Input Pin Capacitance	C <sub>CP</sub>		—	7.5	—	pF
Common-Mode Rejection Ratio	CMRR <sub>CP</sub>		—	70	—	dB
Power Supply Rejection Ratio	PSRR <sub>CP</sub>		—	72	—	dB
Input Offset Voltage	V <sub>OFF</sub>	T <sub>A</sub> = 25 °C	-10	0	10	mV
Input Offset Tempco	TC <sub>OFF</sub>		—	3.5	—	μV/°C



**Figure 4.4. Typical ADC0 and Internal Reference Supply Current in Burst Mode**

## 5. Typical Connection Diagrams

### 5.1 Power

Figure 5.1 Power Connection Diagram on page 31 shows a typical connection diagram for the power pins of the EFM8BB1 devices.

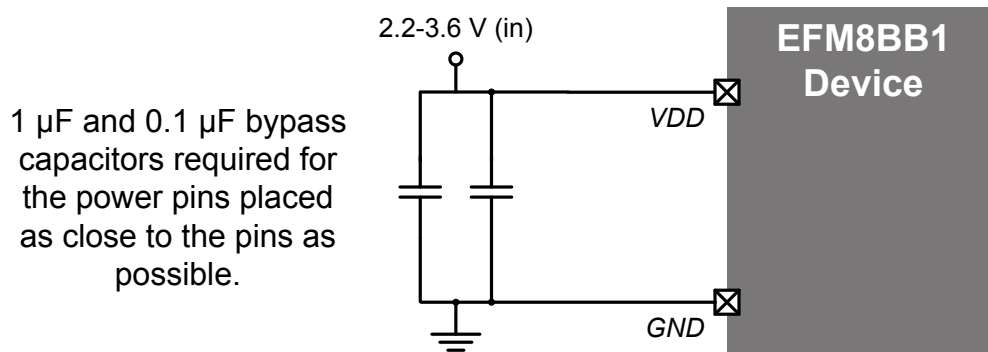


Figure 5.1. Power Connection Diagram

### 5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in application note, "AN127: Pin Sharing Techniques for the C2 Interface." Application notes can be found on the Silicon Labs website (<http://www.silabs.com/8bit-app-notes>) or in Simplicity Studio.

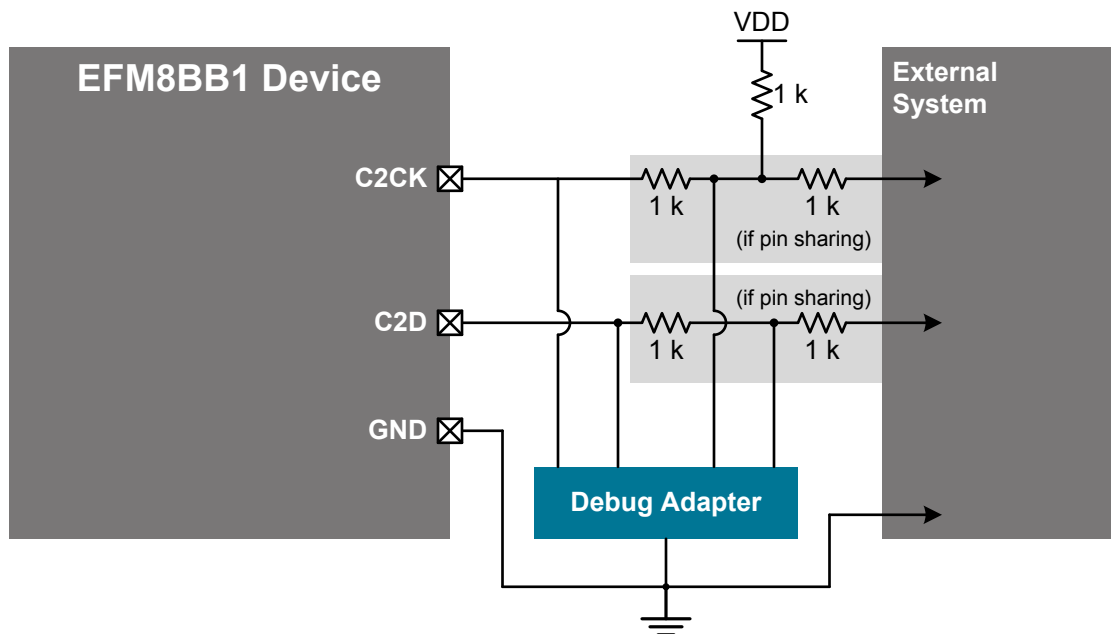


Figure 5.2. Debug Connection Diagram

### 5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application note, "AN203: 8-bit MCU Printed Circuit Board Design Notes", contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website ([www.silabs.com/8bit-appnotes](http://www.silabs.com/8bit-appnotes)).

## 6. Pin Definitions

### 6.1 EFM8BB1x-QSOP24 Pin Definitions

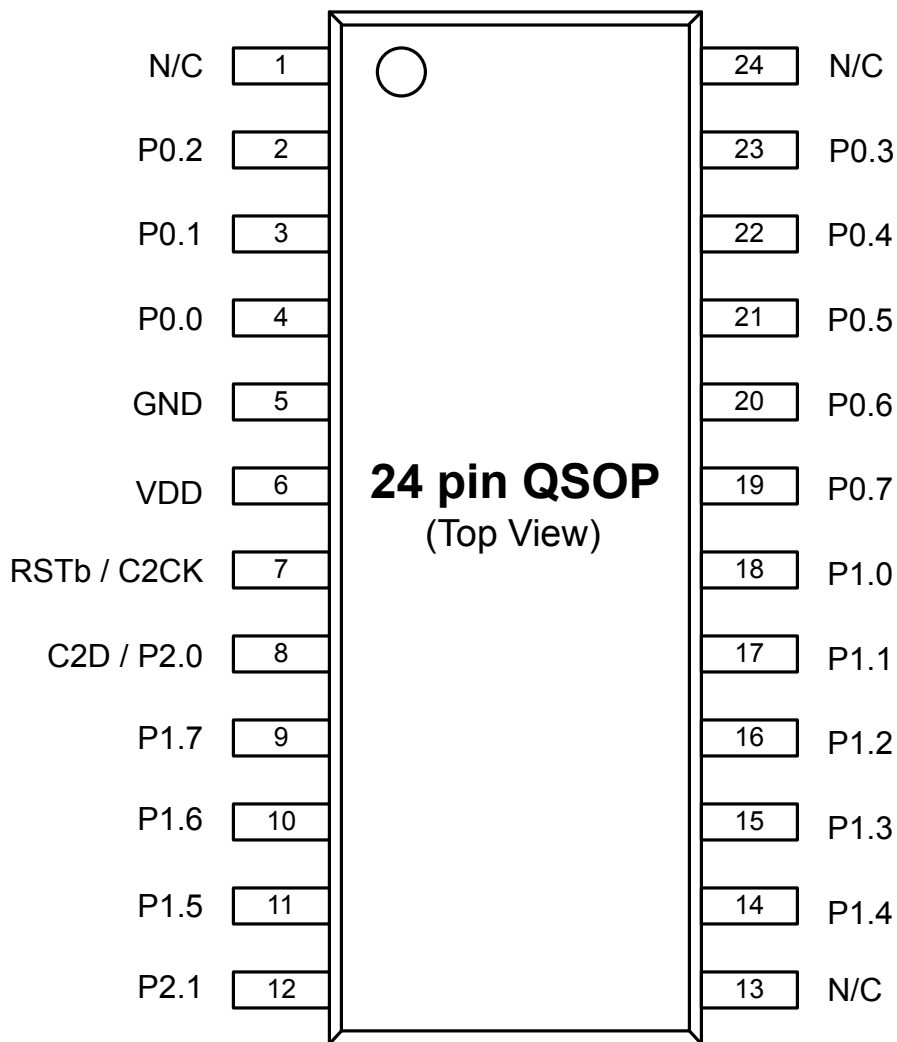


Figure 6.1. EFM8BB1x-QSOP24 Pinout

Table 6.1. Pin Definitions for EFM8BB1x-QSOP24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	N/C	No Connection			
2	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.2 CMP0N.2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
3	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1 AGND
4	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF
5	GND	Ground			
6	VDD	Supply Power Input			
7	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
8	P2.0 / C2D	Multifunction I/O / C2 Debug Data			
9	P1.7	Multifunction I/O	Yes	P1MAT.7	ADC0.15 CMP1P.7 CMP1N.7
10	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.14 CMP1P.6 CMP1N.6
11	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.13 CMP1P.5 CMP1N.5
12	P2.1	Multifunction I/O			
13	N/C	No Connection			
14	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP1P.4 CMP1N.4
15	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CMP1P.3 CMP1N.3
16	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CMP1P.2 CMP1N.2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
17	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CMP1P.1 CMP1N.1
18	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CMP1P.0 CMP1N.0
19	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CMP0P.7 CMP0N.7
20	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.6 CMP0N.6
21	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CMP0P.5 CMP0N.5
22	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CMP0P.4 CMP0N.4
23	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CMP0P.3 CMP0N.3
24	N/C	No Connection			

6.2 EFM8BB1x-QFN20 Pin Definitions

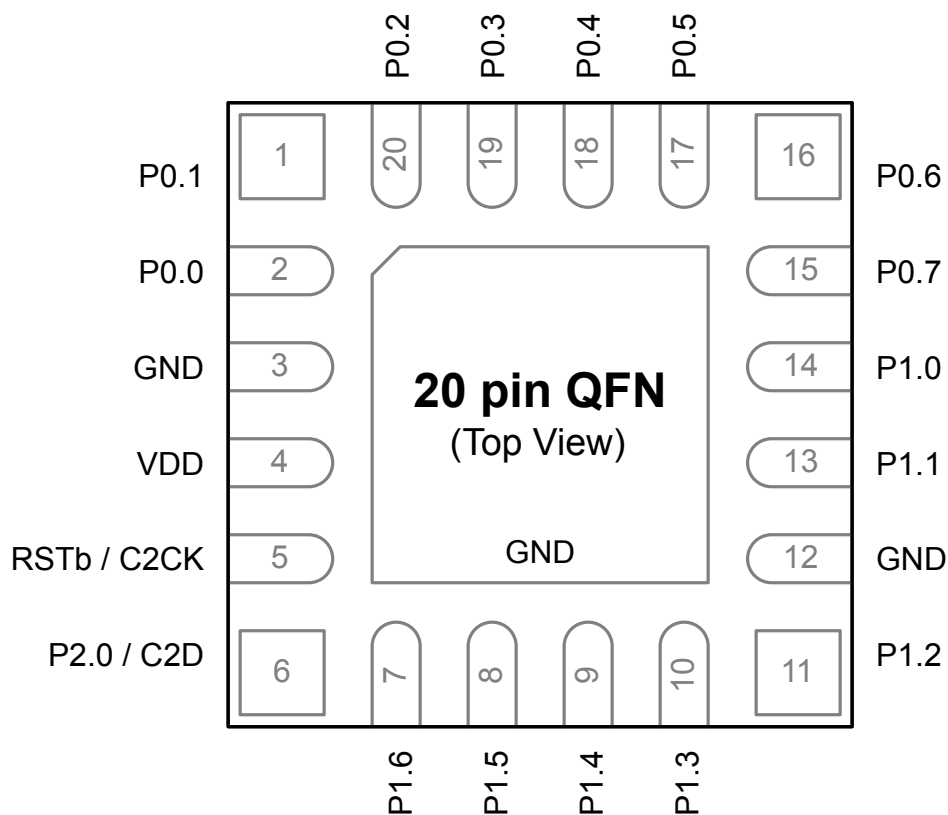


Figure 6.2. EFM8BB1x-QFN20 Pinout

Table 6.2. Pin Definitions for EFM8BB1x-QFN20

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1 AGND
2	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF



Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
3	GND	Ground			
4	VDD	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
6	P2.0 / C2D	Multifunction I/O / C2 Debug Data			
7	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.14 CMP1P.6 CMP1N.6
8	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.13 CMP1P.5 CMP1N.5
9	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP1P.4 CMP1N.4
10	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CMP1P.3 CMP1N.3
11	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CMP1P.2 CMP1N.2
12	GND	Ground			
13	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CMP1P.1 CMP1N.1
14	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CMP1P.0 CMP1N.0
15	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CMP0P.7 CMP0N.7
16	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.6 CMP0N.6

### 7.3 QSOP24 Package Marking



Figure 7.3. QSOP24 Package Marking

The package marking consists of:

- P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

## 8. QFN20 Package Specifications

### 8.1 QFN20 Package Dimensions

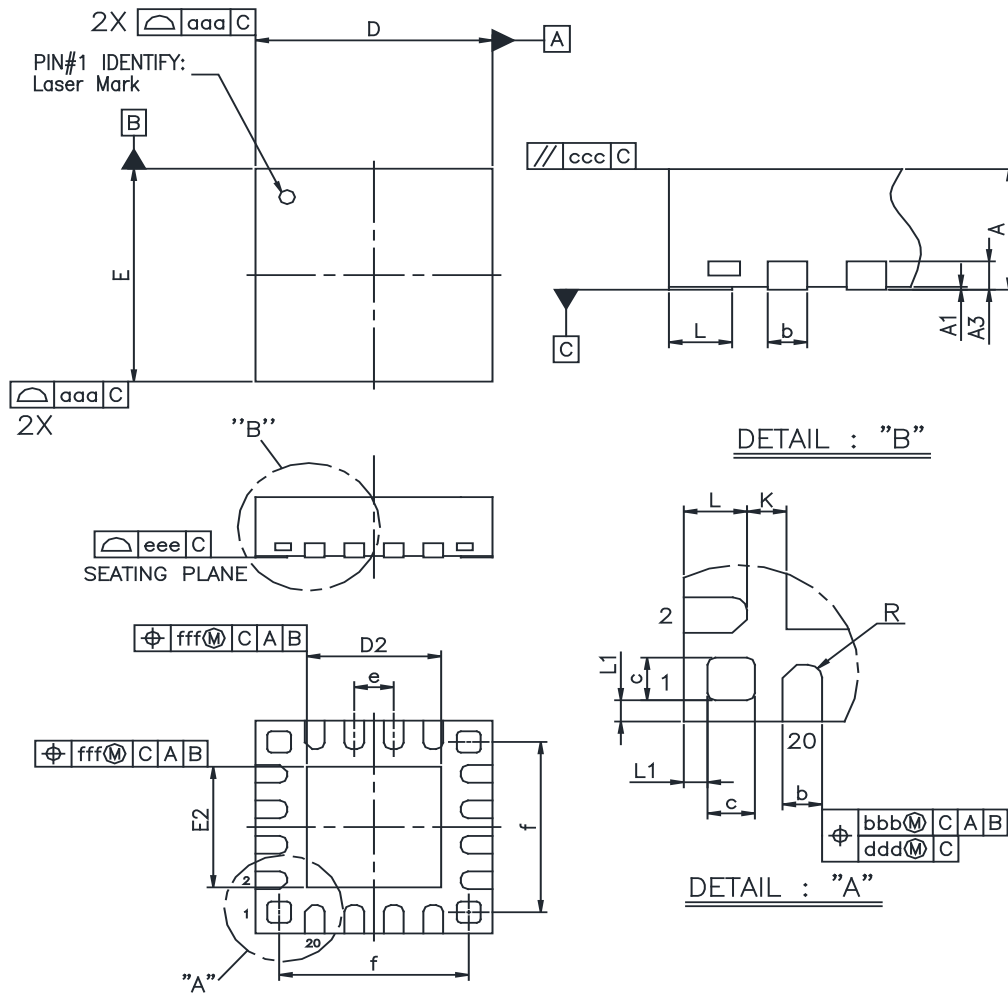


Figure 8.1. QFN20 Package Drawing

Table 8.1. QFN20 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.18	0.25	0.30
c	0.25	0.30	0.35
D	3.00 BSC		
D2	1.6	1.70	1.80
e	0.50 BSC		

## 10. Revision History

### 10.1 Revision 1.5

October 7th, 2016

Added A-grade parts.

Added specifications for [4.1.13 SMBus](#).

Added bootloader pinout information to [3.10 Bootloader](#).

Added CRC Calculation Time to [4.1.4 Flash Memory](#).

Added Thermal Resistance (Junction to Case) for QFN20 packages to [4.2 Thermal Conditions](#).

Added a note linking to the Typical VOH and VOL Performance graphs in [4.1.12 Port I/O](#).

Added [4.1.10 1.8 V Internal LDO Voltage Regulator](#).

Added a note to [3.1 Introduction](#) referencing the Reference Manual.

### 10.2 Revision 1.4

April 22nd, 2016

Added a reference to *AN945: EFM8 Factory Bootloader User Guide* in [3.10 Bootloader](#).

Added I-grade devices.

Added a note that all GPIO values are undefined when VDD is below 1 V to [4.1.1 Recommended Operating Conditions](#).

Adjusted the Total Current Sunk into Supply Pin and Total Current Sourced out of Ground Pin specifications in [4.3 Absolute Maximum Ratings](#).

### 10.3 Revision 1.3

January 7th, 2016

Added [5.2 Debug](#).

Updated [3.10 Bootloader](#) to include information about the bootloader implementation.

### 10.4 Revision 1.2

Updated Port I/O specifications in [4.1.12 Port I/O](#) to include new  $V_{OL}$  specifications.

Added a note to [Table 4.3 Reset and Supply Monitor on page 15](#) regarding guaranteed operation.

Updated package diagram and landing diagram specifications for the QFN20 package.

### 10.5 Revision 1.1

Initial release.

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