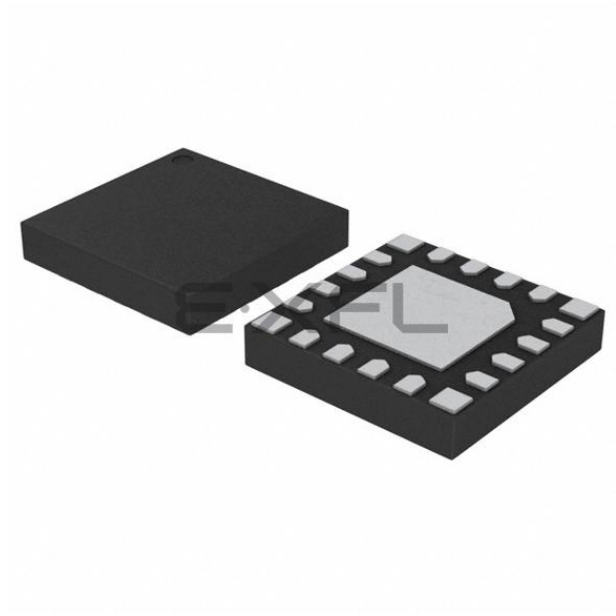
Silicon Labs - EFM8BB10F4A-A-QFN20R Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-WFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8bb10f4a-a-qfn20r

1. Feature List

The EFM8BB1 highlighted features are listed below.

- Core:
  - Pipelined CIP-51 Core
  - Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 25 MHz maximum operating frequency
- Memory:
  - Up to 8 kB flash memory, in-system re-programmable from firmware.
  - Up to 512 bytes RAM (including 256 bytes standard 8051 RAM and 256 bytes on-chip XRAM)
- Power:
  - Internal LDO regulator for CPU core voltage
  - Power-on reset circuit and brownout detectors
- I/O: Up to 18 total multifunction I/O pins:
  - All pins 5 V tolerant under bias
  - Flexible peripheral crossbar for peripheral routing
  - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
  - Internal 24.5 MHz oscillator with ±2% accuracy
  - Internal 80 kHz low-frequency oscillator
  - External CMOS clock option
- Timers/Counters and PWM:
  - 3-channel programmable counter array (PCA) supporting PWM, capture/compare, and frequency output modes
  - 4 x 16-bit general-purpose timers
  - Independent watchdog timer, clocked from the low frequency oscillator
- Communications and Digital Peripherals:
  - UART
  - SPI™ Master / Slave
  - SMBus™/I2C™ Master / Slave
  - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
- Analog:
  - 12-Bit Analog-to-Digital Converter (ADC)
  - 2 x Low-current analog comparators with adjustable reference
- On-Chip, Non-Intrusive Debugging
  - Full memory and register inspection
  - Four hardware breakpoints, single-stepping
- Pre-loaded UART bootloader
- Temperature range -40 to 85 ºC or -40 to 125 ºC
- Single power supply 2.2 to 3.6 V
- QSOP24, SOIC16, and QFN20 packages

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8BB1 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Each device is specified for 2.2 to 3.6 V operation, is AEC-Q100 qualified, and is available in 20-pin QFN, 16-pin SOIC or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB10F8I-A-QFN20	8	512	16	15	8	7	Yes	-40 to +125 C	QFN20
EFM8BB10F8I-A-SOIC16	8	512	13	12	6	6	Yes	-40 to +125 C	SOIC16
EFM8BB10F4I-A-QFN20	4	512	16	15	8	7	Yes	-40 to +125 C	QFN20
EFM8BB10F2I-A-QFN20	2	256	16	15	8	7	Yes	-40 to +125 C	QFN20
EFM8BB10F8A-A-QFN20	8	512	16	15	8	7	Yes	-40 to +125 C	QFN20
EFM8BB10F4A-A-QFN20	4	512	16	15	8	7	Yes	-40 to +125 C	QFN20
EFM8BB10F2A-A-QFN20	2	256	16	15	8	7	Yes	-40 to +125 C	QFN20

The A-grade (i.e. EFM8BB10F8A-A-QFN20) devices receive full automotive quality production status, including AEC-Q100 qualification, registration with International Material Data System (IMDS), and Part Production Approval Process (PPAP) documentation. PPAP documentation is available at www.silabs.com with a registered and NDA approved user account.

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational	—	—
Idle	• Core halted • All peripherals clocked and fully operational • Code resumes execution on wake event	Set IDLE bit in PCON0	Any interrupt
Stop	• All internal power nets shut down • Pins retain state • Exit on any reset source	1. Clear STOPCF bit in REG0CN 2. Set STOP bit in PCON0	Any reset source
Shutdown	• All internal power nets shut down • Pins retain state • Exit on pin or power-on reset	1. Set STOPCF bit in REG0CN 2. Set STOP bit in PCON0	• RSTb pin reset • Power-on reset

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P1.7 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.0 and P2.1 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P2.0.

- Up to 18 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 16 direct-pin interrupt sources with shared interrupt vector (Port Match).

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

- Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to ±2% over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External CMOS clock input (EXTCLK).
- Clock divider with eight settings for flexible clock scaling: Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.

3.10 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in the code security page, which is the last last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [**Application Notes**] tile.

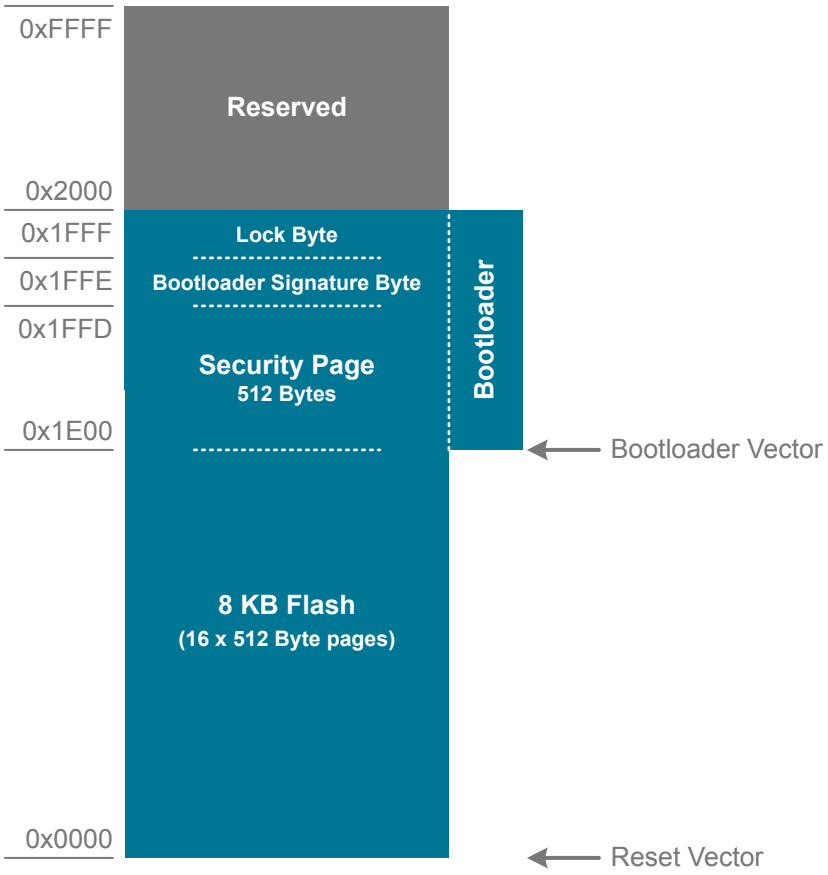

Figure 3.2. Flash Memory Map with Bootloader—8 KB Devices

Table 3.2. Summary of Pins for Bootloader Communication

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5

Table 3.3. Summary of Pins for Bootload Mode Entry

Device Package	Pin for Bootload Mode Entry
QSOP24	P2.0 / C2D
QFN20	P2.0 / C2D
SOIC16	P2.0 / C2D

4.1.6 External Clock Input

Table 4.6. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	f_{CMOS}		0	—	25	MHz
External Input CMOS Clock High Time	t_{CMOSH}		18	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		18	—	—	ns

4.1.9 Temperature Sensor

Table 4.9. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	T_A = 0 °C	—	757	—	mV
Offset Error[1]	E_{OFF}	T_A = 0 °C	—	17	—	mV
Slope	M		—	2.85	—	mV/°C
Slope Error[1]	E_M		—	70	—	µV/°C
Linearity			—	0.5	—	°C
Turn-on Time			—	1.8	—	µs

Note:
1. Represents one standard deviation from the mean.

4.1.10 1.8 V Internal LDO Voltage Regulator

Table 4.10. 1.8V Internal LDO Voltage Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage	$V_{OUT\_1.8V}$		1.74	1.8	1.85	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CPHYN = 00	—	-1.5	—	mV
		CPHYN = 01	—	–4	—	mV
		CPHYN = 10	—	–8	—	mV
		CPHYN = 11	—	–16	—	mV
Input Range (CP+ or CP–)	V_{IN}		-0.25	—	V_{DD}+0.25	V
Input Pin Capacitance	C_{CP}		—	7.5	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	70	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}	T_A = 25 °C	-10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C

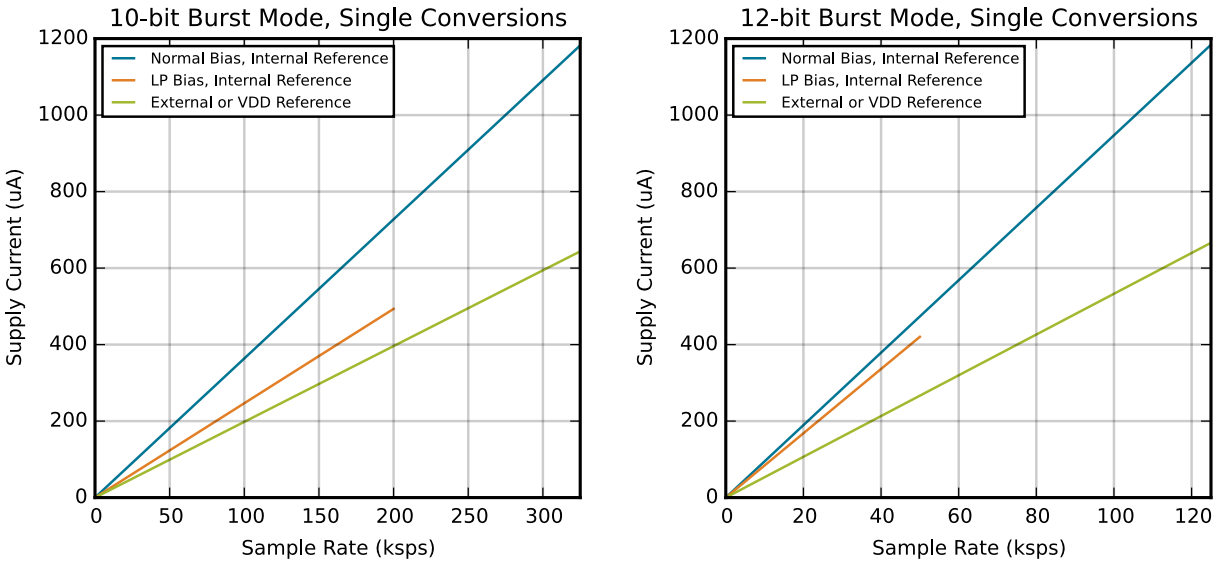

Figure 4.4. Typical ADC0 and Internal Reference Supply Current in Burst Mode

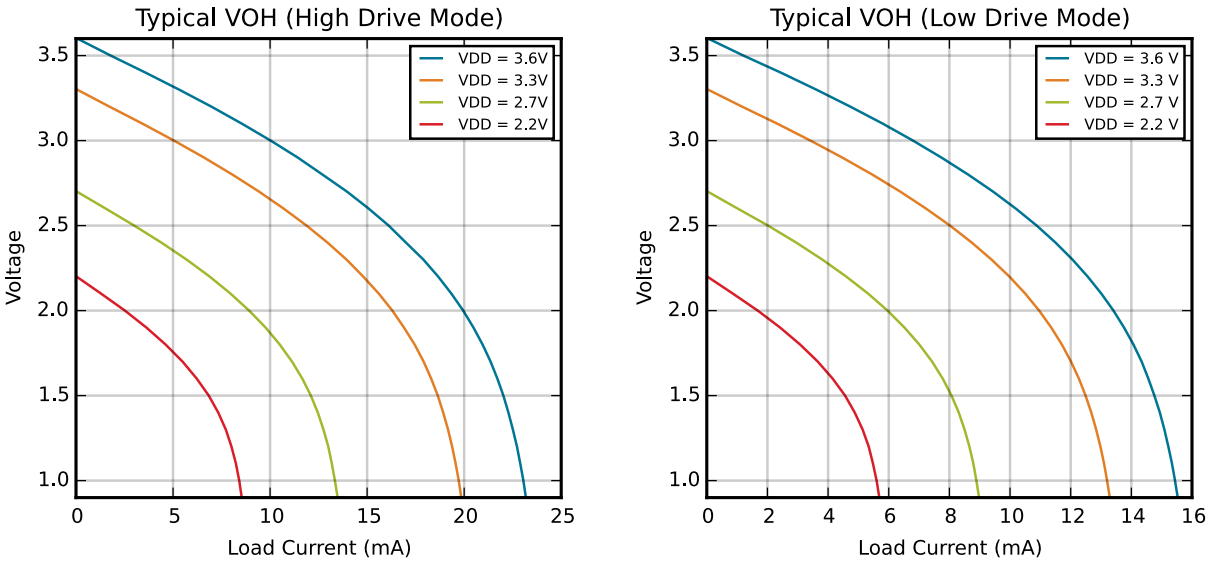

Figure 4.6. Typical V_{OH} Curves

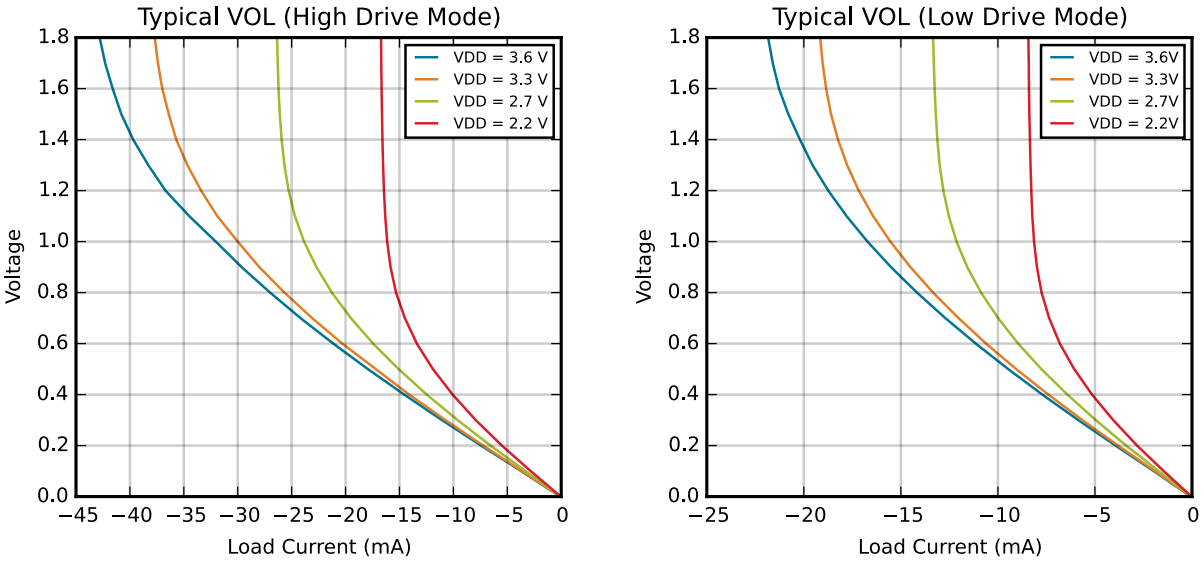

Figure 4.7. Typical V_{OL} Curves

6.2 EFM8BB1x-QFN20 Pin Definitions

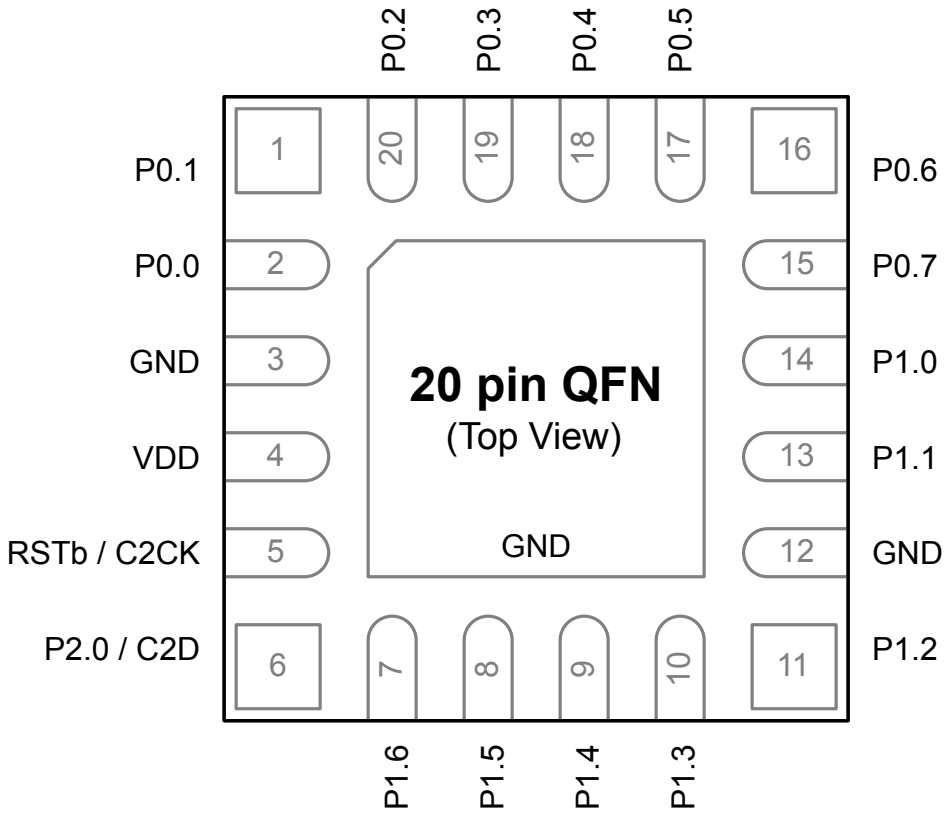

Figure 6.2. EFM8BB1x-QFN20 Pinout

Table 6.2. Pin Definitions for EFM8BB1x-QFN20

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1 AGND
2	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
3	GND	Ground			
4	VDD	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
6	P2.0 / C2D	Multifunction I/O / C2 Debug Data			
7	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.14 CMP1P.6 CMP1N.6
8	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.13 CMP1P.5 CMP1N.5
9	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP1P.4 CMP1N.4
10	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CMP1P.3 CMP1N.3
11	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CMP1P.2 CMP1N.2
12	GND	Ground			
13	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CMP1P.1 CMP1N.1
14	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CMP1P.0 CMP1N.0
15	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CMP0P.7 CMP0N.7
16	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.6 CMP0N.6

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
17	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CMP0P.5 CMP0N.5
18	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CMP0P.4 CMP0N.4
19	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CMP0P.3 CMP0N.3
20	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.2 CMP0N.2
Center	GND	Ground			

6.3 EFM8BB1x-SOIC16 Pin Definitions

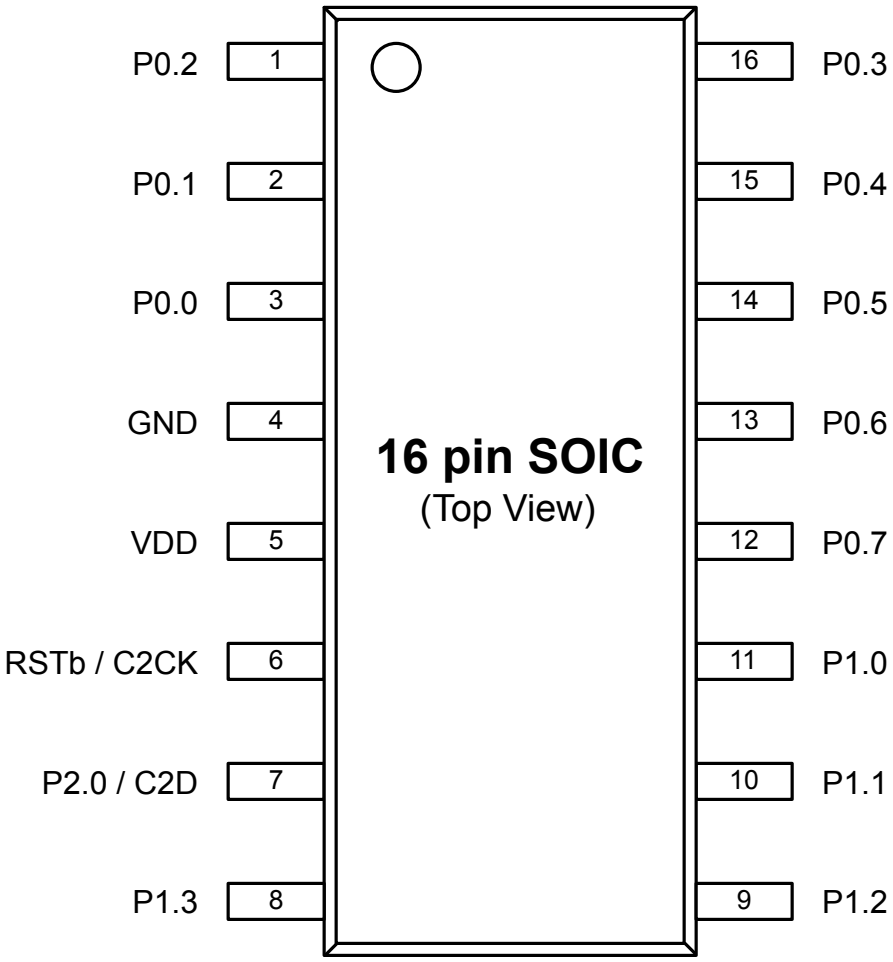

Figure 6.3. EFM8BB1x-SOIC16 Pinout

Table 6.3. Pin Definitions for EFM8BB1x-SOIC16

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.2 CMP0N.2
2	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1
3	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0

Dimension	Min	Typ	Max
E		3.00 BSC	
E2	1.60	1.70	1.80
f		2.50 BSC	
L	0.30	0.40	0.50
K		0.25 REF	
R	0.09	0.125	0.15
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. The drawing complies with JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 QFN20 PCB Land Pattern

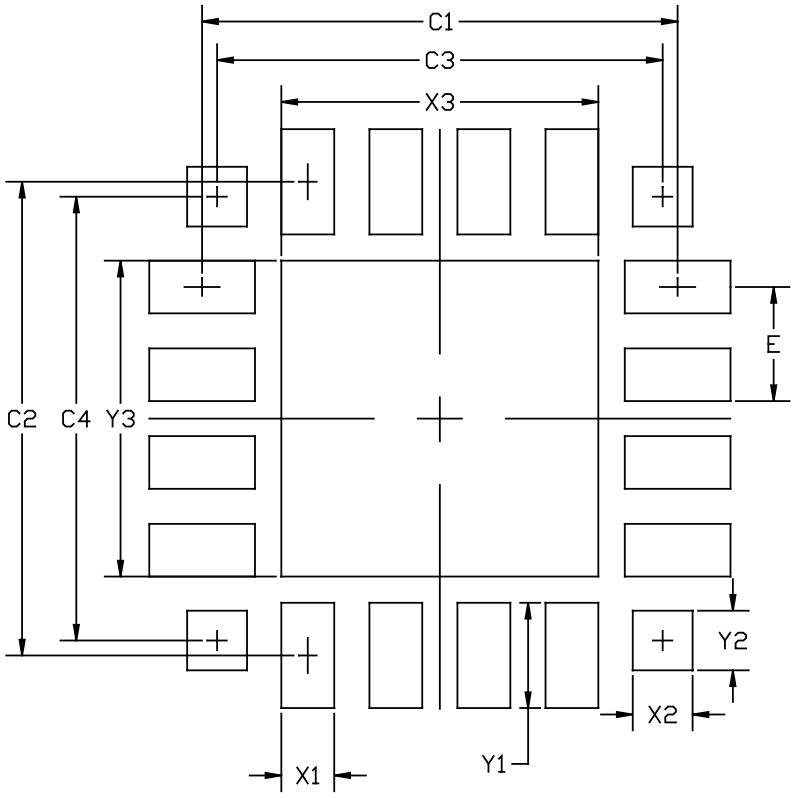

Figure 8.2. QFN20 PCB Land Pattern Drawing

Table 8.2. QFN20 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	3.10	
C2	3.10	
C3	2.50	
C4	2.50	
E	0.50	
X1	0.30	
X2	0.25	0.35
X3	1.80	
Y1	0.90	
Y2	0.25	0.35
Y3	1.80	

Dimension	Min	Typ	Max
h	0.25	—	0.50
θ	0º	—	8º
aaa		0.10	
bbb		0.20	
ccc		0.10	
ddd		0.25	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. Revision History

10.1 Revision 1.5

October 7th, 2016

Added A-grade parts.

Added specifications for 4.1.13 SMBus.

Added bootloader pinout information to 3.10 Bootloader.

Added CRC Calculation Time to 4.1.4 Flash Memory.

Added Thermal Resistance (Junction to Case) for QFN20 packages to 4.2 Thermal Conditions.

Added a note linking to the Typical VOH and VOL Performance graphs in 4.1.12 Port I/O.

Added 4.1.10 1.8 V Internal LDO Voltage Regulator.

Added a note to 3.1 Introduction referencing the Reference Manual.

10.2 Revision 1.4

April 22nd, 2016

Added a reference to *AN945: EFM8 Factory Bootloader User Guide* in 3.10 Bootloader.

Added I-grade devices.

Added a note that all GPIO values are undefined when VDD is below 1 V to 4.1.1 Recommended Operating Conditions.

Adjusted the Total Current Sunk into Supply Pin and Total Current Sourced out of Ground Pin specifications in 4.3 Absolute Maximum Ratings.

10.3 Revision 1.3

January 7th, 2016

Added 5.2 Debug.

Updated 3.10 Bootloader to include information about the bootloader implementation.

10.4 Revision 1.2

Updated Port I/O specifications in 4.1.12 Port I/O to include new V_{OL} specifications.

Added a note to Table 4.3 Reset and Supply Monitor on page 15 regarding guaranteed operation.

Updated package diagram and landing diagram specifications for the QFN20 package.

10.5 Revision 1.1

Initial release.

Table of Contents

1. Feature List . . . 1

2. Ordering Information . . . 2

3. System Overview . . . 4

3.1 Introduction . . . 4

3.2 Power . . . 5

3.3 I/O . . . 5

3.4 Clocking . . . 5

3.5 Counters/Timers and PWM . . . 6

3.6 Communications and Other Digital Peripherals . . . 7

3.7 Analog . . . 8

3.8 Reset Sources . . . 9

3.9 Debugging . . . 9

3.10 Bootloader . . . 10

4. Electrical Specifications . . . 12

4.1 Electrical Characteristics . . . 12

4.1.1 Recommended Operating Conditions . . . 12

4.1.2 Power Consumption . . . 13

4.1.3 Reset and Supply Monitor . . . 15

4.1.4 Flash Memory . . . 16

4.1.5 Internal Oscillators . . . 16

4.1.6 External Clock Input . . . 17

4.1.7 ADC . . . 18

4.1.8 Voltage Reference . . . 19

4.1.9 Temperature Sensor . . . 20

4.1.10 1.8 V Internal LDO Voltage Regulator . . . 20

4.1.11 Comparators . . . 21

4.1.12 Port I/O . . . 23

4.1.13 SMBus . . . 24

4.2 Thermal Conditions . . . 26

4.3 Absolute Maximum Ratings . . . 26

4.4 Typical Performance Curves . . . 27

5. Typical Connection Diagrams . . . 31

5.1 Power . . . 31

5.2 Debug . . . 31

5.3 Other Connections . . . 32

6. Pin Definitions . . . 33

6.1 EFM8BB1x-QSOP24 Pin Definitions . . . 33

6.2 EFM8BB1x-QFN20 Pin Definitions . . . 36

6.3 EFM8BB1x-SOIC16 Pin Definitions 39
7. QSOP24 Package Specifications 41
7.1 QSOP24 Package Dimensions 41
7.2 QSOP24 PCB Land Pattern 43
7.3 QSOP24 Package Marking 44
8. QFN20 Package Specifications. 45
8.1 QFN20 Package Dimensions 45
8.2 QFN20 PCB Land Pattern 47
8.3 QFN20 Package Marking 48
9. SOIC16 Package Specifications 49
9.1 SOIC16 Package Dimensions 49
9.2 SOIC16 PCB Land Pattern 51
9.3 SOIC16 Package Marking 52
10. Revision History. 53
10.1 Revision 1.5 53
10.2 Revision 1.4 53
10.3 Revision 1.3 53
10.4 Revision 1.2 53
10.5 Revision 1.1 53
Table of Contents 54