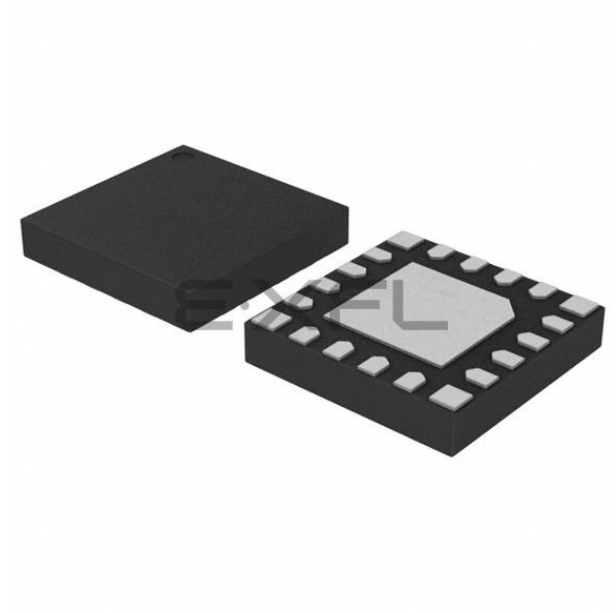

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-WFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8bb10f8a-a-qfn20r

2. Ordering Information

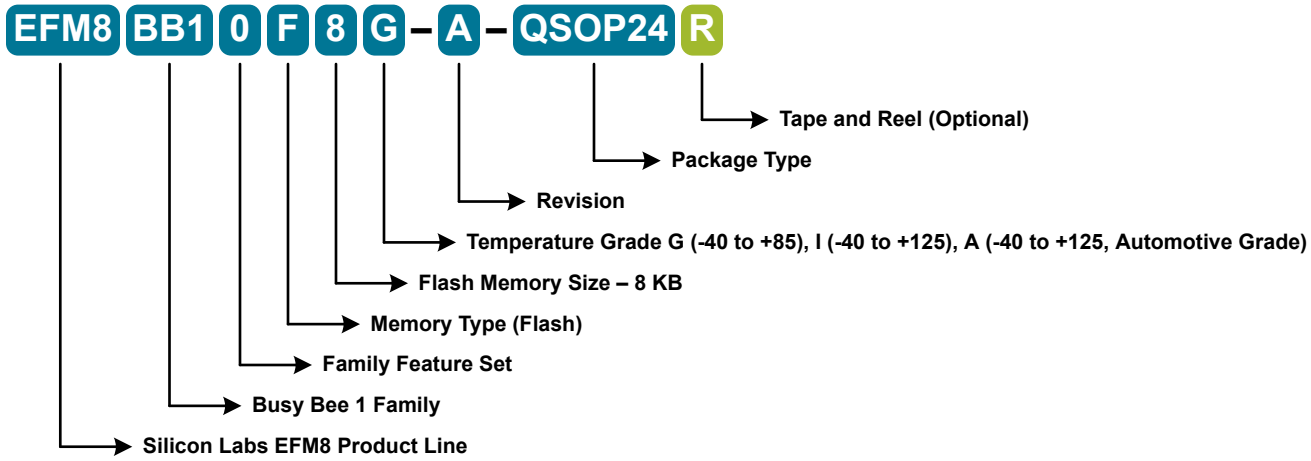


Figure 2.1. EFM8BB1 Part Numbering

All EFM8BB1 family members have the following features:

- CIP-51 Core running up to 25 MHz
- Two Internal Oscillators (24.5 MHz and 80 kHz)
- SMBus / I2C
- SPI
- UART
- 3-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- 4 16-bit Timers
- 2 Analog Comparators
- 12-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, and temperature sensor
- 16-bit CRC Unit
- AEC-Q100 qualified
- Pre-loaded UART bootloader

In addition to these features, each part number in the EFM8BB1 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB10F8G-A-QSOP24	8	512	18	16	8	8	Yes	-40 to +85 C	QSOP24
EFM8BB10F8G-A-QFN20	8	512	16	15	8	7	Yes	-40 to +85 C	QFN20
EFM8BB10F8G-A-SOIC16	8	512	13	12	6	6	Yes	-40 to +85 C	SOIC16
EFM8BB10F4G-A-QFN20	4	512	16	15	8	7	Yes	-40 to +85 C	QFN20
EFM8BB10F2G-A-QFN20	2	256	16	15	8	7	Yes	-40 to +85 C	QFN20
EFM8BB10F8I-A-QSOP24	8	512	18	16	8	8	Yes	-40 to +125 C	QSOP24

3.7 Analog

12-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12-, 10-, and 8-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 16 external inputs.
- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 200 ksps samples per second in 12-bit mode or 800 ksps samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer sources.
- Output data window comparator allows automatic range checking.
- Support for burst mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Includes an internal fast-settling reference with two levels (1.65 V and 2.4 V) and support for external reference and signal ground.
- Integrated temperature sensor.

Low Current Comparators (CMP0, CMP1)

Analog comparators are used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator module includes the following features:

- Up to 8 external positive inputs.
- Up to 8 external negative inputs.
- Additional input options:
  - Internal connection to LDO output.
  - Direct connection to GND.
- Synchronous and asynchronous outputs can be routed to pins via crossbar.
- Programmable hysteresis between 0 and ±20 mV
- Programmable response time.
- Interrupts generated on rising, falling, or both edges.

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 4.1 Recommended Operating Conditions on page 12, unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		2.2	—	3.6	V
System Clock Frequency	f_{SYSCLK}		0	—	25	MHz
Operating Ambient Temperature	T_A	G-grade devices	–40	—	85	°C
		I-grade or A-grade devices	-40	—	125	°C

Note:
1. All voltages with respect to GND
2. GPIO levels are undefined whenever VDD is less than 1 V.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC0 Always-on[4]	I_{ADC}	800 ksps, 10-bit conversions or 200 ksps, 12-bit conversions Normal bias settings V_{DD} = 3.0 V	—	845	1200	µA
		250 ksps, 10-bit conversions or 62.5 ksps 12-bit conversions Low power bias settings V_{DD} = 3.0 V	—	425	580	µA
ADC0 Burst Mode, 10-bit single conversions, external reference	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	370	—	µA
		100 ksps, V_{DD} = 3.0 V	—	185	—	µA
		10 ksps, V_{DD} = 3.0 V	—	19	—	µA
ADC0 Burst Mode, 10-bit single conversions, internal reference, Low power bias settings	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	490	—	µA
		100 ksps, V_{DD} = 3.0 V	—	245	—	µA
		10 ksps, V_{DD} = 3.0 V	—	23	—	µA
ADC0 Burst Mode, 12-bit single conversions, external reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V	—	530	—	µA
		50 ksps, V_{DD} = 3.0 V	—	265	—	µA
		10 ksps, V_{DD} = 3.0 V	—	53	—	µA
ADC0 Burst Mode, 12-bit single conversions, internal reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V, Normal bias	—	950	—	µA
		50 ksps, V_{DD} = 3.0 V, Low power bias	—	420	—	µA
		10 ksps, V_{DD} = 3.0 V, Low power bias	—	85	—	µA
Internal ADC0 Reference, Always-on[5]	I_{VREFFS}	Normal Power Mode	—	680	790	µA
		Low Power Mode	—	160	210	µA
Temperature Sensor	I_{TSENSE}		—	75	120	µA
Comparator 0 (CMP0), Comparator 1 (CMP1)	I_{CMP}	CPMD = 11	—	0.5	—	µA
		CPMD = 10	—	3	—	µA
		CPMD = 01	—	10	—	µA
		CPMD = 00	—	25	—	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	20	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 always-on power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.

4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{DD} Supply Monitor Threshold	V_{VDDM}		1.85[1]	1.95	2.1	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on V_{DD}	—	1.4	—	V
		Falling Voltage on V_{DD}	0.75	—	1.36	V
V_{DD} Ramp Time	t_{RMP}	Time to $V_{DD} \geq 2.2$ V	10	—	—	µs
Reset Delay from POR	t_{POR}	Relative to $V_{DD} \geq V_{POR}$	3	10	31	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	39	—	µs
RST Low Time to Generate Reset	t_{RSTL}		15	—	—	µs
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	$F_{SYSCLK} > 1$ MHz	—	0.625	1.2	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	7.5	13.5	kHz
V_{DD} Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

Note:

1. MCU core, digital logic, flash memory, and RAM operation is guaranteed down to the minimum VDD Supply Monitor Threshold.

4.1.11 Comparators

Table 4.11. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		–100 mV Differential	—	150	—	ns
Response Time, CPMD = 11 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.5	—	µs
		–100 mV Differential	—	3.5	—	µs
Positive Hysterisis Mode 0 (CPMD = 00)	HYS_{CP+}	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysterisis Mode 0 (CPMD = 00)	HYS_{CP-}	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	–8	—	mV
		CPHYN = 10	—	–16	—	mV
		CPHYN = 11	—	–32	—	mV
Positive Hysterisis Mode 1 (CPMD = 01)	HYS_{CP+}	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysterisis Mode 1 (CPMD = 01)	HYS_{CP-}	CPHYN = 00	—	-0.5	—	mV
		CPHYN = 01	—	–6	—	mV
		CPHYN = 10	—	–12	—	mV
		CPHYN = 11	—	–24	—	mV
Positive Hysterisis Mode 2 (CPMD = 10)	HYS_{CP+}	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysterisis Mode 2 (CPMD = 10)	HYS_{CP-}	CPHYN = 00	—	-0.6	—	mV
		CPHYN = 01	—	–4.5	—	mV
		CPHYN = 10	—	–9	—	mV
		CPHYN = 11	—	–18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV

4.1.12 Port I/O

Table 4.12. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (Low Drive)[1]	V_{OH}	I_{OH} = –1 mA	V_{DD} – 0.7	—	—	V
Output High Voltage (High Drive)[1]	V_{OH}	I_{OH} = –3 mA	V_{DD} – 0.7	—	—	V
Output Low Voltage (Low Drive)[1]	V_{OL}	I_{OL} = 1.4 mA	—	—	0.6	V
Output Low Voltage (High Drive)[1]	V_{OL}	I_{OL} = 8.5 mA	—	—	0.6	V
Output Low Voltage (High Drive)[1]	V_{OL}	I_{OL} = 10 mA -10 °C ≤ T_A ≤ 60 °C V_{DD} = 3.0 V Guaranteed by characterization	—	0.25	0.33	V
Output Low Voltage (High Drive)[1]	V_{OL}	I_{OL} = 10 mA -10 °C ≤ T_A ≤ 60 °C V_{DD} = 3.6 V Guaranteed by characterization	—	0.23	0.31	V
Input High Voltage	V_{IH}		V_{DD} – 0.6	—	—	V
Input Low Voltage	V_{IL}		—	—	0.6	V
Pin Capacitance	C_{IO}		—	7	—	pF
Weak Pull-Up Current (V_{IN} = 0 V)	I_{PU}	V_{DD} = 3.6	–30	–20	–10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	GND < V_{IN} < V_{DD}	–1.1	—	1.1	µA
Input Leakage Current with V_{IN} above V_{DD}	I_{LK}	V_{DD} < V_{IN} < V_{DD}+2.0 V	0	5	150	µA

Note:
1. See Figure 4.6 Typical V_{OH} Curves on page 30 and Figure 4.7 Typical V_{OL} Curves on page 30 for more information.

4.1.13 SMBus

Table 4.13. SMBus Peripheral Timing Performance (Master Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Mode (100 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	70[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	70[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		9.4	—	—	µs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		4.7	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		9.4	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		9.4	—	—	µs
Data Hold Time	$t_{HD:DAT}$		489[3]	—	—	ns
Data Setup Time	$t_{SU:DAT}$		448[3]	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		4.7	—	—	µs
Clock High Period	t_{HIGH}		9.4	—	50[4]	µs
Fast Mode (400 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	255[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	255[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		2.6	—	—	µs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		1.3	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		2.6	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		2.6	—	—	µs
Data Hold Time	$t_{HD:DAT}$		489[3]	—	—	ns
Data Setup Time	$t_{SU:DAT}$		448[3]	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		1.3	—	—	µs
Clock High Period	t_{HIGH}		2.6	—	50[4]	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications. The maximum frequency cannot be achieved with all combinations of oscillators and dividers available, but the effective frequency must not exceed 256 kHz.
3. Data setup and hold timing at 25 MHz or lower with EXTHOLD set to 1.
4. SMBus has a maximum requirement of 50 µs for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50 µs. I2C can support periods longer than 50 µs.

Table 4.14. SMBus Peripheral Timing Formulas (Master Mode)

Parameter	Symbol	Clocks
SMBus Operating Frequency	f_{SMB}	f_{CSO} / 3
Bus Free Time Between STOP and START Conditions	t_{BUF}	2 / f_{CSO}
Hold Time After (Repeated) START Condition	$t_{HD:STA}$	1 / f_{CSO}
Repeated START Condition Setup Time	$t_{SU:STA}$	2 / f_{CSO}
STOP Condition Setup Time	$t_{SU:STO}$	2 / f_{CSO}
Clock Low Period	t_{LOW}	1 / f_{CSO}
Clock High Period	t_{HIGH}	2 / f_{CSO}

Note:

1. f_{CSO} is the SMBus peripheral clock source overflow frequency.

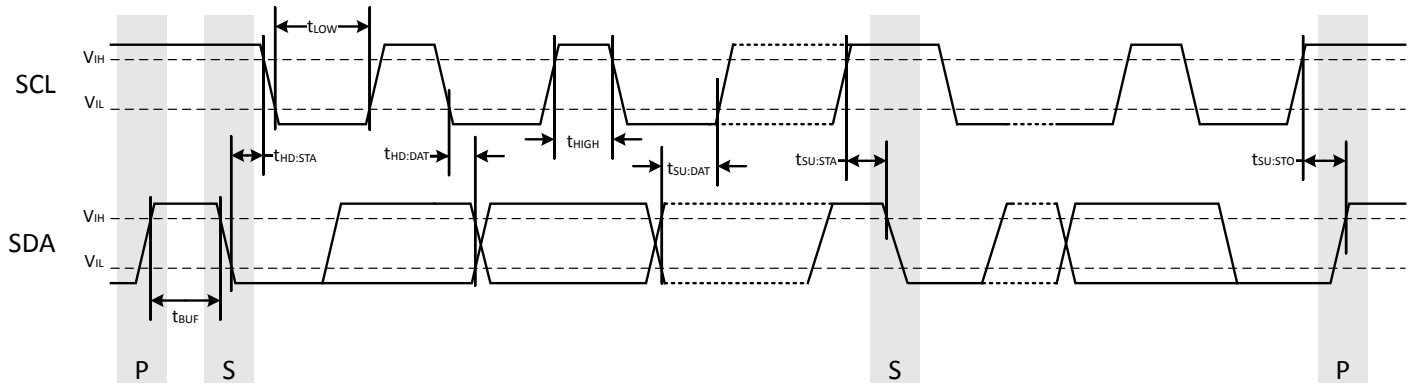


Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)

4.4 Typical Performance Curves

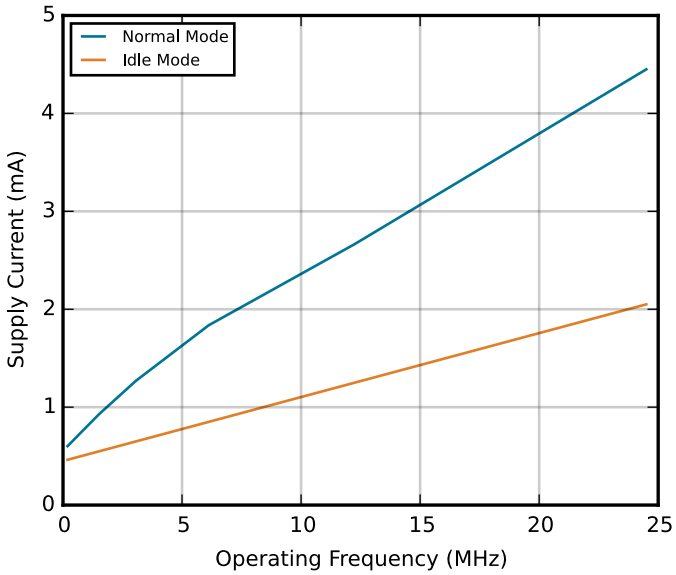


Figure 4.2. Typical Operating Supply Current using HFOSC0

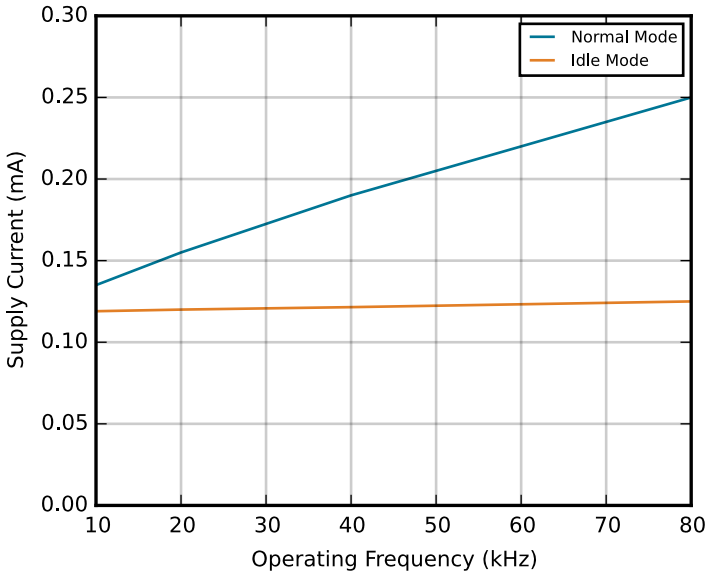


Figure 4.3. Typical Operating Supply Current using LFOSC

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Power Connection Diagram on page 31 shows a typical connection diagram for the power pins of the EFM8BB1 devices.

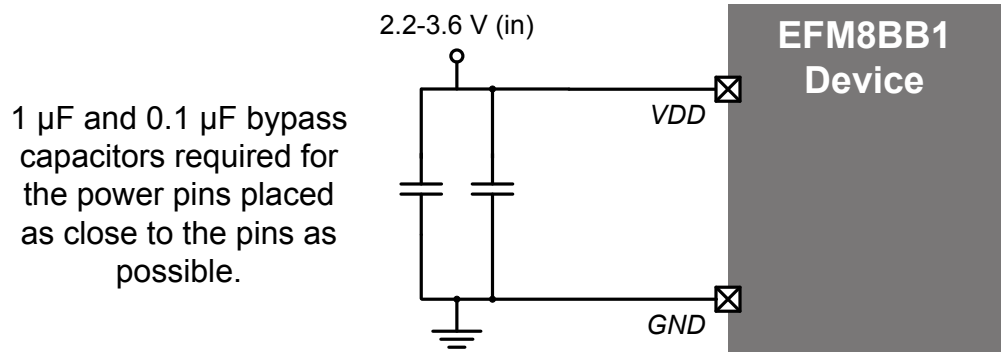


Figure 5.1. Power Connection Diagram

5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in application note, "AN127: Pin Sharing Techniques for the C2 Interface." Application notes can be found on the Silicon Labs website (http://www.silabs.com/8bit-appnotes) or in Simplicity Studio.

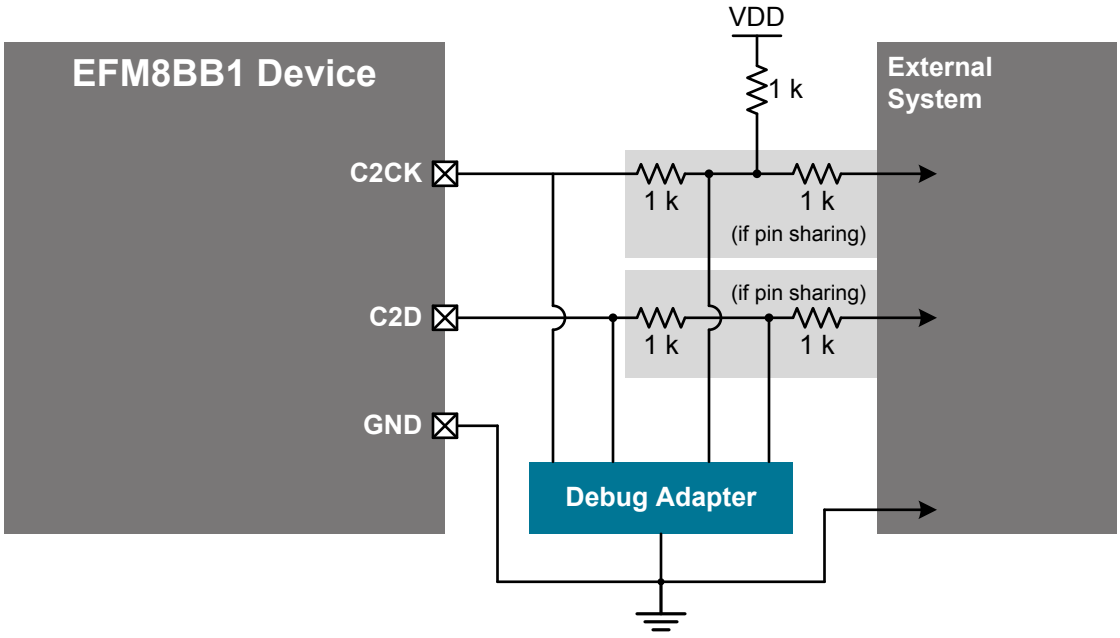


Figure 5.2. Debug Connection Diagram

6. Pin Definitions

6.1 EFM8BB1x-QSOP24 Pin Definitions

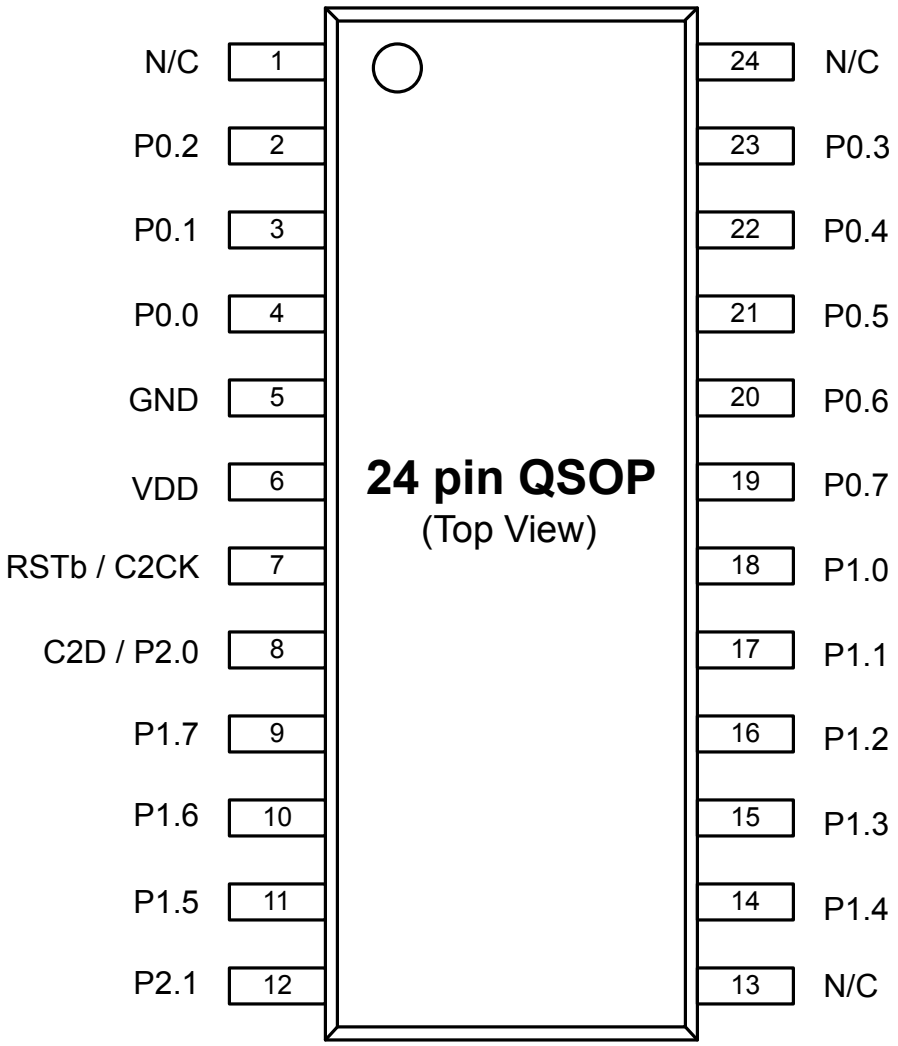


Figure 6.1. EFM8BB1x-QSOP24 Pinout

Table 6.1. Pin Definitions for EFM8BB1x-QSOP24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	N/C	No Connection			
2	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.2 CMP0N.2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
3	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1 AGND
4	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF
5	GND	Ground			
6	VDD	Supply Power Input			
7	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
8	P2.0 / C2D	Multifunction I/O / C2 Debug Data			
9	P1.7	Multifunction I/O	Yes	P1MAT.7	ADC0.15 CMP1P.7 CMP1N.7
10	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.14 CMP1P.6 CMP1N.6
11	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.13 CMP1P.5 CMP1N.5
12	P2.1	Multifunction I/O			
13	N/C	No Connection			
14	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP1P.4 CMP1N.4
15	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CMP1P.3 CMP1N.3
16	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CMP1P.2 CMP1N.2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
4	GND	Ground			
5	VDD	Supply Power Input			
6	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
7	P2.0 / C2D	Multifunction I/O / C2 Debug Data			
8	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CMP1P.5 CMP1N.5
9	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CMP1P.4 CMP1N.4
10	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CMP1P.3 CMP1N.3
11	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CMP1P.2 CMP1N.2
12	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CMP1P.1 CMP1N.1
13	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP1P.0 CMP1N.0
14	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CMP0P.5 CMP0N.5
15	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CMP0P.4 CMP0N.4
16	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CMP0P.3 CMP0N.3

7. QSOP24 Package Specifications

7.1 QSOP24 Package Dimensions

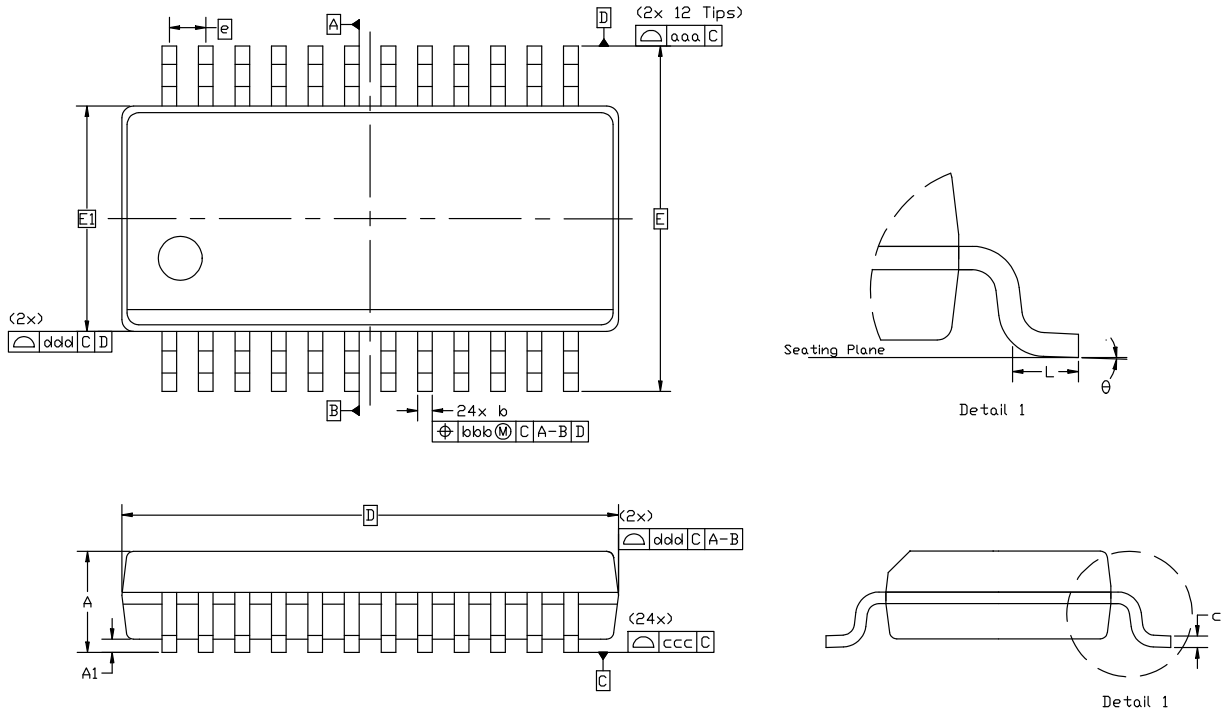


Figure 7.1. QSOP24 Package Drawing

Table 7.1. QSOP24 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.20	—	0.30
c	0.10	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	0.635 BSC		
L	0.40	—	1.27
theta	0°	—	8°

7.2 QSOP24 PCB Land Pattern

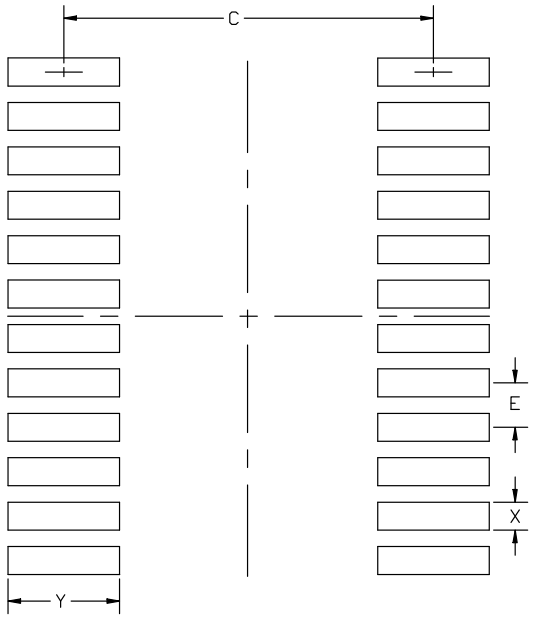


Figure 7.2. QSOP24 PCB Land Pattern Drawing

Table 7.2. QSOP24 PCB Land Pattern Dimensions

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 QSOP24 Package Marking

Figure 7.3. QSOP24 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

9.2 SOIC16 PCB Land Pattern

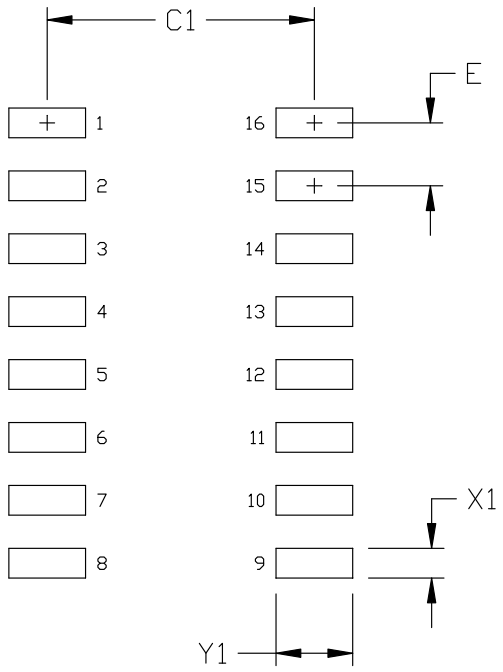


Figure 9.2. SOIC16 PCB Land Pattern Drawing

Table 9.2. SOIC16 PCB Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
3. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

10. Revision History

10.1 Revision 1.5

October 7th, 2016

Added A-grade parts.

Added specifications for 4.1.13 SMBus.

Added bootloader pinout information to 3.10 Bootloader.

Added CRC Calculation Time to 4.1.4 Flash Memory.

Added Thermal Resistance (Junction to Case) for QFN20 packages to 4.2 Thermal Conditions.

Added a note linking to the Typical VOH and VOL Performance graphs in 4.1.12 Port I/O.

Added 4.1.10 1.8 V Internal LDO Voltage Regulator.

Added a note to 3.1 Introduction referencing the Reference Manual.

10.2 Revision 1.4

April 22nd, 2016

Added a reference to *AN945: EFM8 Factory Bootloader User Guide* in 3.10 Bootloader.

Added I-grade devices.

Added a note that all GPIO values are undefined when VDD is below 1 V to 4.1.1 Recommended Operating Conditions.

Adjusted the Total Current Sunk into Supply Pin and Total Current Sourced out of Ground Pin specifications in 4.3 Absolute Maximum Ratings.

10.3 Revision 1.3

January 7th, 2016

Added 5.2 Debug.

Updated 3.10 Bootloader to include information about the bootloader implementation.

10.4 Revision 1.2

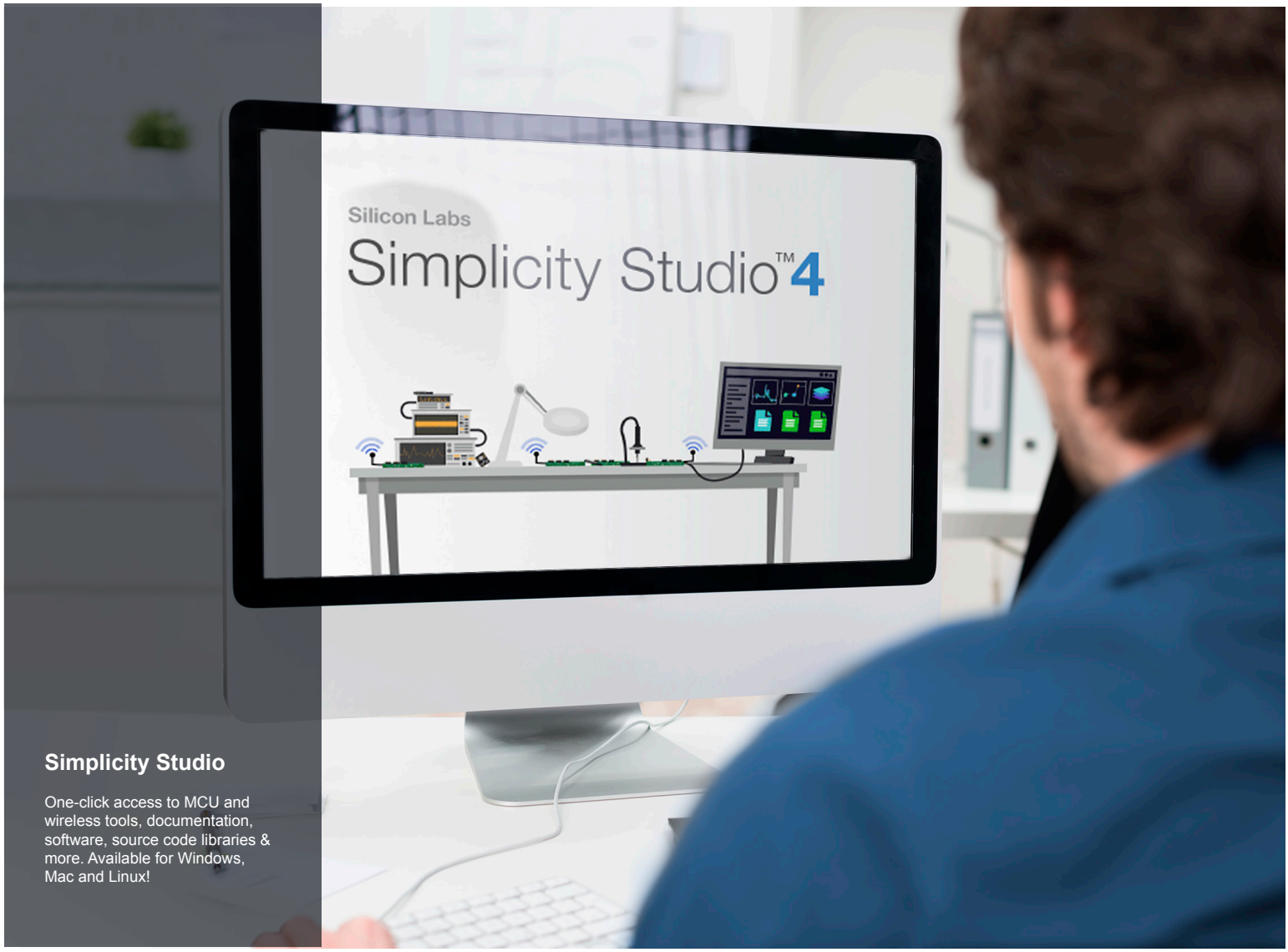
Updated Port I/O specifications in 4.1.12 Port I/O to include new V_{OL} specifications.

Added a note to Table 4.3 Reset and Supply Monitor on page 15 regarding guaranteed operation.

Updated package diagram and landing diagram specifications for the QFN20 package.

10.5 Revision 1.1

Initial release.



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