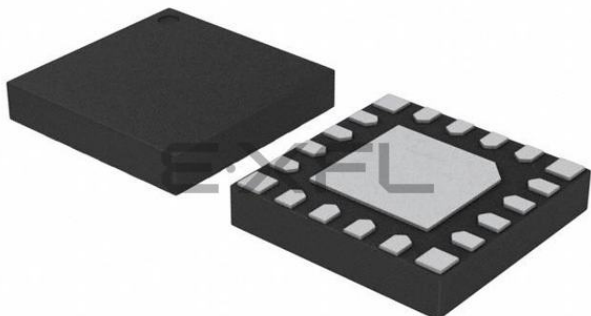




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8bb10f8g-a-qfn20r

2. Ordering Information

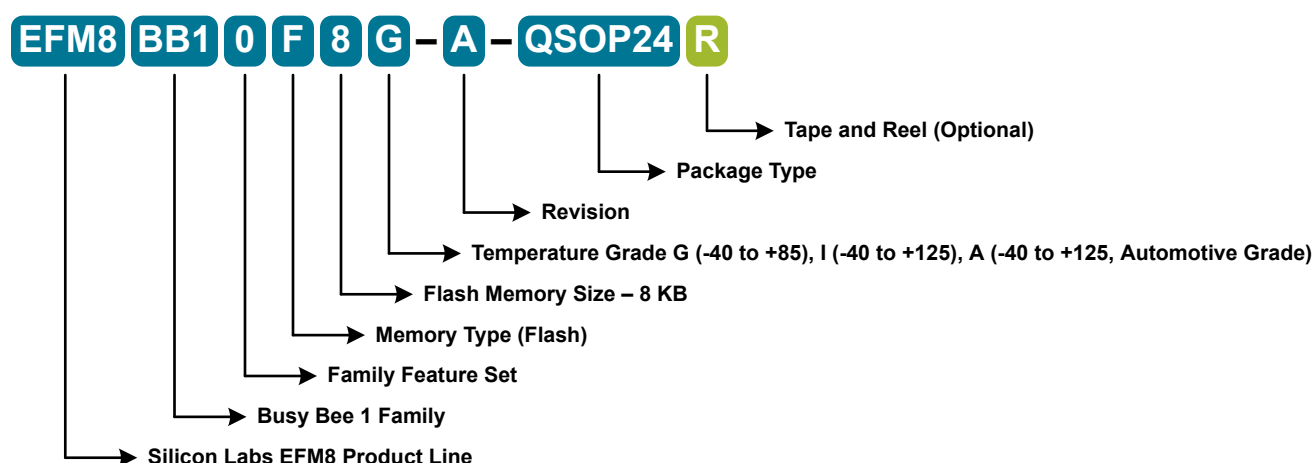


Figure 2.1. EFM8BB1 Part Numbering

All EFM8BB1 family members have the following features:

- CIP-51 Core running up to 25 MHz
- Two Internal Oscillators (24.5 MHz and 80 kHz)
- SMBus / I2C
- SPI
- UART
- 3-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- 4 16-bit Timers
- 2 Analog Comparators
- 12-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, and temperature sensor
- 16-bit CRC Unit
- AEC-Q100 qualified
- Pre-loaded UART bootloader

In addition to these features, each part number in the EFM8BB1 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB10F8G-A-QSOP24	8	512	18	16	8	8	Yes	-40 to +85 C	QSOP24
EFM8BB10F8G-A-QFN20	8	512	16	15	8	7	Yes	-40 to +85 C	QFN20
EFM8BB10F8G-A-SOIC16	8	512	13	12	6	6	Yes	-40 to +85 C	SOIC16
EFM8BB10F4G-A-QFN20	4	512	16	15	8	7	Yes	-40 to +85 C	QFN20
EFM8BB10F2G-A-QFN20	2	256	16	15	8	7	Yes	-40 to +85 C	QFN20
EFM8BB10F8I-A-QSOP24	8	512	18	16	8	8	Yes	-40 to +125 C	QSOP24

3. System Overview

3.1 Introduction

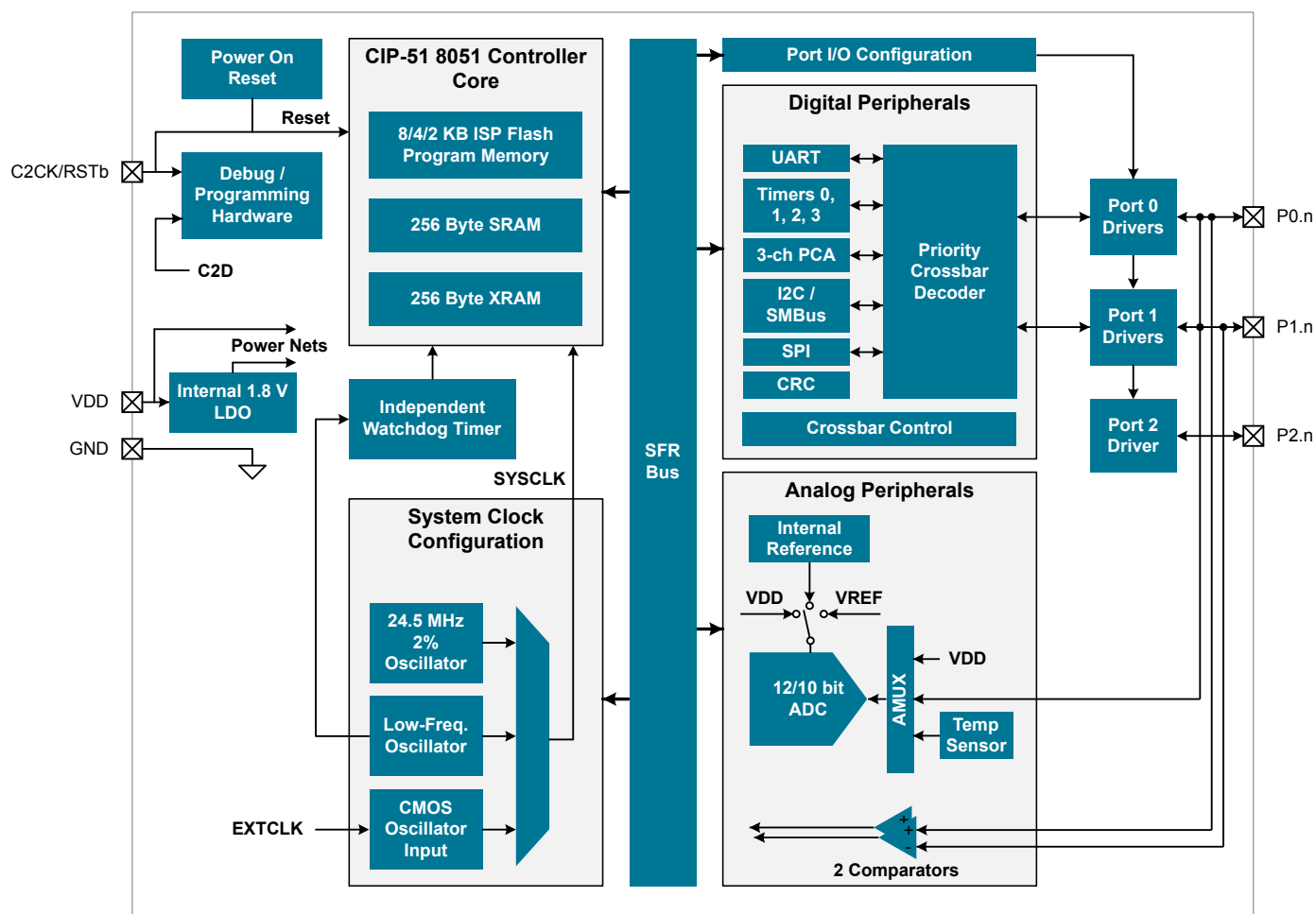


Figure 3.1. Detailed EFM8BB1 Block Diagram

This section describes the EFM8BB1 family at a high level. For more information on each module including register definitions, see the EFM8BB1 Reference Manual.

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational	—	—
Idle	- Core halted - All peripherals clocked and fully operational - Code resumes execution on wake event	Set IDLE bit in PCON0	Any interrupt
Stop	- All internal power nets shut down - Pins retain state - Exit on any reset source	1. Clear STOPCF bit in REG0CN 2. Set STOP bit in PCON0	Any reset source
Shutdown	- All internal power nets shut down - Pins retain state - Exit on pin or power-on reset	1. Set STOPCF bit in REG0CN 2. Set STOP bit in PCON0	- RSTb pin reset - Power-on reset

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P1.7 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.0 and P2.1 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P2.0.

- Up to 18 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 16 direct-pin interrupt sources with shared interrupt vector (Port Match).

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

- Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to $\pm 2\%$ over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External CMOS clock input (EXTCLK).
- Clock divider with eight settings for flexible clock scaling: Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.

3.5 Counters/Timers and PWM

Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base
- Programmable clock divisor and clock source selection
- Up to three independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation)
- Output polarity control
- Frequency output mode
- Capture on rising, falling or any edge
- Compare function for arbitrary waveform generation
- Software timer (internal compare) mode
- Can accept hardware “kill” signal from comparator 0

Timers (Timer 0, Timer 1, Timer 2, and Timer 3)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2 and Timer 3 are 16-bit timers including the following features:

- Clock sources include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8.
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- External pin capture (Timer 2)
- LFOSC0 capture (Timer 3)

Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) running off the low-frequency oscillator. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the RST pin is unaffected by this reset.

The Watchdog Timer has the following features:

- Programmable timeout interval
- Runs from the low-frequency oscillator
- Lock-out feature to prevent any modification until a system reset

3.6 Communications and Other Digital Peripherals

Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions.
- Baud rates up to $\text{SYSCLK}/2$ (transmit) or $\text{SYSCLK}/8$ (receive).
- 8- or 9-bit data.
- Automatic start and stop generation.
- Single-byte FIFO on transmit and receive.

Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

The SPI module includes the following features:

- Supports 3- or 4-wire operation in master or slave modes.
- Supports external clock frequencies up to $\text{SYSCLK} / 2$ in master mode and $\text{SYSCLK} / 10$ in slave mode.
- Support for four clock phase and polarity options.
- 8-bit dedicated clock rate generator.
- Support for multiple masters on the same data lines.

System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I²C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to inhibit all slave states.
- Programmable data setup/hold times.

16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- Automatic CRC of flash contents on one or more 256-byte blocks
- Initial seed selection of 0x0000 or 0xFFFF

3.7 Analog

12-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12-, 10-, and 8-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 16 external inputs.
- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 200 ksps samples per second in 12-bit mode or 800 ksps samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer sources.
- Output data window comparator allows automatic range checking.
- Support for burst mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Includes an internal fast-settling reference with two levels (1.65 V and 2.4 V) and support for external reference and signal ground.
- Integrated temperature sensor.

Low Current Comparators (CMP0, CMP1)

Analog comparators are used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator module includes the following features:

- Up to 8 external positive inputs.
- Up to 8 external negative inputs.
- Additional input options:
 - Internal connection to LDO output.
 - Direct connection to GND.
- Synchronous and asynchronous outputs can be routed to pins via crossbar.
- Programmable hysteresis between 0 and ± 20 mV
- Programmable response time.
- Interrupts generated on rising, falling, or both edges.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC0 Always-on ⁴	I_{ADC}	800 ksps, 10-bit conversions or 200 ksps, 12-bit conversions Normal bias settings $V_{DD} = 3.0\text{ V}$	—	845	1200	μA
		250 ksps, 10-bit conversions or 62.5 ksps 12-bit conversions Low power bias settings $V_{DD} = 3.0\text{ V}$	—	425	580	μA
ADC0 Burst Mode, 10-bit single conversions, external reference	I_{ADC}	200 ksps, $V_{DD} = 3.0\text{ V}$	—	370	—	μA
		100 ksps, $V_{DD} = 3.0\text{ V}$	—	185	—	μA
		10 ksps, $V_{DD} = 3.0\text{ V}$	—	19	—	μA
ADC0 Burst Mode, 10-bit single conversions, internal reference, Low power bias settings	I_{ADC}	200 ksps, $V_{DD} = 3.0\text{ V}$	—	490	—	μA
		100 ksps, $V_{DD} = 3.0\text{ V}$	—	245	—	μA
		10 ksps, $V_{DD} = 3.0\text{ V}$	—	23	—	μA
ADC0 Burst Mode, 12-bit single conversions, external reference	I_{ADC}	100 ksps, $V_{DD} = 3.0\text{ V}$	—	530	—	μA
		50 ksps, $V_{DD} = 3.0\text{ V}$	—	265	—	μA
		10 ksps, $V_{DD} = 3.0\text{ V}$	—	53	—	μA
ADC0 Burst Mode, 12-bit single conversions, internal reference	I_{ADC}	100 ksps, $V_{DD} = 3.0\text{ V}$, Normal bias	—	950	—	μA
		50 ksps, $V_{DD} = 3.0\text{ V}$, Low power bias	—	420	—	μA
		10 ksps, $V_{DD} = 3.0\text{ V}$, Low power bias	—	85	—	μA
Internal ADC0 Reference, Always-on ⁵	I_{VREFFS}	Normal Power Mode	—	680	790	μA
		Low Power Mode	—	160	210	μA
Temperature Sensor	I_{TSENSE}		—	75	120	μA
Comparator 0 (CMP0), Comparator 1 (CMP1)	I_{CMP}	CPMD = 11	—	0.5	—	μA
		CPMD = 10	—	3	—	μA
		CPMD = 01	—	10	—	μA
		CPMD = 00	—	25	—	μA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	20	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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Note:

1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 always-on power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.

4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V _{DD} Supply Monitor Threshold	V _{VDDM}		1.85 ¹	1.95	2.1	V
Power-On Reset (POR) Threshold	V _{POR}	Rising Voltage on V _{DD}	—	1.4	—	V
		Falling Voltage on V _{DD}	0.75	—	1.36	V
V _{DD} Ramp Time	t _{RMP}	Time to V _{DD} ≥ 2.2 V	10	—	—	μs
Reset Delay from POR	t _{POR}	Relative to V _{DD} ≥ V _{POR}	3	10	31	ms
Reset Delay from non-POR source	t _{RST}	Time between release of reset source and code execution	—	39	—	μs
RST Low Time to Generate Reset	t _{RSTL}		15	—	—	μs
Missing Clock Detector Response Time (final rising edge to reset)	t _{MCD}	F _{SYSCLK} > 1 MHz	—	0.625	1.2	ms
Missing Clock Detector Trigger Frequency	F _{MCD}		—	7.5	13.5	kHz
V _{DD} Supply Monitor Turn-On Time	t _{MON}		—	2	—	μs

Note:

1. MCU core, digital logic, flash memory, and RAM operation is guaranteed down to the minimum V_{DD} Supply Monitor Threshold.

4.1.9 Temperature Sensor

Table 4.9. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	$T_A = 0\text{ }^{\circ}\text{C}$	—	757	—	mV
Offset Error ¹	E_{OFF}	$T_A = 0\text{ }^{\circ}\text{C}$	—	17	—	mV
Slope	M		—	2.85	—	mV/ $^{\circ}\text{C}$
Slope Error ¹	E_M		—	70	—	$\mu\text{V}/^{\circ}\text{C}$
Linearity			—	0.5	—	$^{\circ}\text{C}$
Turn-on Time			—	1.8	—	μs

Note:

1. Represents one standard deviation from the mean.

4.1.10 1.8 V Internal LDO Voltage Regulator

Table 4.10. 1.8V Internal LDO Voltage Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage	$V_{OUT_1.8V}$		1.74	1.8	1.85	V

4.1.13 SMBus

Table 4.13. SMBus Peripheral Timing Performance (Master Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Mode (100 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	70 ²	kHz
SMBus Operating Frequency	f_{SMB}		40 ¹	—	70 ²	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		9.4	—	—	μ s
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		4.7	—	—	μ s
Repeated START Condition Setup Time	$t_{SU:STA}$		9.4	—	—	μ s
STOP Condition Setup Time	$t_{SU:STO}$		9.4	—	—	μ s
Data Hold Time	$t_{HD:DAT}$		489 ³	—	—	ns
Data Setup Time	$t_{SU:DAT}$		448 ³	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		4.7	—	—	μ s
Clock High Period	t_{HIGH}		9.4	—	50 ⁴	μ s
Fast Mode (400 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	255 ²	kHz
SMBus Operating Frequency	f_{SMB}		40 ¹	—	255 ²	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		2.6	—	—	μ s
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		1.3	—	—	μ s
Repeated START Condition Setup Time	$t_{SU:STA}$		2.6	—	—	μ s
STOP Condition Setup Time	$t_{SU:STO}$		2.6	—	—	μ s
Data Hold Time	$t_{HD:DAT}$		489 ³	—	—	ns
Data Setup Time	$t_{SU:DAT}$		448 ³	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		1.3	—	—	μ s
Clock High Period	t_{HIGH}		2.6	—	50 ⁴	μ s

4.4 Typical Performance Curves

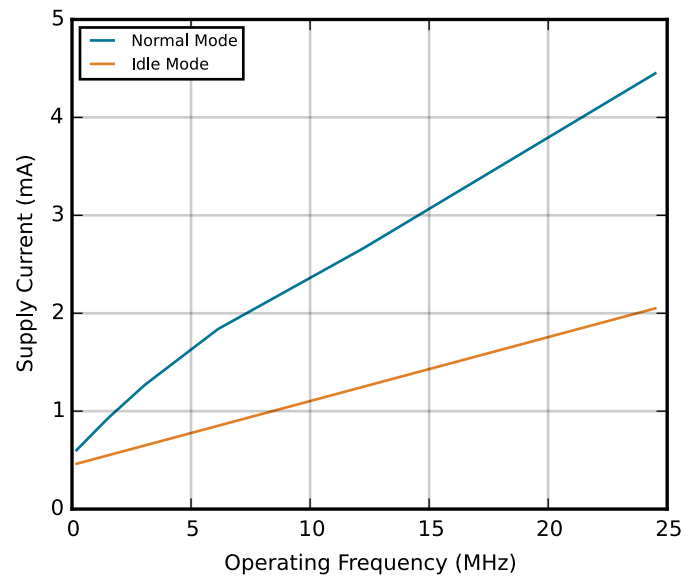


Figure 4.2. Typical Operating Supply Current using HFOSC0

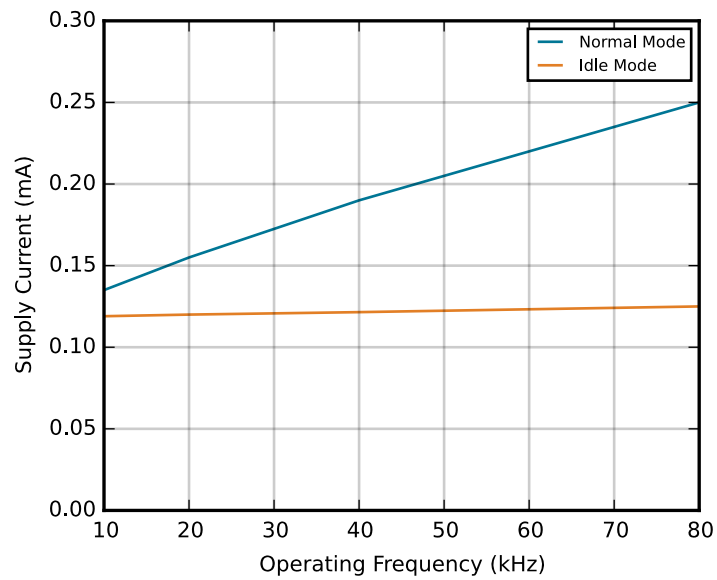


Figure 4.3. Typical Operating Supply Current using LFOSC

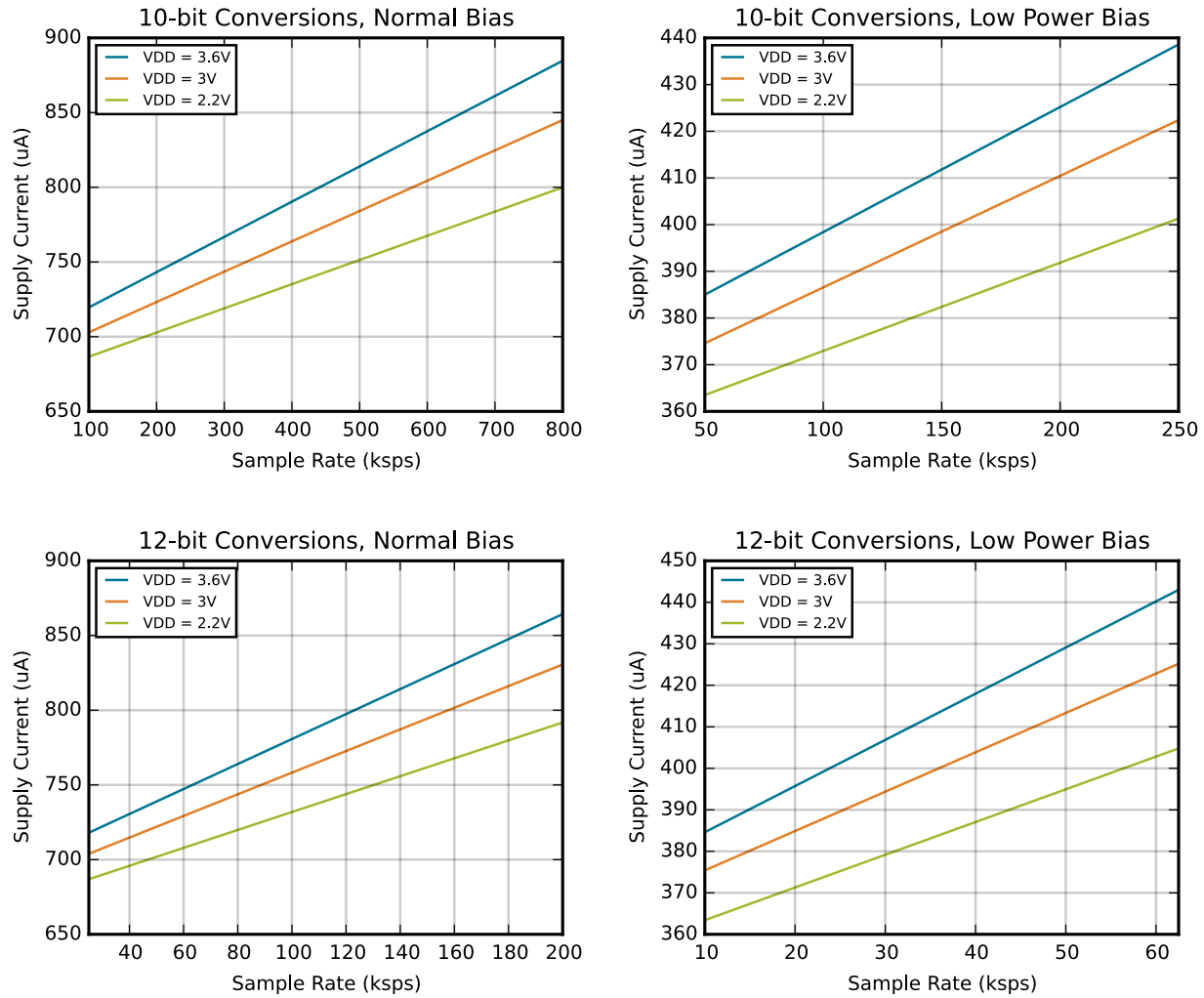


Figure 4.5. Typical ADC0 Supply Current in Normal (always-on) Mode

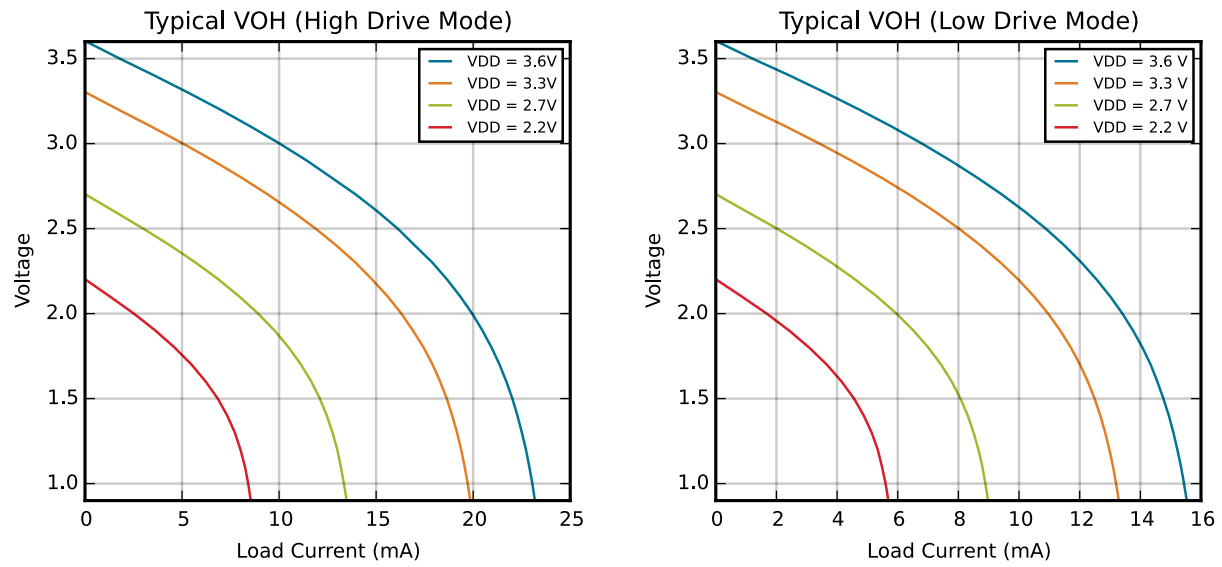


Figure 4.6. Typical V_{OH} Curves

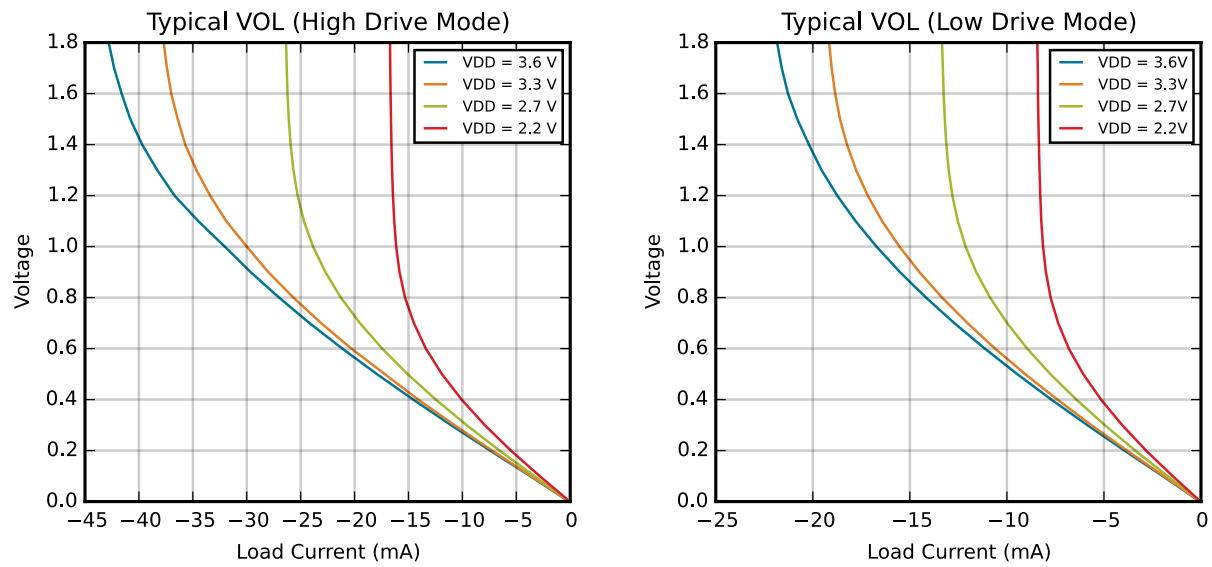


Figure 4.7. Typical V_{OL} Curves

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application note, "AN203: 8-bit MCU Printed Circuit Board Design Notes", contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/8bit-appnotes).

6.2 EFM8BB1x-QFN20 Pin Definitions

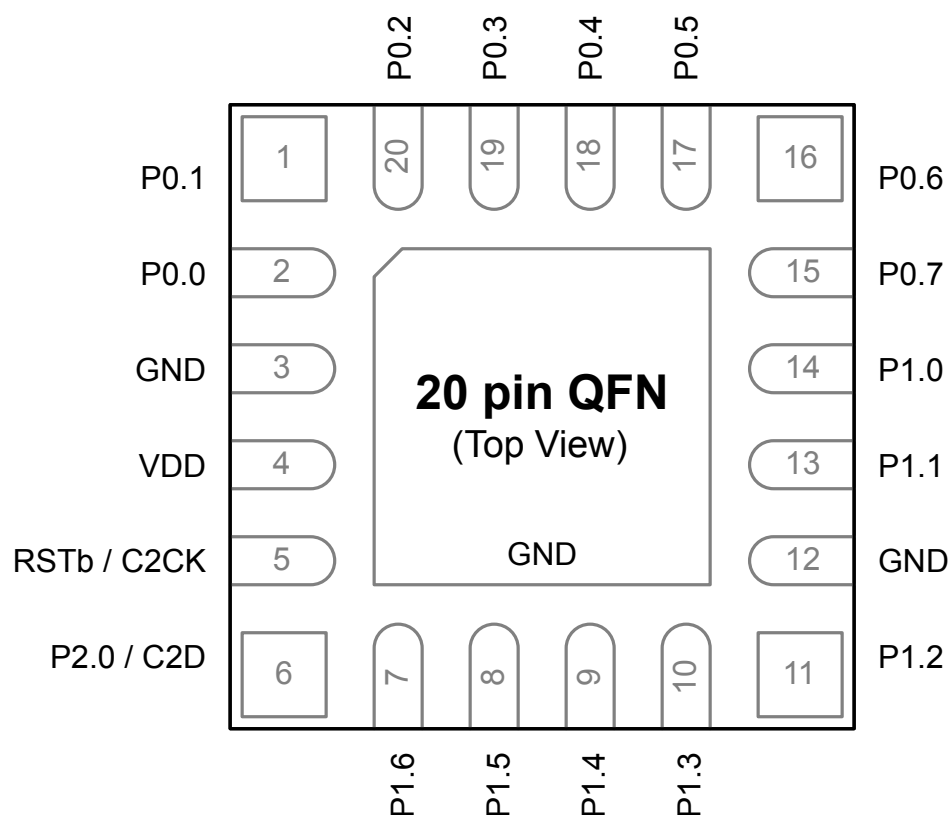


Figure 6.2. EFM8BB1x-QFN20 Pinout

Table 6.2. Pin Definitions for EFM8BB1x-QFN20

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1 AGND
2	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
4	GND	Ground			
5	VDD	Supply Power Input			
6	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
7	P2.0 / C2D	Multifunction I/O / C2 Debug Data			
8	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CMP1P.5 CMP1N.5
9	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CMP1P.4 CMP1N.4
10	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CMP1P.3 CMP1N.3
11	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CMP1P.2 CMP1N.2
12	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CMP1P.1 CMP1N.1
13	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP1P.0 CMP1N.0
14	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CMP0P.5 CMP0N.5
15	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CMP0P.4 CMP0N.4
16	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CMP0P.3 CMP0N.3

7.3 QSOP24 Package Marking



Figure 7.3. QSOP24 Package Marking

The package marking consists of:

- P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

Dimension	Min	Typ	Max
E	3.00 BSC		
E2	1.60	1.70	1.80
f	2.50 BSC		
L	0.30	0.40	0.50
K	0.25 REF		
R	0.09	0.125	0.15
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. The drawing complies with JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Table of Contents

1. Feature List	1
2. Ordering Information	2
3. System Overview	4
3.1 Introduction.	4
3.2 Power	5
3.3 I/O.	5
3.4 Clocking.	5
3.5 Counters/Timers and PWM	6
3.6 Communications and Other Digital Peripherals.	7
3.7 Analog	8
3.8 Reset Sources	9
3.9 Debugging	9
3.10 Bootloader	10
4. Electrical Specifications	12
4.1 Electrical Characteristics	12
4.1.1 Recommended Operating Conditions	12
4.1.2 Power Consumption	13
4.1.3 Reset and Supply Monitor	15
4.1.4 Flash Memory	16
4.1.5 Internal Oscillators.	16
4.1.6 External Clock Input	17
4.1.7 ADC	18
4.1.8 Voltage Reference.	19
4.1.9 Temperature Sensor	20
4.1.10 1.8 V Internal LDO Voltage Regulator	20
4.1.11 Comparators	21
4.1.12 Port I/O	23
4.1.13 SMBus	24
4.2 Thermal Conditions	26
4.3 Absolute Maximum Ratings	26
4.4 Typical Performance Curves	27
5. Typical Connection Diagrams	31
5.1 Power	31
5.2 Debug	31
5.3 Other Connections	32
6. Pin Definitions	33
6.1 EFM8BB1x-QSOP24 Pin Definitions	33
6.2 EFM8BB1x-QFN20 Pin Definitions	36

6.3 EFM8BB1x-SOIC16 Pin Definitions	.39
7. QSOP24 Package Specifications	41
7.1 QSOP24 Package Dimensions	.41
7.2 QSOP24 PCB Land Pattern	.43
7.3 QSOP24 Package Marking	.44
8. QFN20 Package Specifications.	45
8.1 QFN20 Package Dimensions	.45
8.2 QFN20 PCB Land Pattern	.47
8.3 QFN20 Package Marking	.48
9. SOIC16 Package Specifications	49
9.1 SOIC16 Package Dimensions	.49
9.2 SOIC16 PCB Land Pattern	.51
9.3 SOIC16 Package Marking	.52
10. Revision History.	53
10.1 Revision 1.5	.53
10.2 Revision 1.4	.53
10.3 Revision 1.3	.53
10.4 Revision 1.2	.53
10.5 Revision 1.1	.53
Table of Contents	54