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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8bb10f8g-a-soic16

1. Feature List

The EFM8BB1 highlighted features are listed below.

- Core:
 - Pipelined CIP-51 Core
 - Fully compatible with standard 8051 instruction set
 - 70% of instructions execute in 1-2 clock cycles
 - 25 MHz maximum operating frequency
- Memory:
 - Up to 8 kB flash memory, in-system re-programmable from firmware.
 - Up to 512 bytes RAM (including 256 bytes standard 8051 RAM and 256 bytes on-chip XRAM)
- Power:
 - Internal LDO regulator for CPU core voltage
 - Power-on reset circuit and brownout detectors
- I/O: Up to 18 total multifunction I/O pins:
 - All pins 5 V tolerant under bias
 - Flexible peripheral crossbar for peripheral routing
 - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
 - Internal 24.5 MHz oscillator with $\pm 2\%$ accuracy
 - Internal 80 kHz low-frequency oscillator
 - External CMOS clock option
- Timers/Counters and PWM:
 - 3-channel programmable counter array (PCA) supporting PWM, capture/compare, and frequency output modes
 - 4 x 16-bit general-purpose timers
 - Independent watchdog timer, clocked from the low frequency oscillator
- Communications and Digital Peripherals:
 - UART
 - SPI™ Master / Slave
 - SMBus™/I2C™ Master / Slave
 - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
- Analog:
 - 12-Bit Analog-to-Digital Converter (ADC)
 - 2 x Low-current analog comparators with adjustable reference
- On-Chip, Non-Intrusive Debugging
 - Full memory and register inspection
 - Four hardware breakpoints, single-stepping
- Pre-loaded UART bootloader
- Temperature range -40 to 85 °C or -40 to 125 °C
- Single power supply 2.2 to 3.6 V
- QSOP24, SOIC16, and QFN20 packages

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8BB1 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Each device is specified for 2.2 to 3.6 V operation, is AEC-Q100 qualified, and is available in 20-pin QFN, 16-pin SOIC or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

3. System Overview

3.1 Introduction

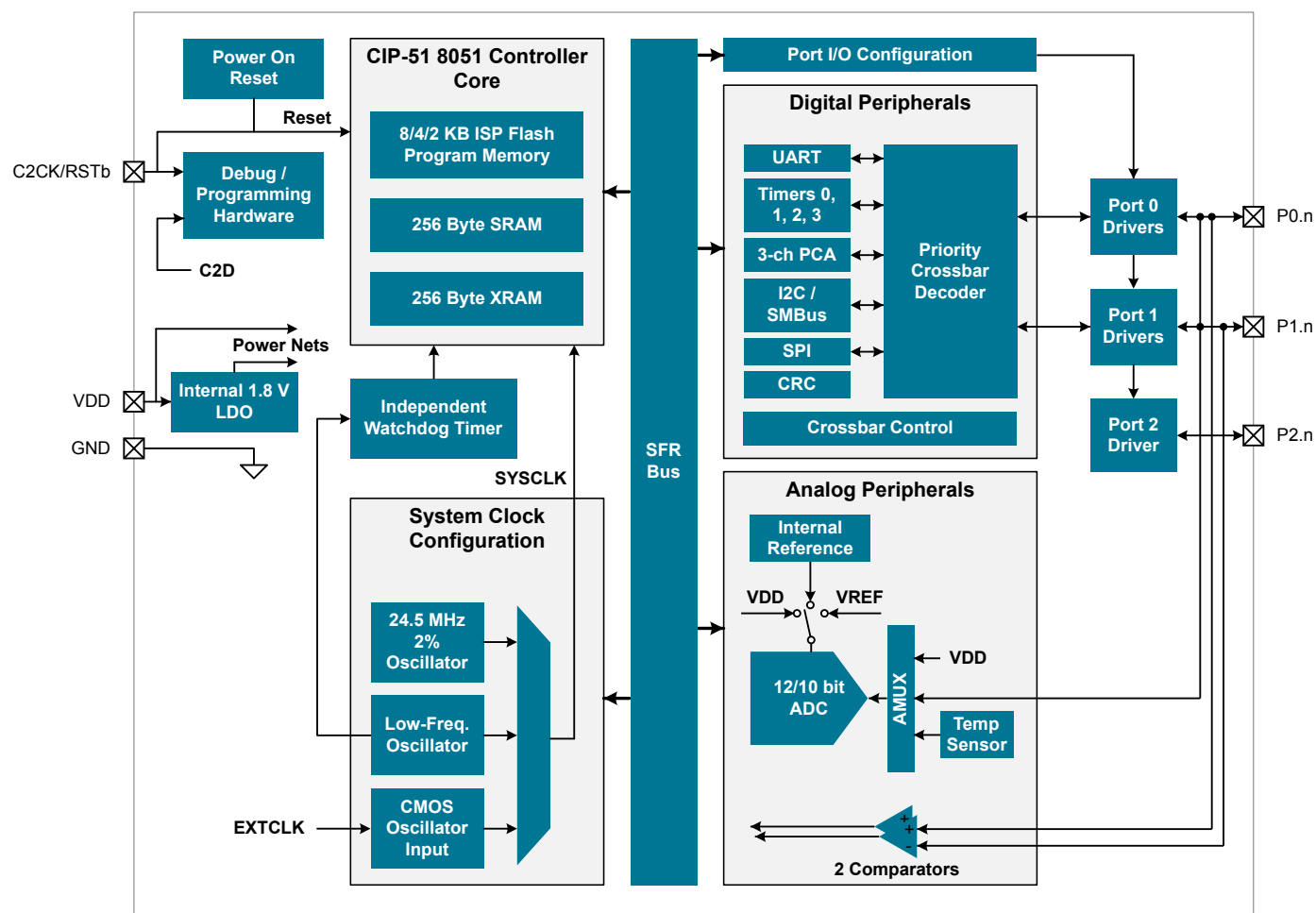


Figure 3.1. Detailed EFM8BB1 Block Diagram

This section describes the EFM8BB1 family at a high level. For more information on each module including register definitions, see the EFM8BB1 Reference Manual.

3.7 Analog

12-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12-, 10-, and 8-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 16 external inputs.
- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 200 ksps samples per second in 12-bit mode or 800 ksps samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer sources.
- Output data window comparator allows automatic range checking.
- Support for burst mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Includes an internal fast-settling reference with two levels (1.65 V and 2.4 V) and support for external reference and signal ground.
- Integrated temperature sensor.

Low Current Comparators (CMP0, CMP1)

Analog comparators are used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator module includes the following features:

- Up to 8 external positive inputs.
- Up to 8 external negative inputs.
- Additional input options:
 - Internal connection to LDO output.
 - Direct connection to GND.
- Synchronous and asynchronous outputs can be routed to pins via crossbar.
- Programmable hysteresis between 0 and ± 20 mV
- Programmable response time.
- Interrupts generated on rising, falling, or both edges.

3.10 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in the code security page, which is the last last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [Application Notes] tile.

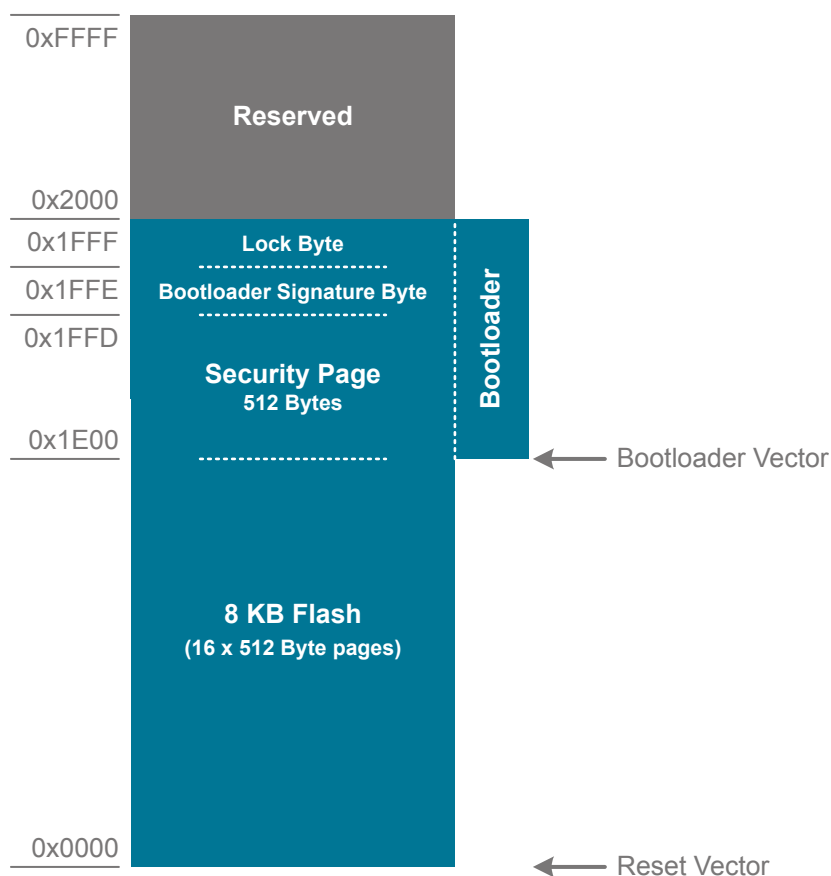


Figure 3.2. Flash Memory Map with Bootloader—8 KB Devices

Table 3.2. Summary of Pins for Bootloader Communication

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5

4.1.2 Power Consumption

Table 4.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current (G-grade devices, -40 °C to +85 °C)						
Normal Mode—Full speed with code executing from flash	I_{DD}	$F_{SYSCLK} = 24.5 \text{ MHz}^2$	—	4.45	4.85	mA
		$F_{SYSCLK} = 1.53 \text{ MHz}^2$	—	915	1150	μA
		$F_{SYSCLK} = 80 \text{ kHz}^3$, $T_A = 25 \text{ }^\circ\text{C}$	—	250	290	μA
		$F_{SYSCLK} = 80 \text{ kHz}^3$	—	250	380	μA
Idle Mode—Core halted with peripherals running	I_{DD}	$F_{SYSCLK} = 24.5 \text{ MHz}^2$	—	2.05	2.3	mA
		$F_{SYSCLK} = 1.53 \text{ MHz}^2$	—	550	700	μA
		$F_{SYSCLK} = 80 \text{ kHz}^3$, $T_A = 25 \text{ }^\circ\text{C}$	—	125	130	μA
		$F_{SYSCLK} = 80 \text{ kHz}^3$	—	125	200	μA
Stop Mode—Core halted and all clocks stopped, Internal LDO On, Supply monitor off.	I_{DD}	$T_A = 25 \text{ }^\circ\text{C}$	—	105	120	μA
		$T_A = -40 \text{ to } +85 \text{ }^\circ\text{C}$	—	105	170	μA
Shutdown Mode—Core halted and all clocks stopped, Internal LDO Off, Supply monitor off.	I_{DD}		—	0.2	—	μA
Digital Core Supply Current (I-grade or A-grade devices, -40 °C to +125 °C)						
Normal Mode—Full speed with code executing from flash	I_{DD}	$F_{SYSCLK} = 24.5 \text{ MHz}^2$	—	4.45	5.25	mA
		$F_{SYSCLK} = 1.53 \text{ MHz}^2$	—	915	1600	μA
		$F_{SYSCLK} = 80 \text{ kHz}^3$, $T_A = 25 \text{ }^\circ\text{C}$	—	250	290	μA
		$F_{SYSCLK} = 80 \text{ kHz}^3$	—	250	725	μA
Idle Mode—Core halted with peripherals running	I_{DD}	$F_{SYSCLK} = 24.5 \text{ MHz}^2$	—	2.05	2.6	mA
		$F_{SYSCLK} = 1.53 \text{ MHz}^2$	—	550	1000	μA
		$F_{SYSCLK} = 80 \text{ kHz}^3$, $T_A = 25 \text{ }^\circ\text{C}$	—	125	130	μA
		$F_{SYSCLK} = 80 \text{ kHz}^3$	—	125	550	μA
Stop Mode—Core halted and all clocks stopped, Internal LDO On, Supply monitor off.	I_{DD}	$T_A = 25 \text{ }^\circ\text{C}$	—	105	120	μA
		$T_A = -40 \text{ to } +125 \text{ }^\circ\text{C}$	—	105	270	μA
Shutdown Mode—Core halted and all clocks stopped, Internal LDO Off, Supply monitor off.	I_{DD}		—	0.2	—	μA
Analog Peripheral Supply Currents (-40 °C to +125 °C)						
High-Frequency Oscillator	I_{HFOSC}	Operating at 24.5 MHz, $T_A = 25 \text{ }^\circ\text{C}$	—	155	—	μA
Low-Frequency Oscillator	I_{LFOSC}	Operating at 80 kHz, $T_A = 25 \text{ }^\circ\text{C}$	—	3.5	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative Hysteresis Mode 3 (CPMD = 11)	HYS _{CP-}	CPHYN = 00	—	-1.5	—	mV
		CPHYN = 01	—	-4	—	mV
		CPHYN = 10	—	-8	—	mV
		CPHYN = 11	—	-16	—	mV
Input Range (CP+ or CP-)	V _{IN}		-0.25	—	V _{DD} +0.25	V
Input Pin Capacitance	C _{CP}		—	7.5	—	pF
Common-Mode Rejection Ratio	CMRR _{CP}		—	70	—	dB
Power Supply Rejection Ratio	PSRR _{CP}		—	72	—	dB
Input Offset Voltage	V _{OFF}	T _A = 25 °C	-10	0	10	mV
Input Offset Tempco	TC _{OFF}		—	3.5	—	μV/°C

4.1.13 SMBus

Table 4.13. SMBus Peripheral Timing Performance (Master Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Mode (100 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	70 ²	kHz
SMBus Operating Frequency	f_{SMB}		40 ¹	—	70 ²	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		9.4	—	—	μ s
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		4.7	—	—	μ s
Repeated START Condition Setup Time	$t_{SU:STA}$		9.4	—	—	μ s
STOP Condition Setup Time	$t_{SU:STO}$		9.4	—	—	μ s
Data Hold Time	$t_{HD:DAT}$		489 ³	—	—	ns
Data Setup Time	$t_{SU:DAT}$		448 ³	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		4.7	—	—	μ s
Clock High Period	t_{HIGH}		9.4	—	50 ⁴	μ s
Fast Mode (400 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	255 ²	kHz
SMBus Operating Frequency	f_{SMB}		40 ¹	—	255 ²	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		2.6	—	—	μ s
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		1.3	—	—	μ s
Repeated START Condition Setup Time	$t_{SU:STA}$		2.6	—	—	μ s
STOP Condition Setup Time	$t_{SU:STO}$		2.6	—	—	μ s
Data Hold Time	$t_{HD:DAT}$		489 ³	—	—	ns
Data Setup Time	$t_{SU:DAT}$		448 ³	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		1.3	—	—	μ s
Clock High Period	t_{HIGH}		2.6	—	50 ⁴	μ s

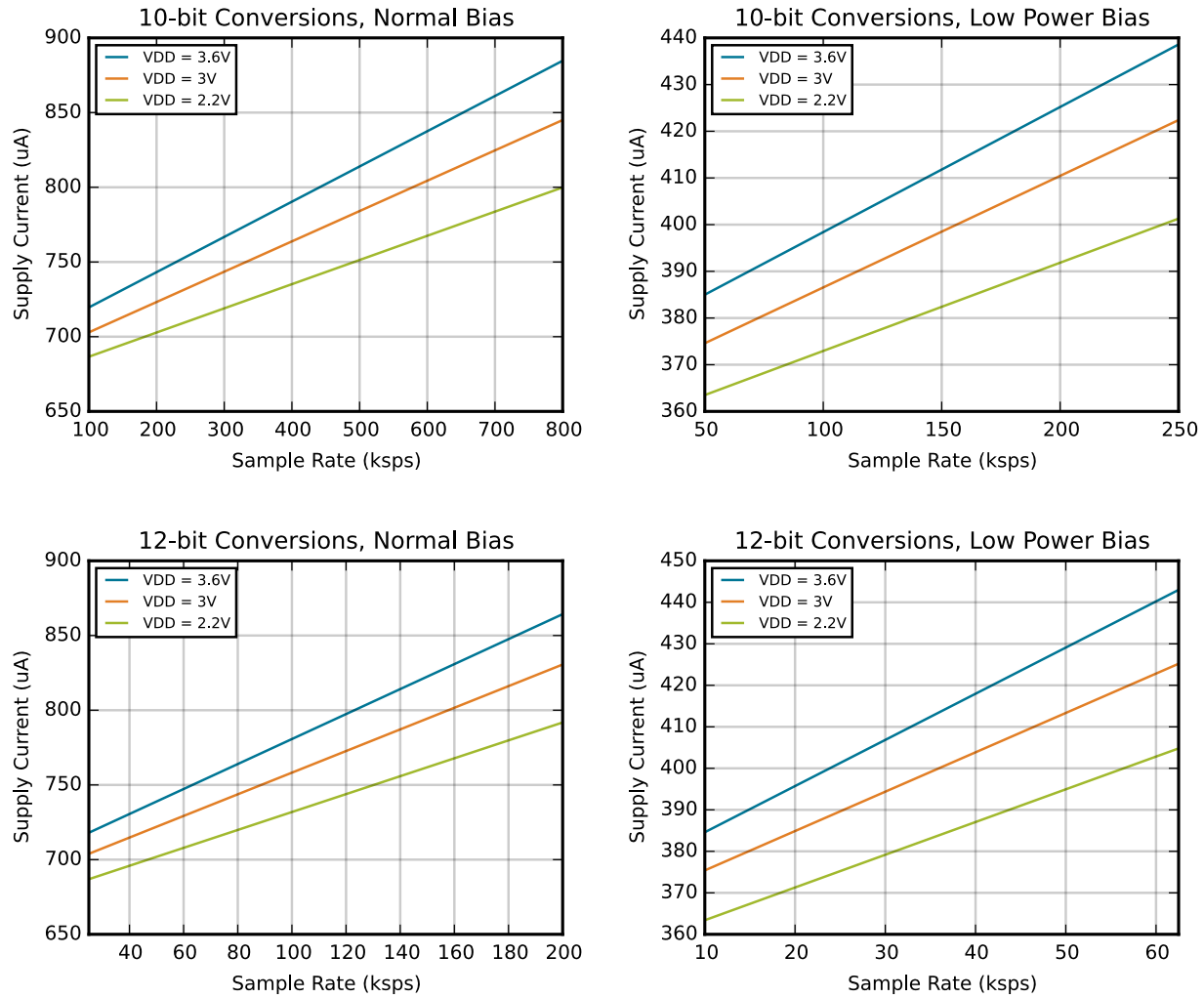


Figure 4.5. Typical ADC0 Supply Current in Normal (always-on) Mode

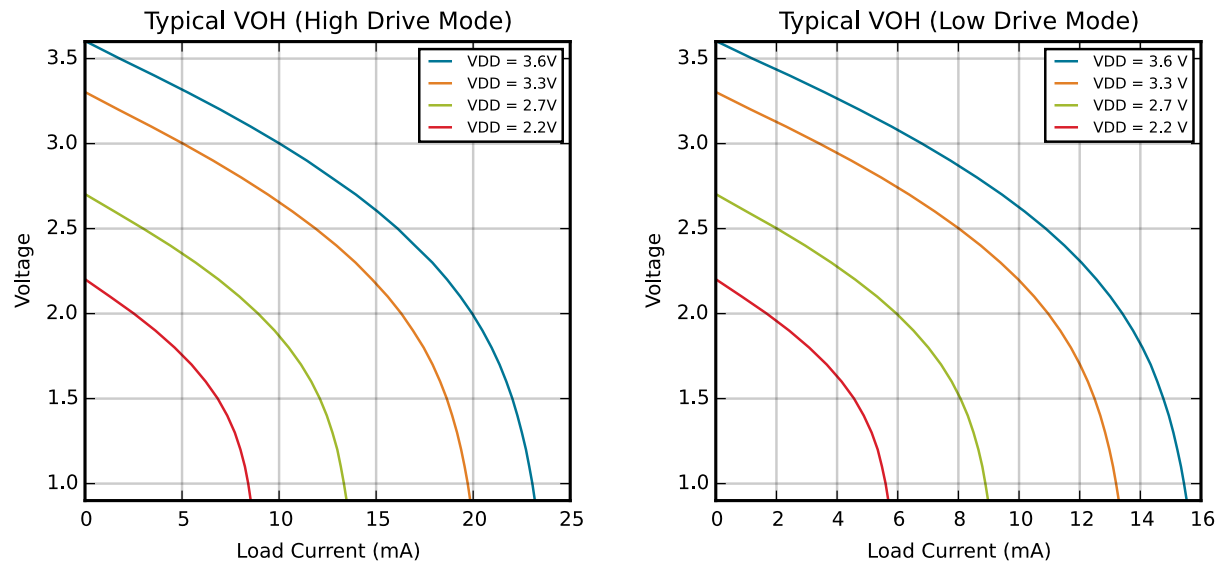


Figure 4.6. Typical V_{OH} Curves

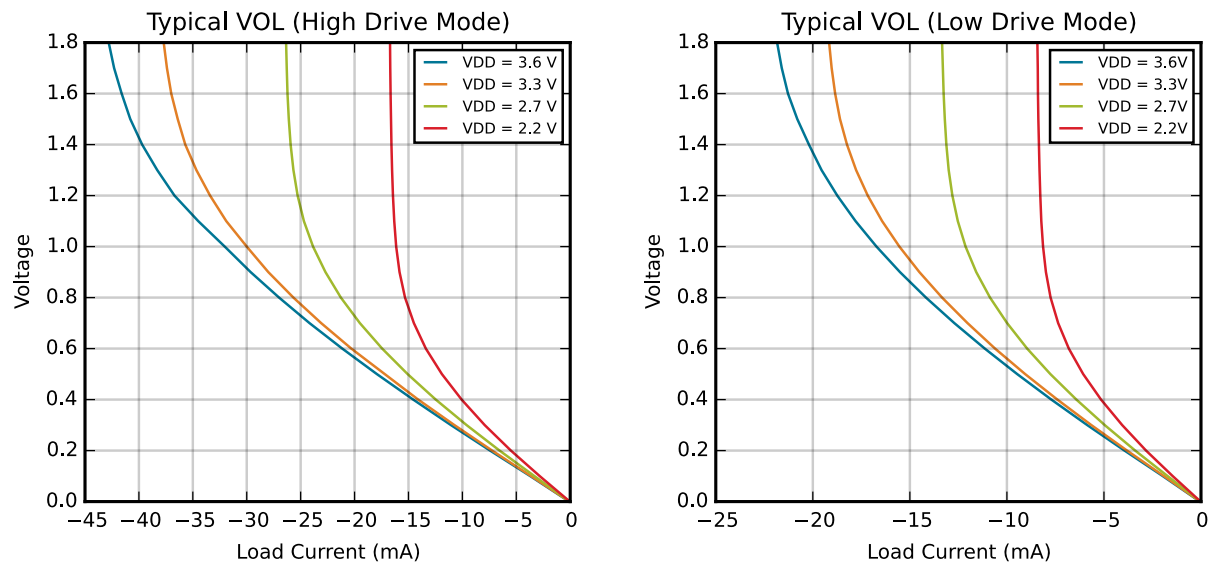


Figure 4.7. Typical V_{OL} Curves

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Power Connection Diagram on page 31 shows a typical connection diagram for the power pins of the EFM8BB1 devices.

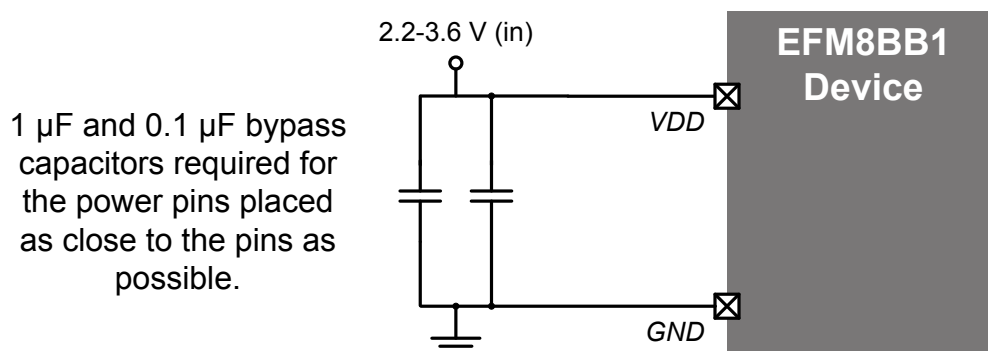


Figure 5.1. Power Connection Diagram

5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in application note, "AN127: Pin Sharing Techniques for the C2 Interface." Application notes can be found on the Silicon Labs website (<http://www.silabs.com/8bit-app-notes>) or in Simplicity Studio.

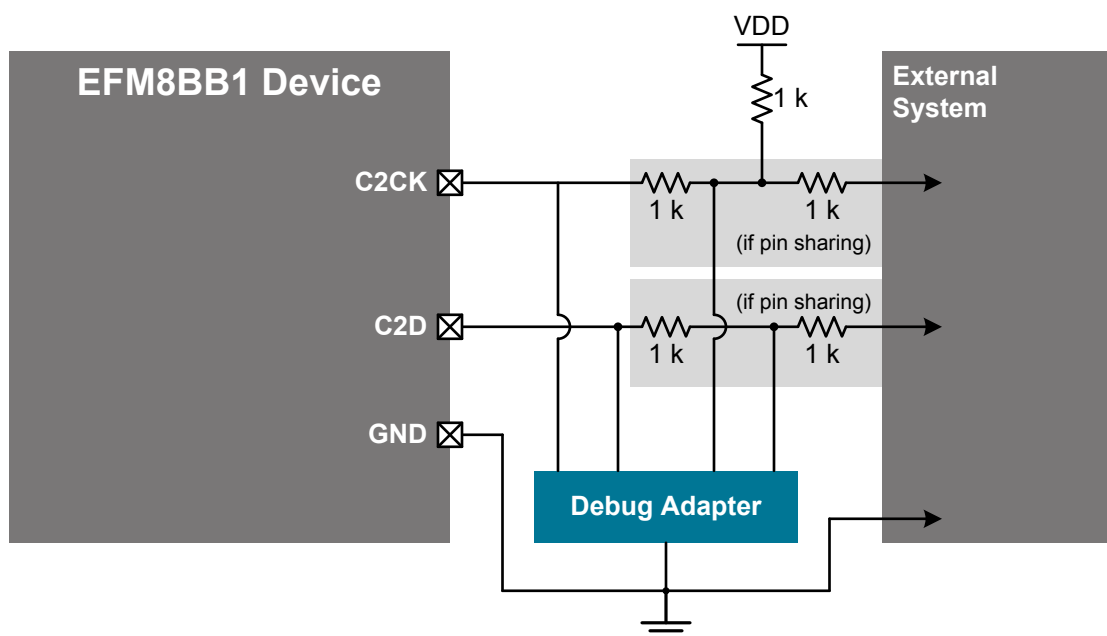


Figure 5.2. Debug Connection Diagram

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application note, "AN203: 8-bit MCU Printed Circuit Board Design Notes", contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/8bit-appnotes).

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
3	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1 AGND
4	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF
5	GND	Ground			
6	VDD	Supply Power Input			
7	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
8	P2.0 / C2D	Multifunction I/O / C2 Debug Data			
9	P1.7	Multifunction I/O	Yes	P1MAT.7	ADC0.15 CMP1P.7 CMP1N.7
10	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.14 CMP1P.6 CMP1N.6
11	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.13 CMP1P.5 CMP1N.5
12	P2.1	Multifunction I/O			
13	N/C	No Connection			
14	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP1P.4 CMP1N.4
15	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CMP1P.3 CMP1N.3
16	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CMP1P.2 CMP1N.2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
17	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CMP1P.1 CMP1N.1
18	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CMP1P.0 CMP1N.0
19	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CMP0P.7 CMP0N.7
20	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.6 CMP0N.6
21	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CMP0P.5 CMP0N.5
22	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CMP0P.4 CMP0N.4
23	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CMP0P.3 CMP0N.3
24	N/C	No Connection			

6.3 EFM8BB1x-SOIC16 Pin Definitions

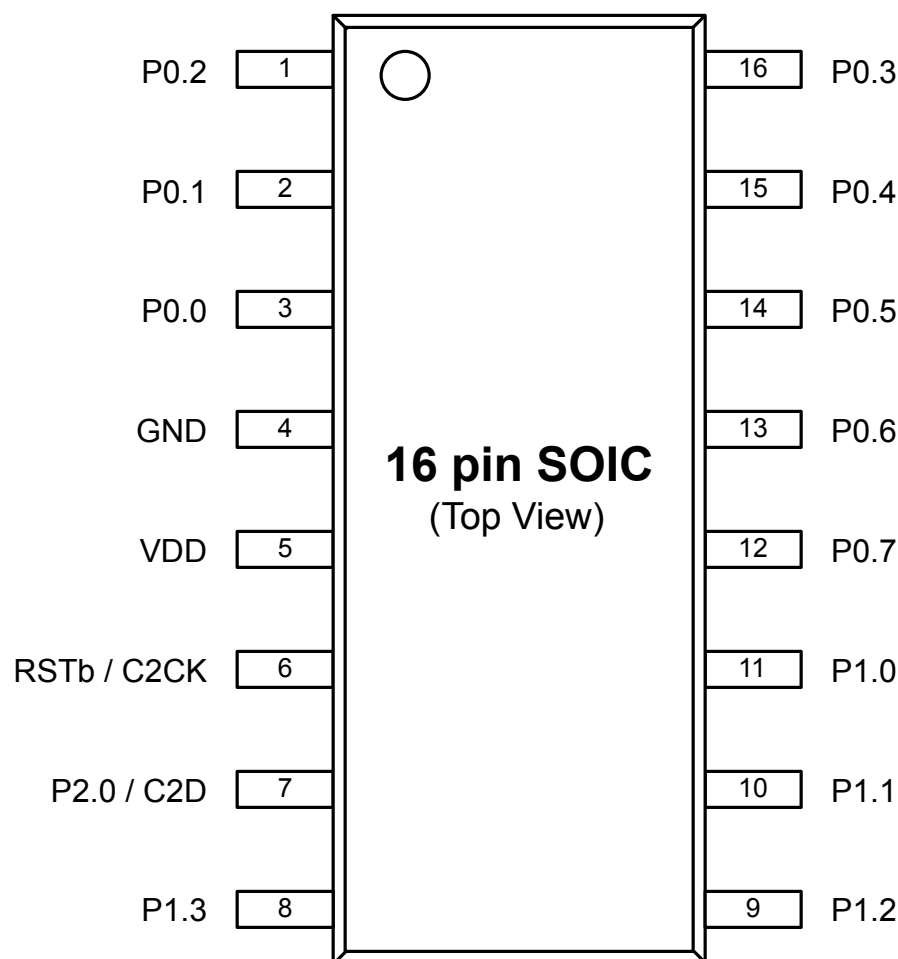


Figure 6.3. EFM8BB1x-SOIC16 Pinout

Table 6.3. Pin Definitions for EFM8BB1x-SOIC16

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.2 CMP0N.2
2	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1
3	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0

Dimension	Min	Typ	Max
aaa		0.20	
bbb		0.18	
ccc		0.10	
ddd		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-137, variation AE.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Dimension	Min	Typ	Max
E	3.00 BSC		
E2	1.60	1.70	1.80
f	2.50 BSC		
L	0.30	0.40	0.50
K	0.25 REF		
R	0.09	0.125	0.15
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. The drawing complies with JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 QFN20 PCB Land Pattern

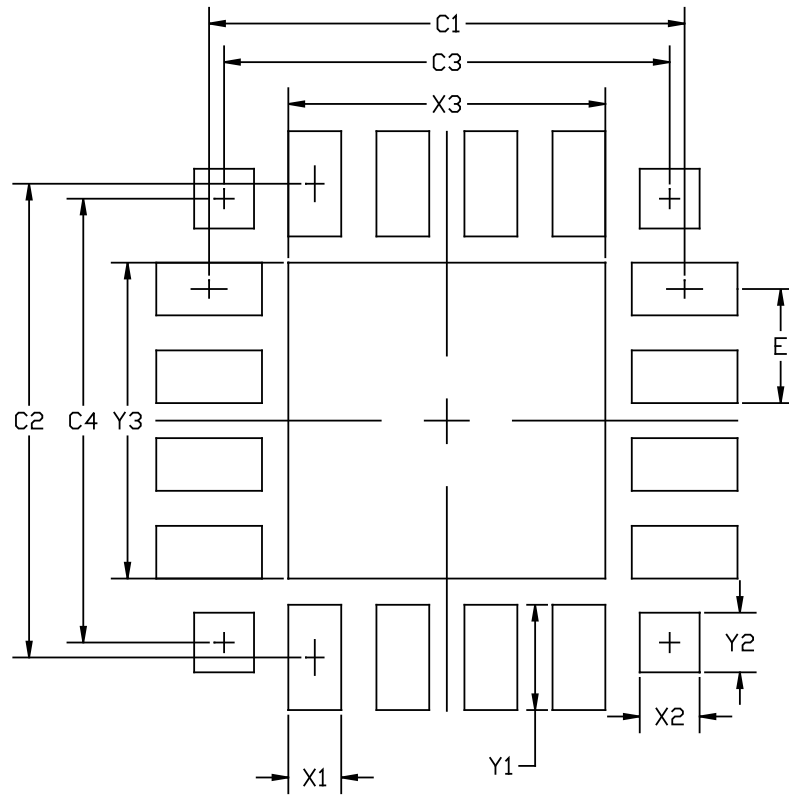


Figure 8.2. QFN20 PCB Land Pattern Drawing

Table 8.2. QFN20 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	3.10	
C2	3.10	
C3	2.50	
C4	2.50	
E	0.50	
X1	0.30	
X2	0.25	0.35
X3	1.80	
Y1	0.90	
Y2	0.25	0.35
Y3	1.80	

9. SOIC16 Package Specifications

9.1 SOIC16 Package Dimensions

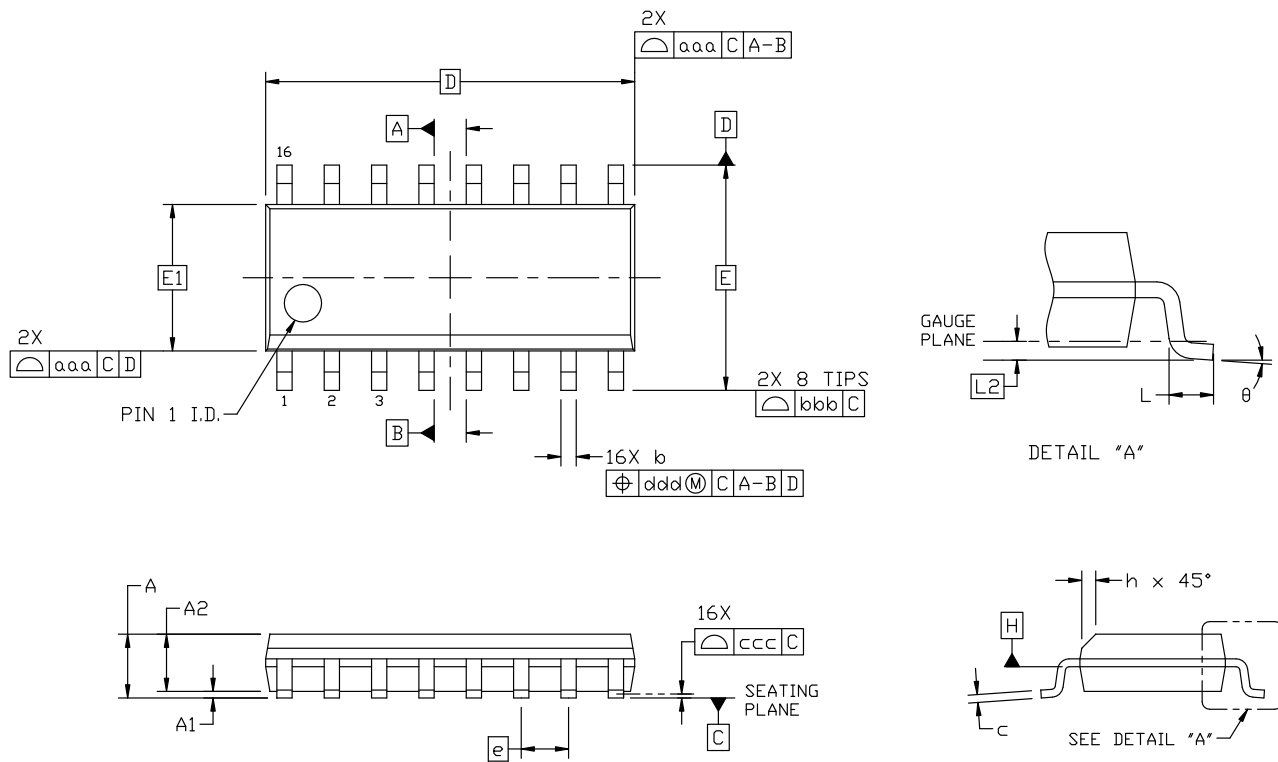


Figure 9.1. SOIC16 Package Drawing

Table 9.1. SOIC16 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.75
A1	0.10	—	0.25
A2	1.25	—	—
b	0.31	—	0.51
c	0.17	—	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	—	1.27
L2	0.25 BSC		

9.2 SOIC16 PCB Land Pattern

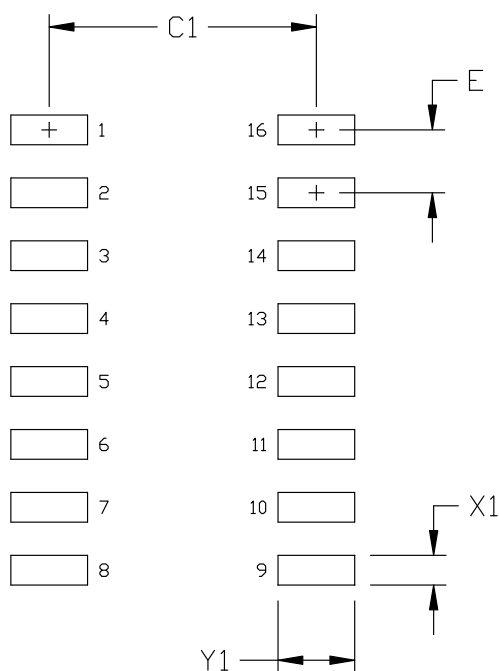


Figure 9.2. SOIC16 PCB Land Pattern Drawing

Table 9.2. SOIC16 PCB Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
3. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

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