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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6246tcssx

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5 Product overview

This section describes the family features that are implemented in the products covered by this datasheet.

For more detailed information on each feature please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).

5.1 STM8A central processing unit (CPU)

The 8-bit STM8A core is a modern CISC core and has been designed for code efficiency and performance. It contains 21 internal registers (six directly addressable in each execution context), 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

5.1.1 Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus with single cycle fetching for most instructions
- X and Y 16-bit index registers, enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter with 16-Mbyte linear memory space
- 16-bit stack pointer with access to a 64 Kbyte stack
- 8-bit condition code register with seven condition flags for the result of the last instruction.

5.1.2 Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for efficient implementation of local variables and parameter passing

5.1.3 Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

UART mode

- Full duplex, asynchronous communications - NRZ standard format (mark/space)
- High-precision baud rate generator
 - A common programmable transmit and receive baud rates up to $f_{\text{MASTER}}/16$
- Programmable data word length (8 or 9 bits) – 1 or 2 stop bits – parity control
- Separate enable bits for transmitter and receiver
- Error detection flags
- Reduced power consumption mode
- Multi-processor communication - enter mute mode if address match does not occur
- Wakeup from mute mode (by idle line detection or address mark detection)
- Two receiver wakeup modes:
 - Address bit (MSB)
 - Idle line

5.10 Input/output specifications

The product features four different I/O types:

- Standard I/O 2 MHz
- Fast I/O up to 10 MHz
- High sink 8 mA, 2 MHz
- True open drain (I²C interface)

To decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os.

The analog inputs are equipped with a low leakage analog switch. Additionally, the schmitt-trigger input stage on the analog I/Os can be disabled in order to reduce the device standby consumption.

STM8A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 μ A. Thanks to this feature, external protection diodes against current injection are no longer required.

7 Memory and register map

7.1 Memory map

Figure 5. Register and memory map of STM8A products

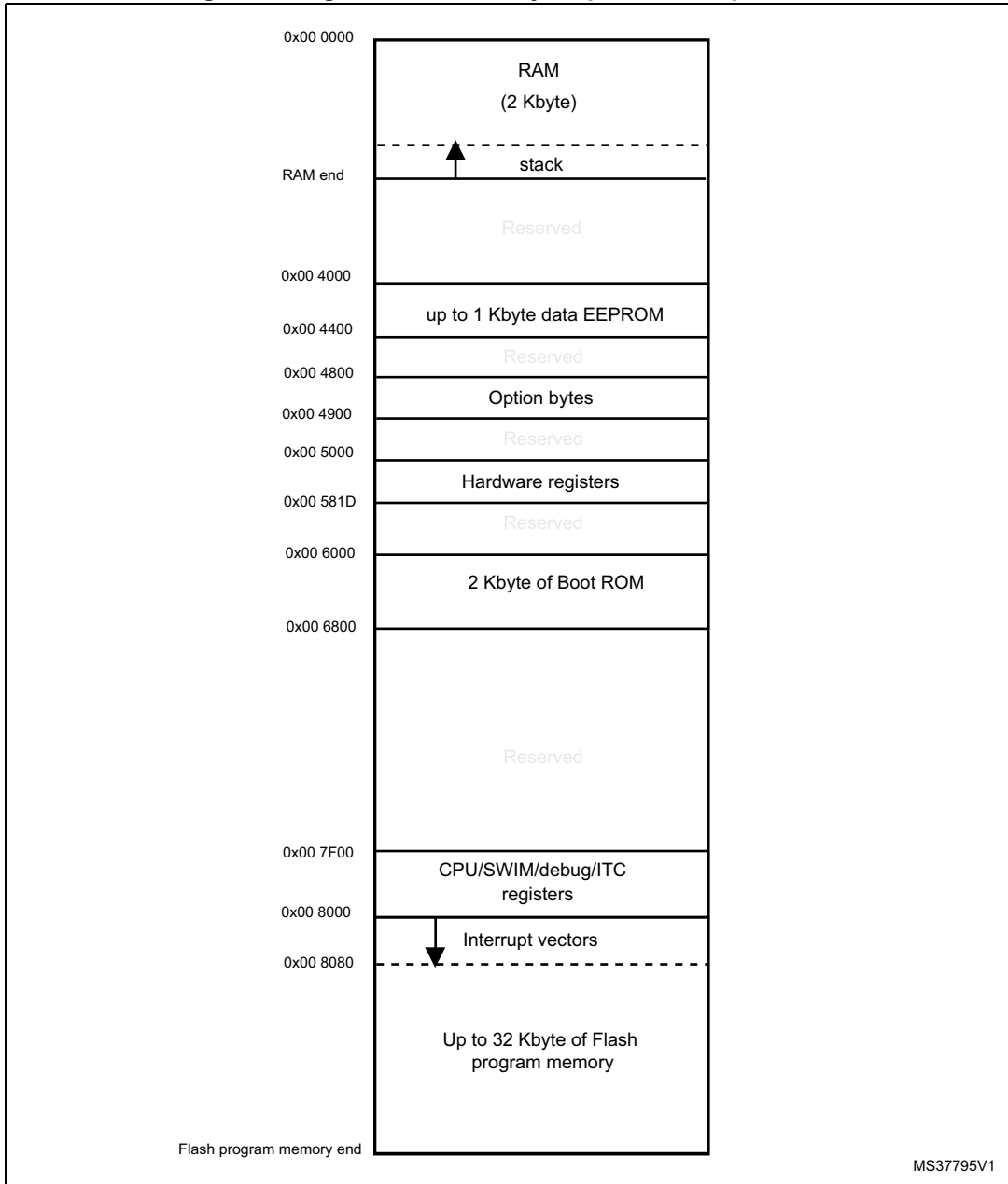


Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50A0	ITC	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2 to 0x00 50B2	Reserved area (17 bytes)			
0x00 50B3	RST	RST_SR	Reset status register	0xXX ⁽¹⁾
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_ICKR	Internal clock control register	0x01
0x00 50C1		CLK_ECKR	External clock control register	0x00
0x00 50C2	Reserved area (1 byte)			
0x00 50C3	CLK	CLK_CMSR	Clock master status register	0xE1
0x00 50C4		CLK_SWR	Clock master switch register	0xE1
0x00 50C5		CLK_SWCR	Clock switch control register	0xXX
0x00 50C6		CLK_CKDIVR	Clock divider register	0x18
0x00 50C7		CLK_PCKENR1	Peripheral clock gating register 1	0xFF
0x00 50C8		CLK_CSSR	Clock security system register	0x00
0x00 50C9		CLK_CCOR	Configurable clock control register	0x00
0x00 50CA		CLK_PCKENR2	Peripheral clock gating register 2	0xFF
0x00 50CB		Reserved area (1 byte)		
0x00 50CC	CLK	CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CD		CLK_SWIMCCR	SWIM clock control register	0bXXXX XXX0
0x00 50CE to 0x00 50D0	Reserved area (3 bytes)			
0x00 50D1	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D2		WWDG_WR	WWDG window register	0x7F
0x00 50D3 to 0x00 50DF	Reserved area (13 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX ⁽²⁾
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	AWU	AWU_CSR1	AWU control/status register 1	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00

Table 16. Option byte description

Option byte no.	Description
OPT0	<p>ROP[7:0]: Memory readout protection (ROP) 0xAA: Enable readout protection (write access via SWIM protocol) <i>Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.</i></p>
OPT1	<p>UBC[5:0]: User boot code area 0x00: No UBC, no write-protection 0x01: Page 0 to 1 defined as UBC, memory write-protected 0x02: Page 0 to 3 defined as UBC, memory write-protected 0x03 to 0x3F: Pages 4 to 63 defined as UBC, memory write-protected <i>Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM write protection for more details.</i></p>
OPT2	<p>AFR7: Alternate function remapping option 7 0: Port D4 alternate function = TIM2_CH1 1: Port D4 alternate function = BEEP</p> <p>AFR6: Alternate function remapping option 6 0: Port B5 alternate function = AIN5, port B4 alternate function = AIN4 1: Port B5 alternate function = I²C_SDA, port B4 alternate function = I²C_SCL.</p> <p>AFR5: Alternate function remapping option 5 0: Port B3 alternate function = AIN3, port B2 alternate function = AIN2, port B1 alternate function = AIN1, port B0 alternate function = AIN0. 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_CH3N, port B1 alternate function = TIM1_CH2N, port B0 alternate function = TIM1_CH1N.</p> <p>AFR4: Alternate function remapping option 4 Reserved, bit must be kept at "0"</p> <p>AFR3: Alternate function remapping option 3 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = TIM1_BKIN</p> <p>AFR2: Alternate function remapping option 2 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = CLK_CCO <i>Note: AFR2 option has priority over AFR3 if both are activated</i></p> <p>AFR1: Alternate function remapping option 1 0: Port A3 alternate function = TIM2_CH3, port D2 alternate function = TIM3_CH1. 1: Port A3 alternate function = TIM3_CH1, port D2 alternate function = TIM2_CH3.</p> <p>AFR0: Alternate function remapping option 0 0: Port D3 alternate function = TIM2_CH2 1: Port D3 alternate function = ADC_ETR</p>

Table 16. Option byte description (continued)

Option byte no.	Description
OPT12	TMU_KEY 5 [7:0]: Temporary unprotection key 4 Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT13	TMU_KEY 6 [7:0]: Temporary unprotection key 5 Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT14	TMU_KEY 7 [7:0]: Temporary unprotection key 6 Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT15	TMU_KEY 8 [7:0]: Temporary unprotection key 7 Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT16	TMU_MAXATT [7:0]: TMU access failure counter TMU_MAXATT can be initialized with the desired value only if TMU is disabled (TMU[3:0]=0101 in OPT6 option byte). When TMU is enabled, any attempt to temporarily remove the readout protection by using wrong key values increments the counter. When the option byte value reaches 0x08, the Flash memory and data EEPROM are erased.
OPT17	BL [7:0]: Bootloader enable If this option byte is set to 0x55 (complementary value 0xAA) the bootloader program is activated also in case of a programmed code memory (for more details, see the bootloader user manual, UM0560).

Table 26. Programming current consumption

Symbol	Parameter	Conditions	Typ	Max	Unit
$I_{DD(Prog)}$	Programming current	$V_{DD} = 5\text{ V}$, $-40\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$, erasing and programming data or Flash program memory	1.0	1.7	mA

Table 27. Typical peripheral current consumption $V_{DD} = 5.0\text{ V}^{(1)}$

Symbol	Parameter	Typ. $f_{master} = 2\text{ MHz}$	Typ. $f_{master} = 16\text{ MHz}$	Unit
$I_{DD(TIM1)}$	TIM1 supply current ⁽²⁾	0.03	0.23	mA
$I_{DD(TIM2)}$	TIM2 supply current ⁽²⁾	0.02	0.12	
$I_{DD(TIM3)}$	TIM3 supply current ⁽²⁾	0.01	0.1	
$I_{DD(TIM4)}$	TIM4 supply current ⁽²⁾	0.004	0.03	
$I_{DD(LINUART)}$	LINUART supply current ⁽²⁾	0.03	0.11	
$I_{DD(SPI)}$	SPI supply current ⁽²⁾	0.01	0.04	
$I_{DD(I^2C)}$	I ² C supply current ⁽²⁾	0.02	0.06	
$I_{DD(AWU)}$	AWU supply current ⁽²⁾	0.003	0.02	
$I_{DD(TOT_DIG)}$	All digital peripherals on	0.22	1	
$I_{DD(ADC)}$	ADC supply current when converting ⁽³⁾	0.93	0.95	

1. Typical values not tested in production. Since the peripherals are powered by an internally regulated, constant digital supply voltage, the values are similar in the full supply voltage range.
2. Data based on a differential I_{DD} measurement between no peripheral clocked and a single active peripheral. This measurement does not include the pad toggling consumption.
3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

Current consumption curves

Figure 10 to Figure 15 show typical current consumption measured with code executing in RAM.

Figure 10. Typ. $I_{DD(RUN)HSE}$ vs. V_{DD} @ $f_{CPU} = 16\text{ MHz}$, peripheral = on

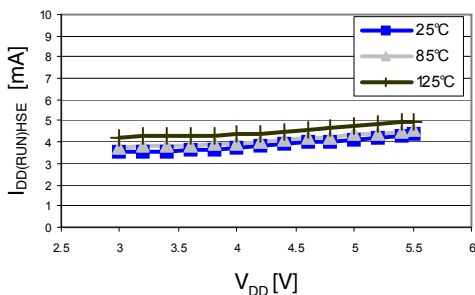


Figure 11. Typ. $I_{DD(RUN)HSE}$ vs. f_{CPU} @ $V_{DD} = 5.0\text{ V}$, peripheral = on

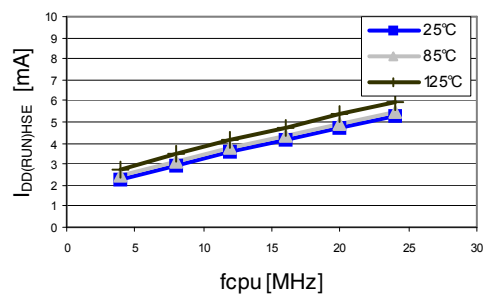
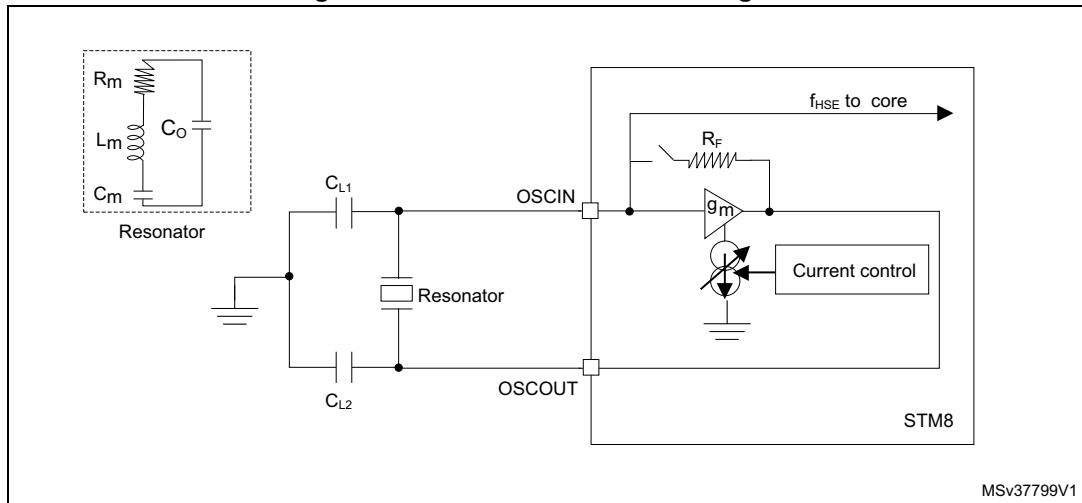


Figure 17. HSE oscillator circuit diagram



HSE oscillator critical gm formula

The crystal characteristics have to be checked with the following formula:

$$g_m \gg g_{m\text{crit}}$$

where $g_{m\text{crit}}$ can be calculated with the crystal parameters as follows:

$$g_{m\text{crit}} = (2 \times \pi \times f_{\text{HSE}})^2 \times R_m(2C_o + C)^2$$

- R_m : Notional resistance (see crystal specification)
- L_m : Notional inductance (see crystal specification)
- C_m : Notional capacitance (see crystal specification)
- C_o : Shunt capacitance (see crystal specification)
- $C_{L1} = C_{L2} = C$: Grounded external capacitance

10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A .

High speed internal RC oscillator (HSI)

Table 30. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz

10.3.8 TIM 1, 2, 3, and 4 timer specifications

Subject to general operating conditions for V_{DD} , f_{MASTER} , and T_A unless otherwise specified.

Table 37. TIM 1, 2, 3, and 4 electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{EXT}	Timer external clock frequency ⁽¹⁾	-	-	-	16	MHz

1. Not tested in production. On 64 Kbyte devices, the frequency is limited to 16 MHz.

10.3.9 SPI serial peripheral interface

Unless otherwise specified, the parameters given in [Table 38](#) are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

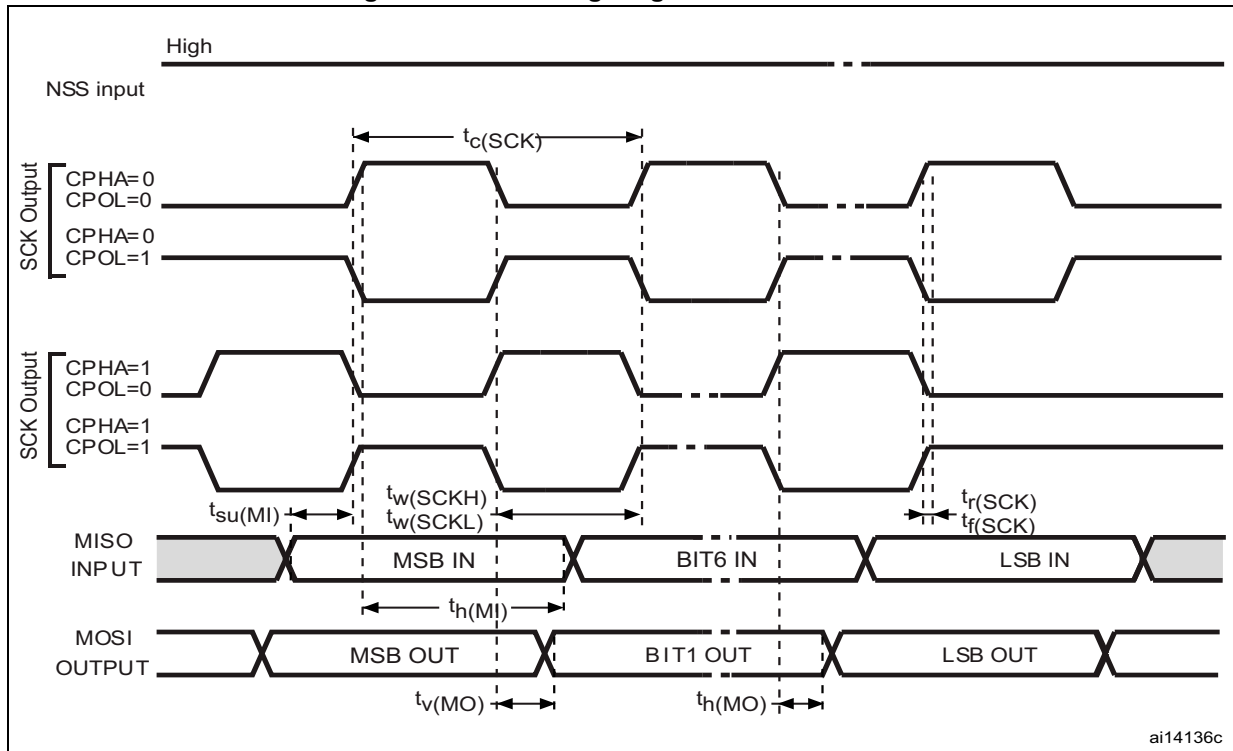
Table 38. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit	
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	10	MHz	
		Slave mode	$V_{DD} < 4.5 V$	0		6 ⁽¹⁾
			$V_{DD} = 4.5 V$ to 5.5 V	0		8 ⁽¹⁾
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	25 ⁽²⁾	ns	
$t_{su(NSS)}^{(3)}$	NSS setup time	Slave mode	$4 * t_{MASTER}$	-		
$t_{h(NSS)}^{(3)}$	NSS hold time	Slave mode	70	-		
$t_{w(SCKH)}^{(3)}$ $t_{w(SCKL)}^{(3)}$	SCK high and low time	Master mode	$t_{SCK}/2 - 15$	$t_{SCK}/2 + 15$		
$t_{su(MI)}^{(3)}$ $t_{su(SI)}^{(3)}$	Data input setup time	Master mode	5	-		
		Slave mode	5	-		
$t_{h(MI)}^{(3)}$ $t_{h(SI)}^{(3)}$	Data input hold time	Master mode	7	-		
		Slave mode	10	-		
$t_{a(SO)}^{(3)(4)}$	Data output access time	Slave mode	-	$3 * t_{MASTER}$		
$t_{dis(SO)}^{(3)(5)}$	Data output disable time	Slave mode	25	-		
$t_{v(SO)}^{(3)}$	Data output valid time	Slave mode (after enable edge)	$V_{DD} < 4.5 V$	-		75
		$V_{DD} = 4.5 V$ to 5.5 V	-	53		
$t_{v(MO)}^{(3)}$	Data output valid time	Master mode (after enable edge)	-	30		
$t_{h(SO)}^{(3)}$ $t_{h(MO)}^{(3)}$	Data output hold time	Slave mode (after enable edge)	31	-		
		Master mode (after enable edge)	12	-		

1. $f_{SCK} < f_{MASTER}/2$.

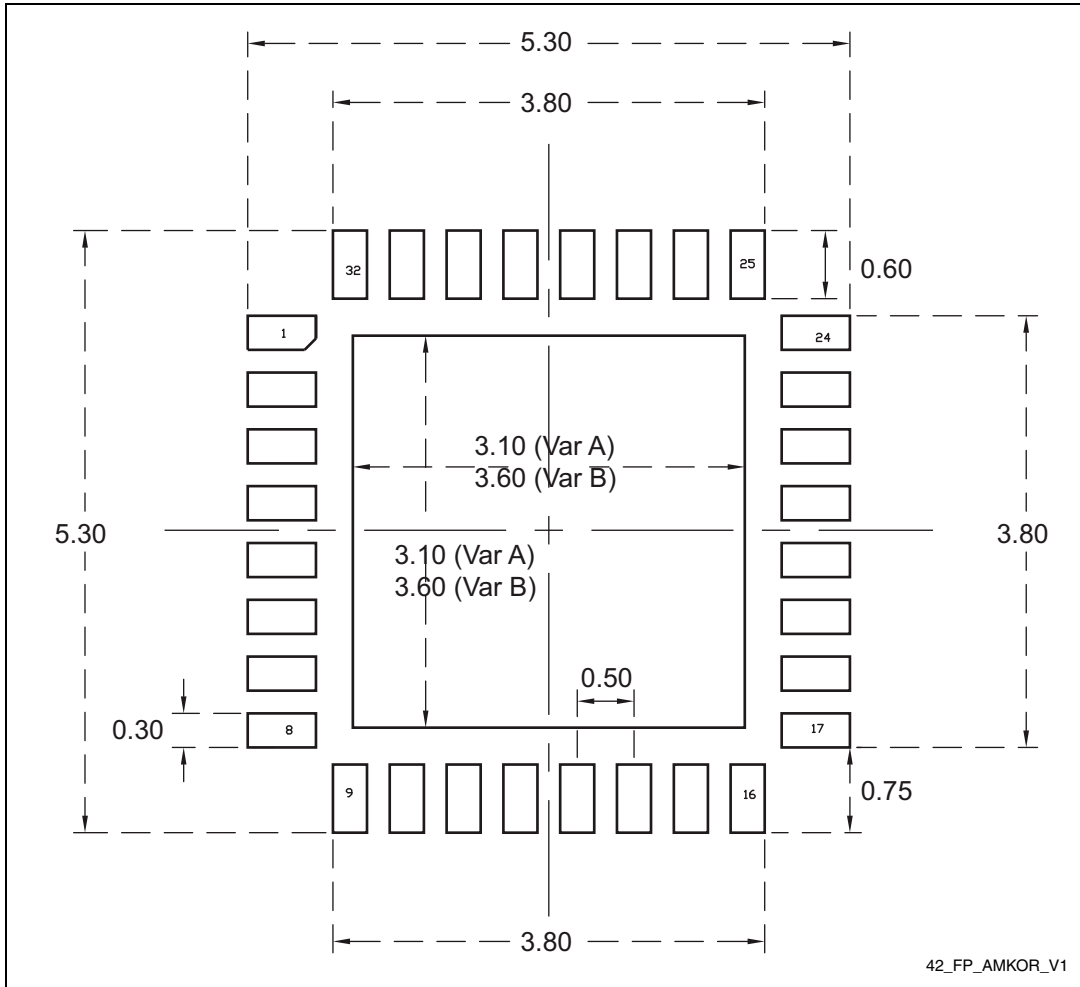
2. The pad has to be configured accordingly (fast mode).

Figure 39. SPI timing diagram - master mode



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD} .

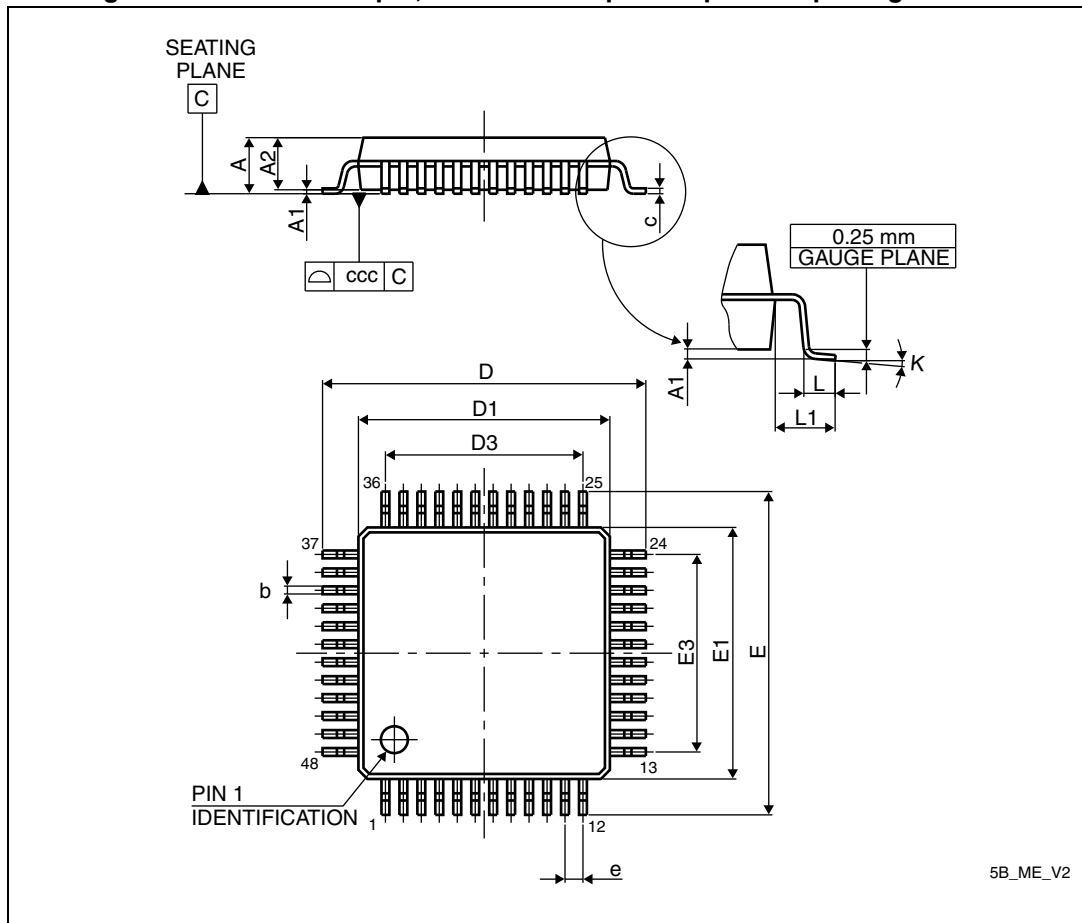
Figure 43. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

11.2 LQFP48 package information

Figure 45. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

**Table 47. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package
mechanical data**

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

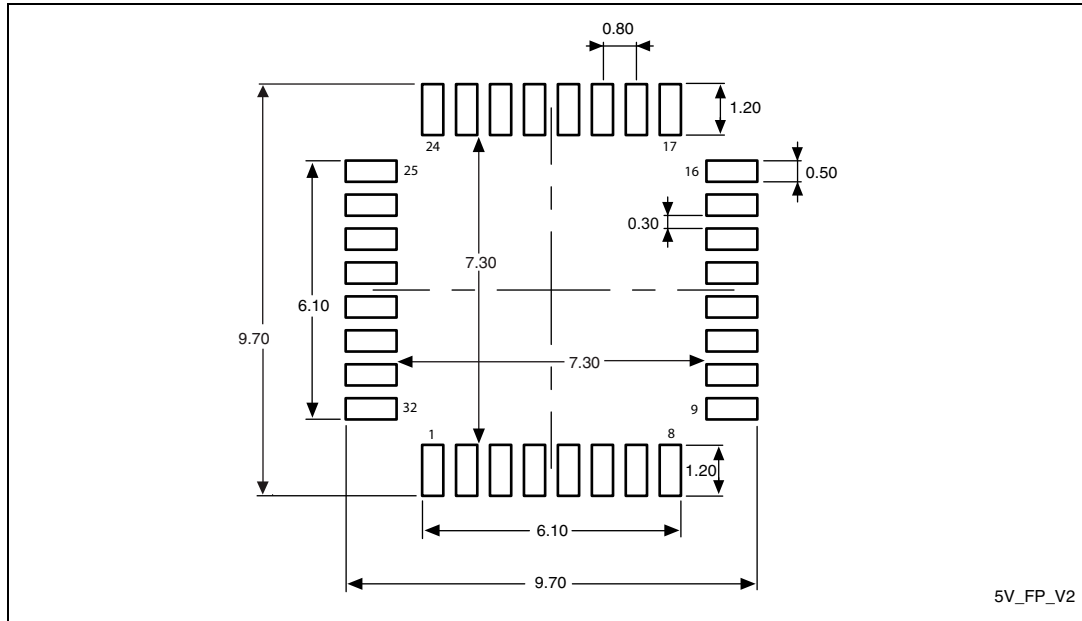
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 48. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 49. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint

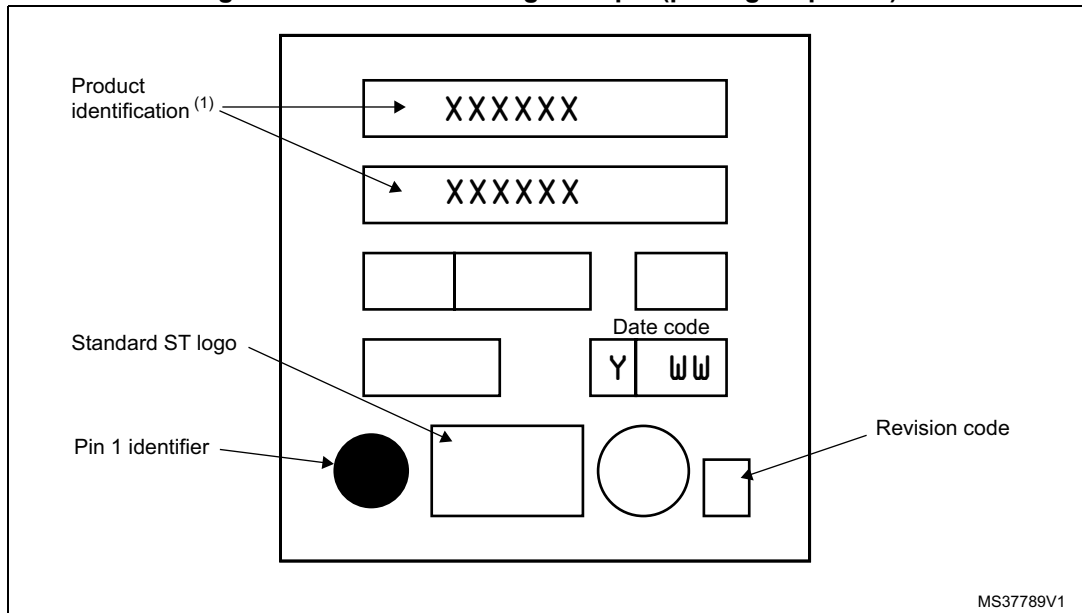


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 50. LQFP32 marking example (package top view)



11.4 Thermal characteristics

In case the maximum chip junction temperature (T_{Jmax}) specified in [Table 21: General operating conditions on page 52](#) is exceeded, the functionality of the device cannot be guaranteed.

T_{Jmax} , in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins

Where:

$$P_{I/Omax} = \Sigma (V_{OL} * I_{OL}) + \Sigma ((V_{DD} - V_{OH}) * I_{OH}),$$

taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 49. Thermal characteristics⁽¹⁾

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm	57	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	59	°C/W
Θ_{JA}	Thermal resistance junction-ambient VFQFPN32	25	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

11.4.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

11.4.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see [Section 12: Ordering information](#)).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 82\text{ }^{\circ}\text{C}$ (measured according to JESD51-2),
 $I_{DDmax} = 14\text{ mA}$, $V_{DD} = 5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 14\text{ mA} \times 5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

This gives: $P_{INTmax} = 70\text{ mW}$ and $P_{IOmax} = 64\text{ mW}$:

$$P_{Dmax} = 70\text{ mW} + 64\text{ mW}$$

Thus: $P_{Dmax} = 134\text{ mW}$.

Using the values obtained in [Table 49: Thermal characteristics](#) T_{Jmax} is calculated as follows:

For LQFP64 $46\text{ }^{\circ}\text{C/W}$

$$T_{Jmax} = 82\text{ }^{\circ}\text{C} + (46\text{ }^{\circ}\text{C/W} \times 134\text{ mW}) = 82\text{ }^{\circ}\text{C} + 6\text{ }^{\circ}\text{C} = 88\text{ }^{\circ}\text{C}$$

This is within the range of the suffix C version parts ($-40 < T_J < 125\text{ }^{\circ}\text{C}$).

Parts must be ordered at least with the temperature range suffix C.

Table 50. Document revision history (continued)

Date	Revision	Changes
09-Jun-2015	10	<p>Updated:</p> <ul style="list-style-type: none"> – the product naming in the document headers and captions, – LIN version in <i>Features</i> and <i>Section 5.9.3: Universal asynchronous receiver/transmitter with LIN support (LINUART)</i>. <p>Added:</p> <ul style="list-style-type: none"> – the third table footnote to <i>Table 22: Operating conditions at power-up/power-down</i>, – <i>Figure 44: VFQFPN32 marking example (package top view)</i>, – <i>Figure 47: LQFP48 marking example (package top view)</i>, – <i>Figure 50: LQFP32 marking example (package top view)</i>, – the note about the parts marked “E” and “ES” below <i>Figure 51: STM8AF6246/48/66/68 ordering information scheme(1) (2)</i>, – the standard for EMI characteristics in <i>Table 43: EMI data</i>. <p>Removed the references to STM8AF61xx and STM8AH61xx obsolete products.</p> <p>Moved <i>Section 11.4: Thermal characteristics</i> to <i>Section 11: Package information</i>.</p>
14-Jun-2016	11	Update <i>Table 46: VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data</i>

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