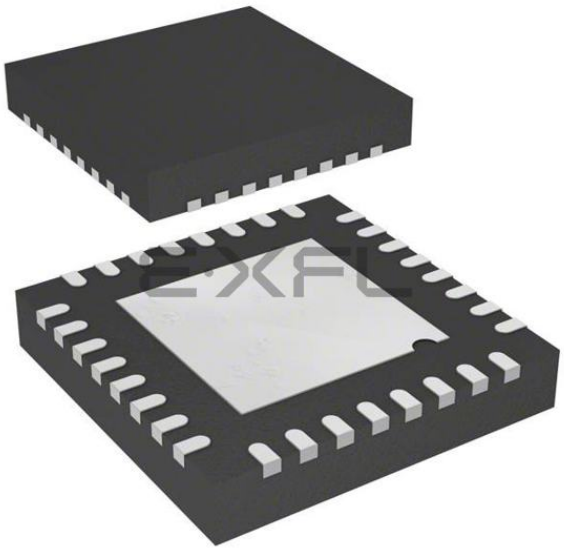

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6246uay

5.4.4 Read-out protection (ROP)

The STM8A provides a read-out protection of the code and data memory which can be activated by an option byte setting (see the ROP option byte in section 10).

The read-out protection prevents reading and writing Flash program memory, data memory and option bytes via the debug module and SWIM interface. This protection is active in all device operation modes. Any attempt to remove the protection by overwriting the ROP option byte triggers a global erase of the program and data memory.

The ROP circuit may provide a temporary access for debugging or failure analysis. The temporary read access is protected by a user defined, 8-byte keyword stored in the option bytes area. This keyword must be entered via the SWIM interface to temporarily unlock the device.

If desired, the temporary unlock mechanism can be permanently disabled by the user through OPT6/NOPT6 option bytes.

5.5 Clock controller

The clock controller distributes the system clock coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

5.5.1 Features

- **Clock sources**
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
  - 1-16 MHz high-speed external crystal (HSE)
  - Up to 16 MHz high-speed user-external clock (HSE user-ext)
- **Reset**: After reset the microcontroller restarts by default with an internal 2-MHz clock (16 MHz/8). The clock source and speed can be changed by the application program as soon as the code execution starts.
- **Safe clock switching**: Clock sources can be changed safely on the fly in Run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management**: To reduce power consumption, the clock controller can stop the clock to the core or individual peripherals.
- **Wakeup**: In case the device wakes up from low-power modes, the internal RC oscillator (16 MHz/8) is used for quick startup. After a stabilization time, the device switches to the clock source that was selected before Halt mode was entered.
- **Clock security system (CSS)**: The CSS permits monitoring of external clock sources and automatic switching to the internal RC (16 MHz/8) in case of a clock failure.
- **Configurable main clock output (CCO)**: This feature permits to output a clock signal for use by the application.

UART mode

- Full duplex, asynchronous communications - NRZ standard format (mark/space)
- High-precision baud rate generator
  - A common programmable transmit and receive baud rates up to $f_{MASTER}/16$
- Programmable data word length (8 or 9 bits) – 1 or 2 stop bits – parity control
- Separate enable bits for transmitter and receiver
- Error detection flags
- Reduced power consumption mode
- Multi-processor communication - enter mute mode if address match does not occur
- Wakeup from mute mode (by idle line detection or address mark detection)
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line

5.10 Input/output specifications

The product features four different I/O types:

- Standard I/O 2 MHz
- Fast I/O up to 10 MHz
- High sink 8 mA, 2 MHz
- True open drain (I^2C interface)

To decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os.

The analog inputs are equipped with a low leakage analog switch. Additionally, the schmitt-trigger input stage on the analog I/Os can be disabled in order to reduce the device standby consumption.

STM8A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA. Thanks to this feature, external protection diodes against current injection are no longer required.

Table 8. STM8AF6246/48/66/68 (32 Kbyte) microcontroller pin description(1)(2)

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	VFQFPN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
2	2	PA1/OSCIN(3)	I/O	**X**	X	-	-	O1	X	X	**Port A1**	Resonator/crystal in	-
3	3	PA2/OSCOUT	I/O	**X**	X	X	-	O1	X	X	**Port A2**	Resonator/crystal out	-
4	-	V_{SSIO_1}	S	-	-	-	-	-	-	-	I/O ground		-
5	4	V_{SS}	S	-	-	-	-	-	-	-	Digital ground		-
6	5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
7	6	V_{DD}	S	-	-	-	-	-	-	-	Digital power supply		-
8	7	V_{DDIO_1}	S	-	-	-	-	-	-	-	I/O power supply		-
-	8	PF4/AIN12(4)(5)	I/O	**X**	X		-	O1	X	X	**Port F4**	Analog input 12	-
9	-	PA3/TIM2_CH3	I/O	**X**	X	X	-	O1	X	X	**Port A3**	Timer 2 - channel 3	TIM3_CH1 [AFR1]
10	-	PA4	I/O	**X**	X	X	-	O3	X	X	**Port A4**		-
11	-	PA5	I/O	**X**	X	X	-	O3	X	X	**Port A5**		-
12	-	PA6	I/O	**X**	X	X	-	O3	X	X	**Port A6**		-
13	9	V_{DDA}	S	-	-	-	-	-	-	-	Analog power supply		-
14	10	V_{SSA}	S	-	-	-	-	-	-	-	Analog ground		-
15	-	PB7/AIN7	I/O	**X**	X	X	-	O1	X	X	**Port B7**	Analog input 7	-
16	-	PB6/AIN6	I/O	**X**	X	X	-	O1	X	X	**Port B6**	Analog input 6	-
17	11	PB5/AIN5	I/O	**X**	X	X	-	O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
18	12	PB4/AIN4	I/O	**X**	X	X	-	O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]
19	13	PB3/AIN3	I/O	**X**	X	X	-	O1	X	X	**Port B3**	Analog input 3	TIM1_ETR [AFR5]
20	14	PB2/AIN2	I/O	**X**	X	X	-	O1	X	X	**Port B2**	Analog input	TIM1_NCC3 [AFR5]
21	15	PB1/AIN1	I/O	**X**	X	X	-	O1	X	X	**Port B1**	Analog input 1	TIM1_NCC2 [AFR5]
22	16	PB0/AIN0	I/O	**X**	X	X	-	O1	X	X	**Port B0**	Analog input 0	TIM1_NCC1 [AFR5]
23	-	PE7/AIN8	I/O	**X**	X		-	O1	X	X	**Port E7**	Analog input 8	-

Table 8. STM8AF6246/48/66/68 (32 Kbyte) microcontroller pin description(1)(2) (continued)

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	VFQFPN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
47	31	PD6/ LINUART_RX	I/O	**X**	X	X	-	O1	X	X	**Port D6**	LINUART data receive	-
48	32	PD7/TLI(8)	I/O	**X**	X	X	-	O1	X	X	**Port D7**	Top level interrupt	-

1. Refer to *Table 7* for the definition of the abbreviations.
2. Reset state is shown in bold.
3. In Halt/Active-halt mode this pad behaves in the following way:
   - the input/output path is disabled
   - if the HSE clock is used for wakeup, the internal weak pull up is disabled
   - if the HSE clock is off, internal weak pull up setting from corresponding OR bit is used
   By managing the OR bit correctly, it must be ensured that the pad is not left floating during Halt/Active-halt.
4. On this pin, a pull-up resistor as specified in *Table 35*. I/O static characteristics is enabled during the reset phase of the product.
5. AIN12 is not selectable in ADC scan mode or with analog watchdog.
6. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, week pull-up, and protection diode to V_{DD} are not implemented)
7. The PD1 pin is in input pull-up during the reset phase and after reset release.
8. If this pin is configured as interrupt pin, it will trigger the TLI.

6.2 Alternate function remapping

As shown in the rightmost column of *Table 8*, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. Refer to *Section 9: Option bytes on page 44*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016).

Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50A0	ITC	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2 to 0x00 50B2	Reserved area (17 bytes)			
0x00 50B3	RST	RST_SR	Reset status register	0xXX(1)
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_ICKR	Internal clock control register	0x01
0x00 50C1		CLK_ECKR	External clock control register	0x00
0x00 50C2	Reserved area (1 byte)			
0x00 50C3	CLK	CLK_CMSR	Clock master status register	0xE1
0x00 50C4		CLK_SWR	Clock master switch register	0xE1
0x00 50C5		CLK_SWCR	Clock switch control register	0xXX
0x00 50C6		CLK_CKDIVR	Clock divider register	0x18
0x00 50C7		CLK_PCKENR1	Peripheral clock gating register 1	0xFF
0x00 50C8		CLK_CSSR	Clock security system register	0x00
0x00 50C9		CLK_CCOR	Configurable clock control register	0x00
0x00 50CA		CLK_PCKENR2	Peripheral clock gating register 2	0xFF
0x00 50CB	Reserved area (1 byte)			
0x00 50CC	CLK	CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CD		CLK_SWIMCCR	SWIM clock control register	0bXXXX XXX0
0x00 50CE to 0x00 50D0	Reserved area (3 bytes)			
0x00 50D1	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D2		WWDG_WR	WWDR window register	0x7F
0x00 50D3 to 0x00 50DF	Reserved area (13 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX(2)
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	AWU	AWU_CSR1	AWU control/status register 1	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00

Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 50FF	Reserved area (12 bytes)			
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07
0x00 5206		SPI_RXCRCR	SPI Rx CRC register	0xFF
0x00 5207		SPI_TXCRCR	SPI Tx CRC register	0xFF
0x00 5208 to 0x00 520F	Reserved area (8 bytes)			
0x00 5210	I2C	I2C_CR1	I2C control register 1	0x00
0x00 5211		I2C_CR2	I2C control register 2	0x00
0x00 5212		I2C_FREQR	I2C frequency register	0x00
0x00 5213		I2C_OARL	I2C own address register low	0x00
0x00 5214		I2C_OARH	I2C own address register high	0x00
0x00 5215		Reserved area (1 byte)		
0x00 5216		I2C_DR	I2C data register	0x00
0x00 5217		I2C_SR1	I2C status register 1	0x00
0x00 5218		I2C_SR2	I2C status register 2	0x00
0x00 5219		I2C_SR3	I2C status register 3	0x00
0x00 521A		I2C_ITR	I2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I2C clock control register low	0x00
0x00 521C		I2C_CCRH	I2C clock control register high	0x00
0x00 521D		I2C_TRISER	I2C TRISE register	0x02
0x00 521E to 0x00 523F	Reserved area (24 bytes)			

Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5240	LINUART	UART2_SR	LINUART status register	0xC0
0x00 5241		UART2_DR	LINUART data register	0xXX
0x00 5242		UART2_BRR1	LINUART baud rate register 1	0x00
0x00 5243		UART2_BRR2	LINUART baud rate register 2	0x00
0x00 5244		UART2_CR1	LINUART control register 1	0x00
0x00 5245		UART2_CR2	LINUART control register 2	0x00
0x00 5246		UART2_CR3	LINUART control register 3	0x00
0x00 5247		UART2_CR4	LINUART control register 4	0x00
0x00 5248		Reserved		
0x00 5249		UART2_CR6	LINUART control register 6	0x00
0x00 524A to 0x00 524F	Reserved area (6 bytes)			
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00

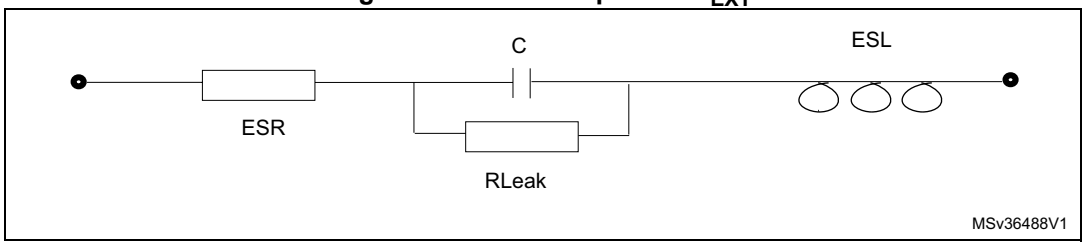
Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5265	TIM1	TIM1_CCR1H	TIM1 capture/compare register 1 high	0x00
0x00 5266		TIM1_CCR1L	TIM1 capture/compare register 1 low	0x00
0x00 5267		TIM1_CCR2H	TIM1 capture/compare register 2 high	0x00
0x00 5268		TIM1_CCR2L	TIM1 capture/compare register 2 low	0x00
0x00 5269		TIM1_CCR3H	TIM1 capture/compare register 3 high	0x00
0x00 526A		TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 bytes)			
0x00 5300	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5301		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5302		TIM2_SR1	TIM2 status register 1	0x00
0x00 5303		TIM2_SR2	TIM2 status register 2	0x00
0x00 5304		TIM2_EGR	TIM2 event generation register	0x00
0x00 5305		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5306		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 5307		TIM2_CCMR3	TIM2 capture/compare mode register 3	0x00
0x00 5308		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 5309		TIM2_CCER2	TIM2 capture/compare enable register 2	0x00
0x00 530A		TIM2_CNTRH	TIM2 counter high	0x00
0x00 530B		TIM2_CNTRL	TIM2 counter low	0x00
00 530C0x		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 530D		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 530E		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 530F		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5310		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5311		TIM2_CCR2H	TIM2 capture/compare reg. 2 high	0x00
0x00 5312		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5313		TIM2_CCR3H	TIM2 capture/compare register 3 high	0x00

10.3.1 VCAP external capacitor

Stabilization for the main regulator is achieved connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 21*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 9. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance and ESL is the equivalent inductance.

10.3.2 Supply current characteristics

The current consumption is measured as described in *Figure 6 on page 49* and *Figure 7 on page 50*.

If not explicitly stated, general conditions of temperature and voltage apply.

Table 23. Total current consumption in Run, Wait and Slow mode. General conditions for V_{DD} apply, T_A = -40 to 150 °C

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$(1)	Supply current in Run mode	All peripherals clocked, code executed from Flash program memory, HSE external clock (without resonator)	f_{CPU} = 16 MHz	7.4	14	mA
			f_{CPU} = 8 MHz	4.0	7.4(2)	
			f_{CPU} = 4 MHz	2.4	4.1(2)	
			f_{CPU} = 2 MHz	1.5	2.5	
$I_{DD(RUN)}$(1)	Supply current in Run mode	All peripherals clocked, code executed from RAM and EEPROM, HSE external clock (without resonator)	f_{CPU} = 16 MHz	3.7	5.0	
			f_{CPU} = 8 MHz	2.2	3.0(2)	
			f_{CPU} = 4 MHz	1.4	2.0(2)	
			f_{CPU} = 2 MHz	1.0	1.5	
$I_{DD(WFI)}$(1)	Supply current in Wait mode	CPU stopped, all peripherals off, HSE external clock	f_{CPU} = 16 MHz	1.65	2.5	
			f_{CPU} = 8 MHz	1.15	1.9(2)	
			f_{CPU} = 4 MHz	0.90	1.6(2)	
			f_{CPU} = 2 MHz	0.80	1.5	
$I_{DD(SLOW)}$(1)	Supply current in Slow mode	f_{CPU} scaled down, all peripherals off, code executed from RAM	Ext. clock 16 MHz f_{CPU} = 125 kHz	1.50	1.95	
			LSI internal RC f_{CPU} = 128 kHz	1.50	1.80(2)	

1. The current due to I/O utilization is not taken into account in these values.
2. Values not tested in production. Design guidelines only.

Figure 12. Typ. $I_{DD(RUN)HSI}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripheral = off

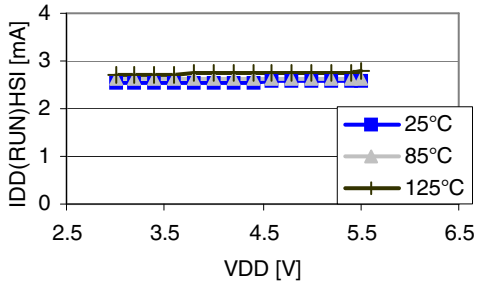


Figure 13. Typ. $I_{DD(WFI)HSE}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripheral = on

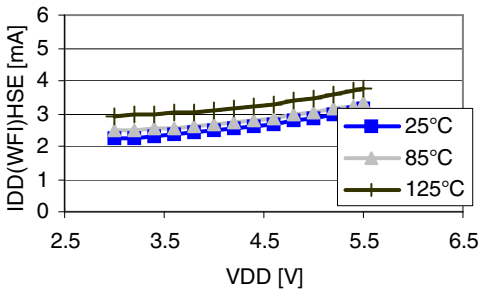


Figure 14. Typ. $I_{DD(WFI)HSE}$ vs. f_{CPU} @ V_{DD} = 5.0 V, peripheral = on

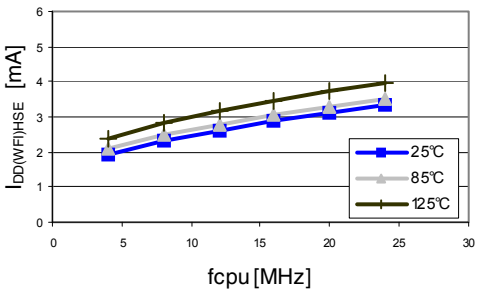
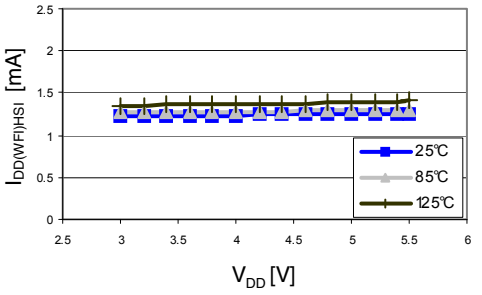


Figure 15. Typ. $I_{DD(WFI)HSI}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripheral = off



10.3.3 External clock sources and timing characteristics

HSE user external clock

Subject to general operating conditions for V_{DD} and T_A.

Table 28. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	T_A is -40 to 150 °C	0(1)	-	16	MHz
V_{HSEdHL}	Comparator hysteresis	-	0.1 x V_{DD}	-	-	V
V_{HSEH}	OSCIN input pin high level voltage	-	0.7 x V_{DD}	-	V_{DD}	
V_{HSEL}	OSCIN input pin low level voltage	-	V_{SS}	-	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	-	+1	µA

1. In CSS is used, the external clock must have a frequency above 500 kHz.

10.3.7 Reset pin characteristics

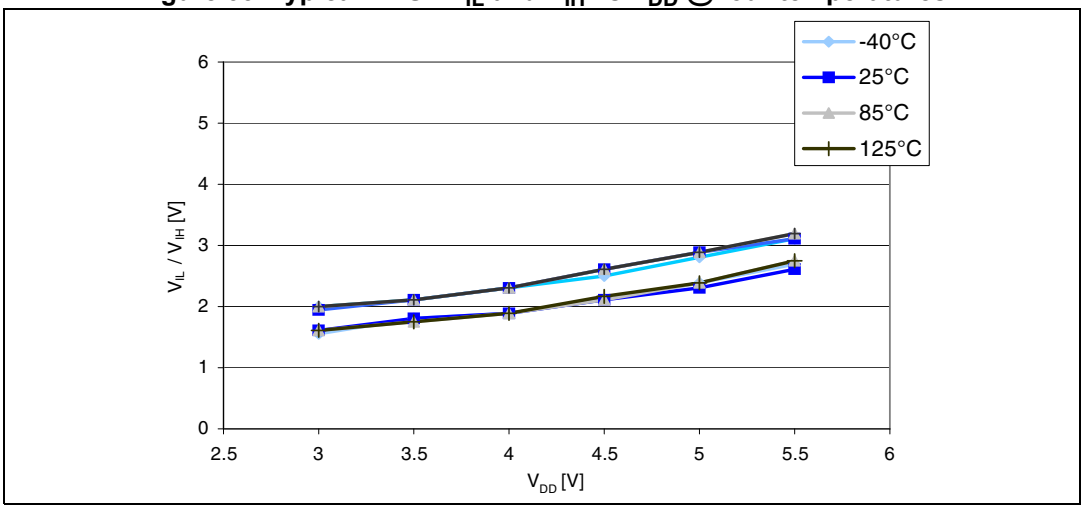
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 36. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)	-	V_{SS}	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage(1)	-	0.7 x V_{DD}	-	V_{DD}	
$V_{OL(NRST)}$	NRST output low level voltage(1)	I_{OL}= 3 mA	-	-	0.6	
$R_{PU(NRST)}$	NRST pull-up resistor	-	30	40	60	kΩ
t_{IFP}	NRST input filtered pulse(1)	-	85	-	315	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse duration(2)	-	500	-	-	

1. Data based on characterization results, not tested in production.
2. Data guaranteed by design, not tested in production.

Figure 33. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ four temperatures



10.3.10 I²C interface characteristics

Table 39. I²C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	-	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time (V_{DD} = 3 to 5.5 V)	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time (V_{DD} = 3 to 5.5 V)	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

Electromagnetic interference (EMI)

Emission tests conform to the IEC 61967-2 standard for test software, board layout and pin loading.

Table 43. EMI data

Symbol	Parameter	Conditions				Unit
		General conditions	Monitored frequency band	Max f_{CPU}(1)		
				8 MHz	16 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP80 package conforming to IEC 61967-2	0.1 MHz to 30 MHz	15	17	dBµV
			30 MHz to 130 MHz	18	22	
			130 MHz to 1 GHz	-1	3	
	EMI level		-	2	2.5	

1. Data based on characterization results, not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

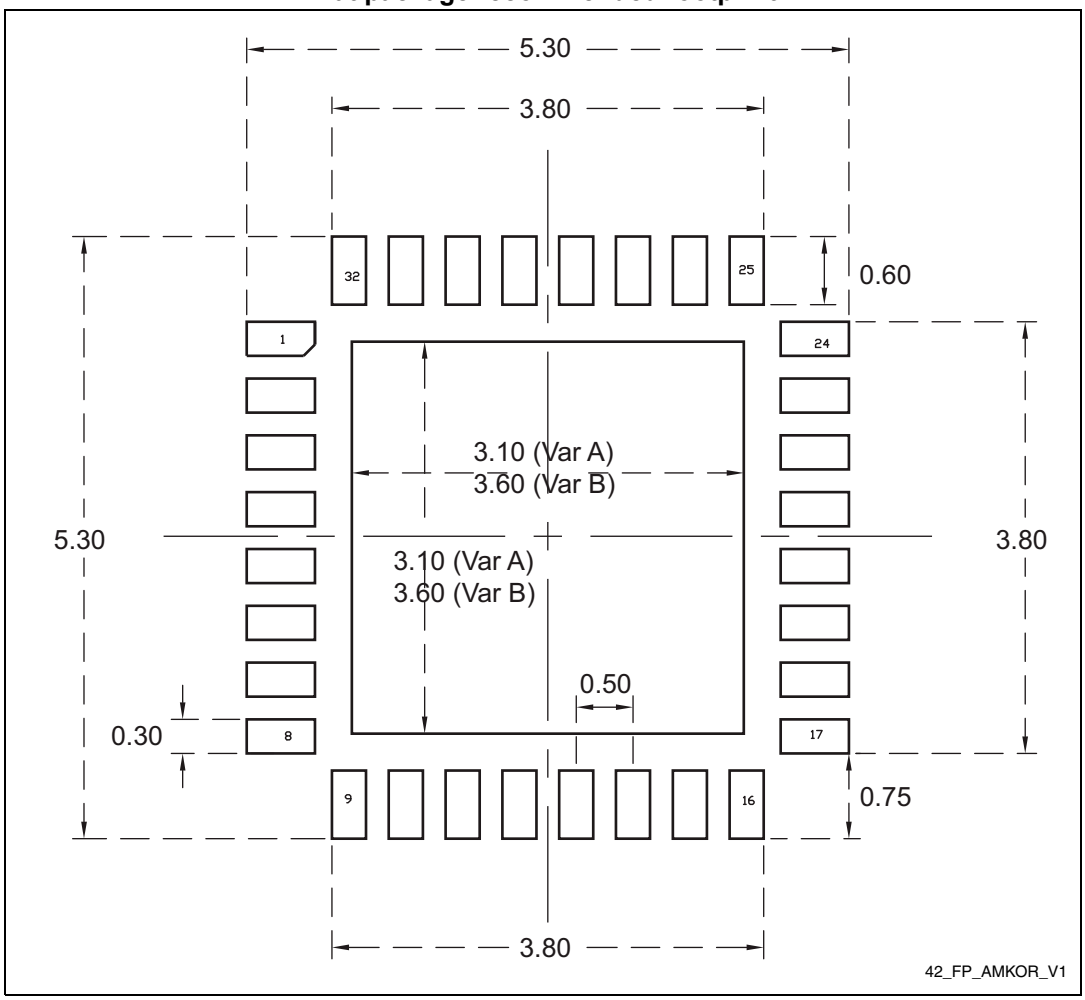
Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 44. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to JESD22-A114	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A= 25°C, conforming to JESD22-C101	3	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine model)	T_A= 25°C, conforming to JESD22-A115	B	200	

1. Data based on characterization results, not tested in production

Figure 43. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 44. VFQFPN32 marking example (package top view)

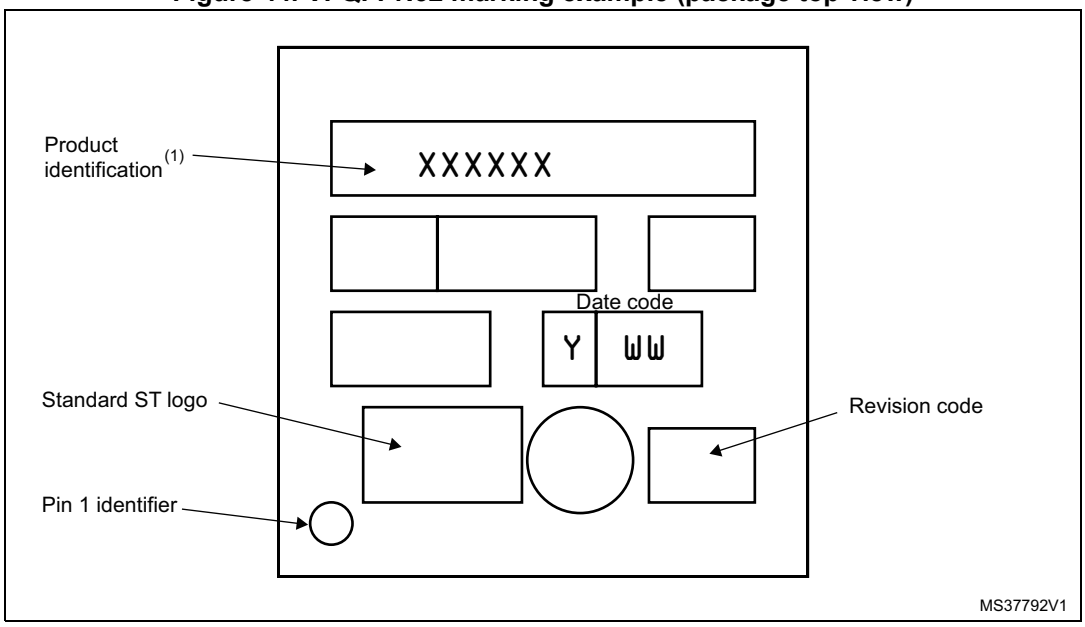
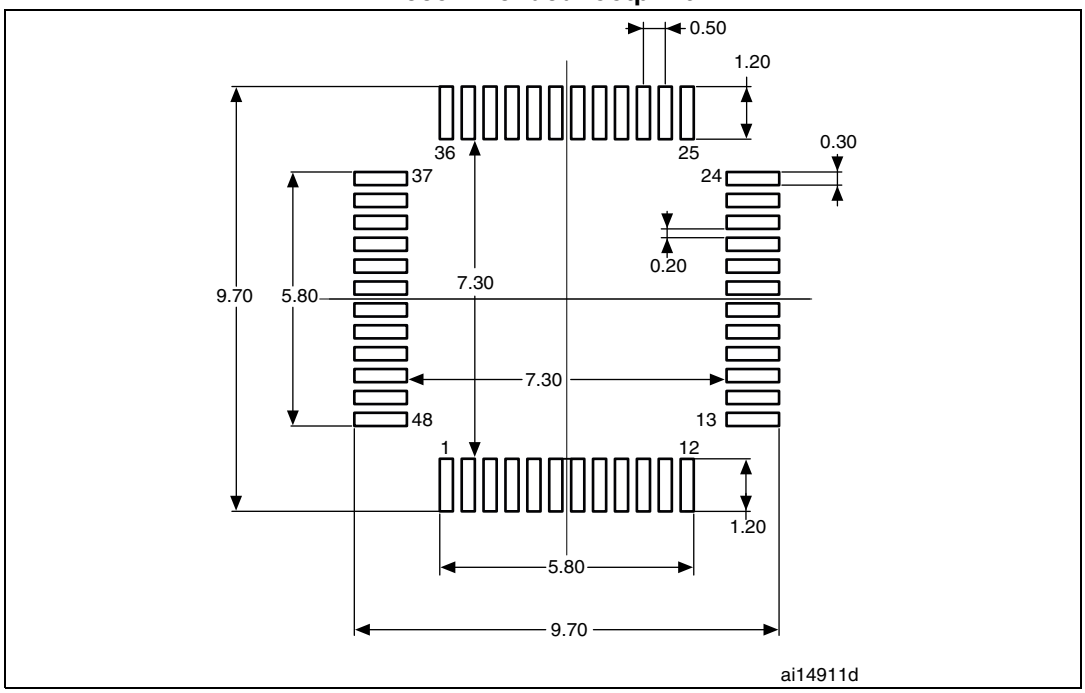


Figure 46. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint

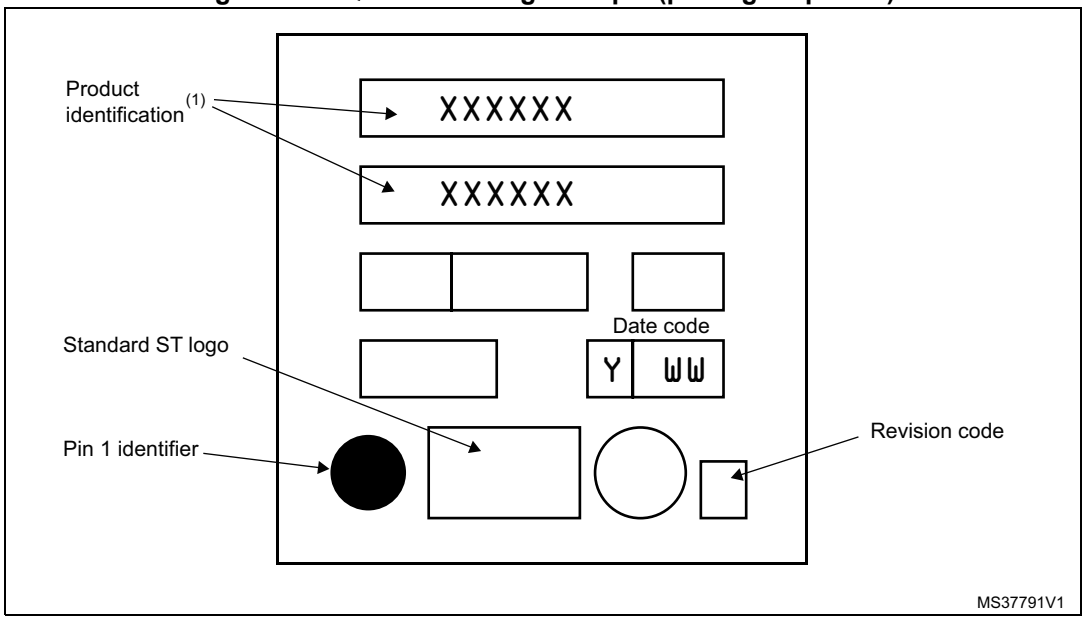


1. Dimensions are expressed in millimeters.

Device marking

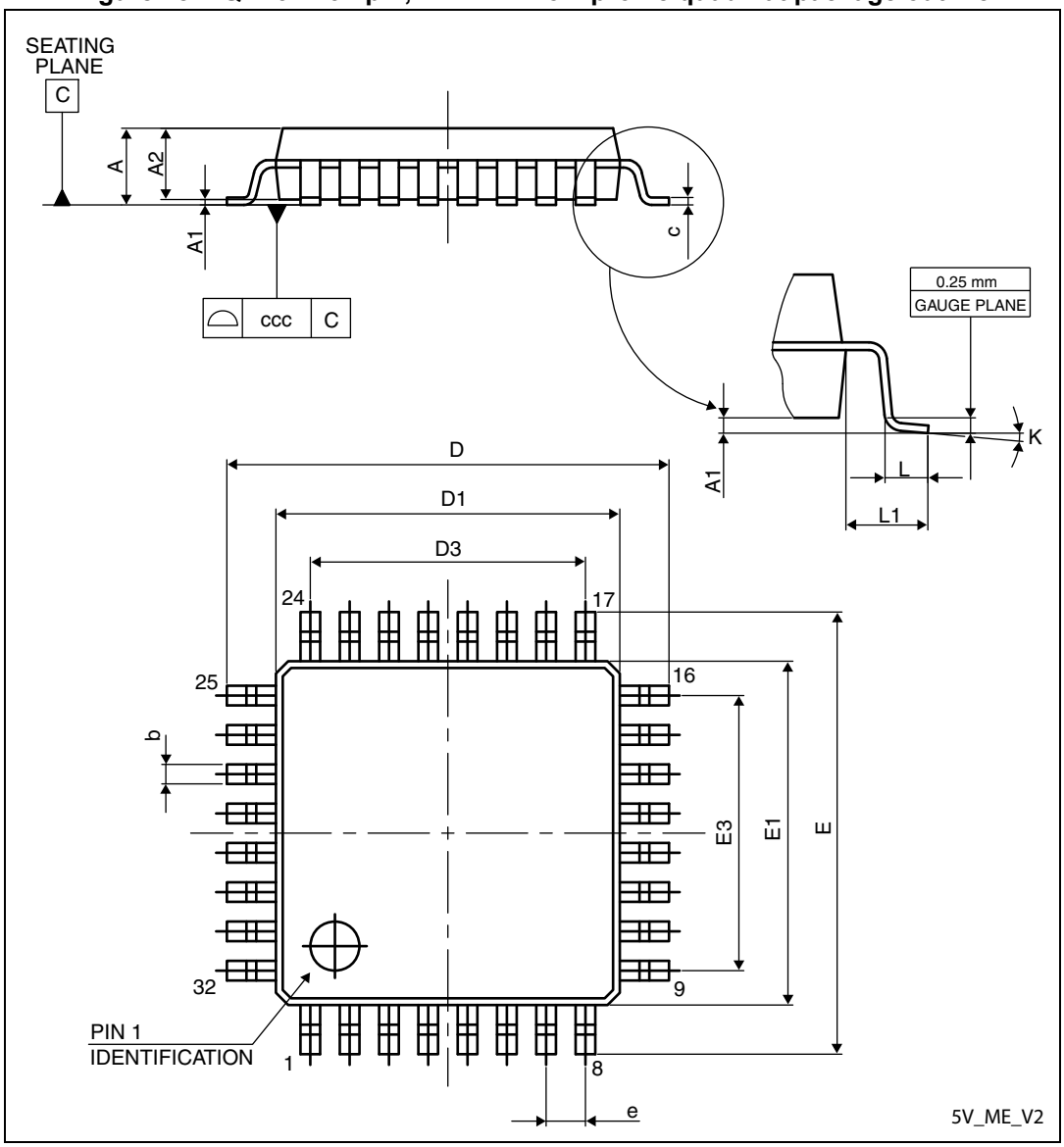
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 47. LQFP48 marking example (package top view)



11.3 LQFP32 package information

Figure 48. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

13.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST visual develop (STVD) IDE and the ST visual programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8.

13.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at www.st.com. This package includes:

ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8A microcontroller Flash memory. STVP also offers project mode for saving programming configurations and automating programming sequences.

13.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of the application directly from an easy-to-use graphical interface.

Available toolchains include:

C compiler for STM8

All compilers are available in free version with a limited code size depending on the compiler. For more information, refer to www.cosmic-software.com, www.raisonance.com, and www.iar.com.

STM8 assembler linker

Free assembly toolchain included in the STM8 toolset, which allows users to assemble and link the application source code.

Table 50. Document revision history (continued)

Date	Revision	Changes
31-Jan-2011	5	Modified references to reference manual, and Flash programming manual in the whole document. Added reference to AEC Q100 standard on cover page. Renamed timer types as follows: – Auto-reload timer to general purpose timer – Multipurpose timer to advanced control timer – System timer to basic timer Introduced concept of medium density Flash program memory. Updated timer names in *Figure: STM8A block diagram.* Added TMU brief description in *Section: Flash program and data EEPROM*, and updated TMU_MAXATT description in *Table: Option byte description*. Updated clock sources in clock controller features. Changed 16MHZTRIM0 to HSITRIM bit in *Section: User trimming.* Added *Table: Peripheral clock gating bits.* Updated *Section: Low-power operating modes.* Added calibration using TIM3 in *Section: Auto-wakeup counter.* Added *Table: ADC naming* and *Table: Communication peripheral naming correspondence.* Added *Note 1* related AIN12 pin in *Section: Analog-to-digital converter (ADC)* and *Table: STM8AF61xx/62xx (32 Kbyte) microcontroller pin description.* Updated SPI data rate to 10 Mbit/s or $f_{MASTER}/2$ in *Section: Serial peripheral interface (SPI).* Added reset state in *Table: Legend/abbreviation.* *Table: STM8AF61xx/62xx (32 Kbyte) microcontroller pin description:* added *Note 7* related to PD1/SWIM, modified *Note 6,* corrected wpu input for PE1 and PE2, and renamed TIMn_CCx and TIMn_NCCx to TIMn_CHx and TIMn_CHxN, respectively. ***Section: Register map:*** Replaced tables describing register maps and reset values for non-volatile memory, global configuration, reset status, clock controller, interrupt controller, timers, communication interfaces, and ADC, by *Table: General hardware register map*. Added *Note 1* for Px_IDR registers in *Table: I/O port hardware register map.* Updated register reset values for Px_IDR registers. Added SWIM and debug module register map.