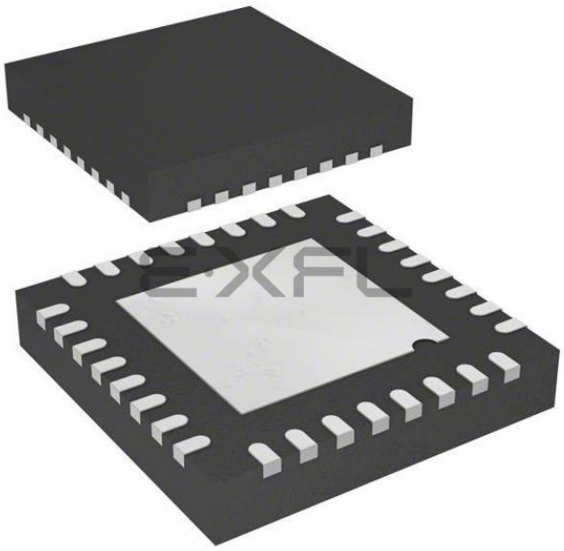


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6246udy

List of tables

1 Introduction

This datasheet refers to the STM8AF6246, STM8AF6248, STM8AF6266 and STM8AF6268 products with 16 to 32 Kbyte of Flash program memory.

In the order code, the letter ‘F’ refers to product versions with data EEPROM and ‘H’ refers to product versions without data EEPROM. The identifiers ‘F’ and ‘H’ do not coexist in a given order code.

The datasheet contains the description of family features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8A microcontroller memory, registers and peripherals, please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8 Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

3 Product line-up

Table 1. STM8AF6246/48/66/68 product line-up

Order code	Package	Medium density Flash program memory (byte)	RAM (byte)	Data EE (byte)	10-bit A/D ch.	Timers (IC/OC/PWM)	Serial interfaces	I/0 wakeup pins
STM8AF/P6268	LQFP48 (7x7)	32 K	2 K	1 K	10	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	LIN(UART), SPI, I²C	38/35
STM8AF/P6248		16 K		0.5 K				
STM8AF/P6266	LQFP32 (7x7)	32 K		1 K	7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	LIN(UART), SPI, I²C	25/23
STM8AF/P6246		16 K		0.5 K				
STM8AF/P6266	VFQFPN32	32 K		1 K	7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	LIN(UART), SPI, I²C	25/23
STM8AF/P6246		16 K		0.5 K				

5.4.2 Write protection (WP)

Write protection in application mode is intended to avoid unintentional overwriting of the memory. The write protection can be removed temporarily by executing a specific sequence in the user software.

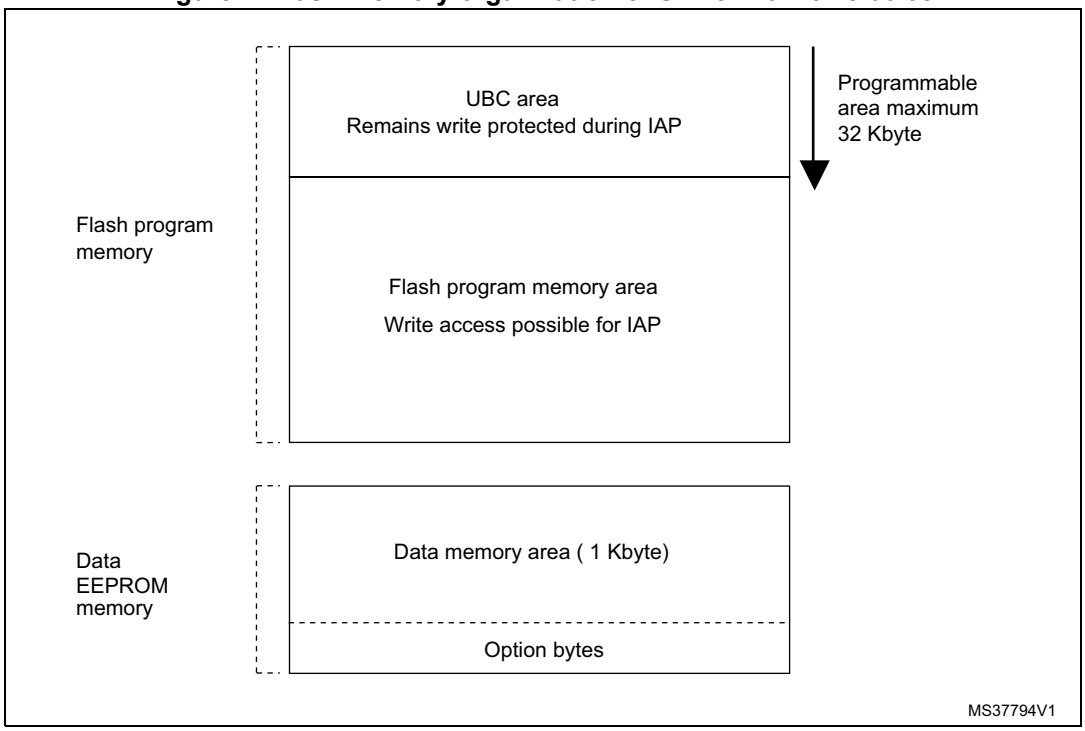
5.4.3 Protection of user boot code (UBC)

If the user chooses to update the Flash program memory using a specific boot code to perform in application programming (IAP), this boot code needs to be protected against unwanted modification.

In the STM8A a memory area of up to 32 Kbyte can be protected from overwriting at user option level. Other than the standard write protection, the UBC protection can exclusively be modified via the debug interface, the user software cannot modify the UBC protection status.

The UBC memory area contains the reset and interrupt vectors and its size can be adjusted in increments of 512 bytes by programming the UBC and NUBC option bytes (see *Section 9: Option bytes on page 44*).

Figure 2. Flash memory organization of STM8AF6246/48/66/68



5.9.1 Serial peripheral interface (SPI)

The devices covered by this datasheet contain one SPI. The SPI is available on all the supported packages.

- Maximum speed: 10 Mbit/s or $f_{MASTER}/2$ both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave mode/master mode management by hardware or software for both master and slave
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Dedicated transmission and reception flags with interrupt capability
- SPI bus busy status flag
- Hardware CRC feature for reliable communication:
  - CRC value can be transmitted as last byte in Tx mode
  - CRC error checking for last received byte

5.9.2 Inter integrated circuit (I^2C) interface

The devices covered by this datasheet contain one I^2C interface. The interface is available on all the supported packages.

- I^2C master features:
  - Clock generation
  - Start and stop generation
- I^2C slave features:
  - Programmable I^2C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz),
  - Fast speed (up to 400 kHz)
- Status flags:
  - Transmitter/receiver mode flag
  - End-of-byte transmission flag
  - I^2C busy flag
- Error flags:
  - Arbitration lost condition for master mode
  - Acknowledgment failure after address/data transmission
  - Detection of misplaced start or stop condition
  - Overrun/underrun if clock stretching is disabled

- Interrupt:
  - Successful address/data communication
  - Error condition
  - Wakeup from Halt
- Wakeup from Halt on address detection in slave mode

5.9.3 Universal asynchronous receiver/transmitter with LIN support (LINUART)

The devices covered by this datasheet contain one LINUART interface. The interface is available on all the supported packages. The LINUART is an asynchronous serial communication interface which supports extensive LIN functions tailored for LIN slave applications. In LIN mode it is compliant to the LIN standards rev 1.2 to rev 2.2.

Detailed feature list:

LIN mode

Master mode:

- LIN break and delimiter generation
- LIN break and delimiter detection with separate flag and interrupt source for read back checking.

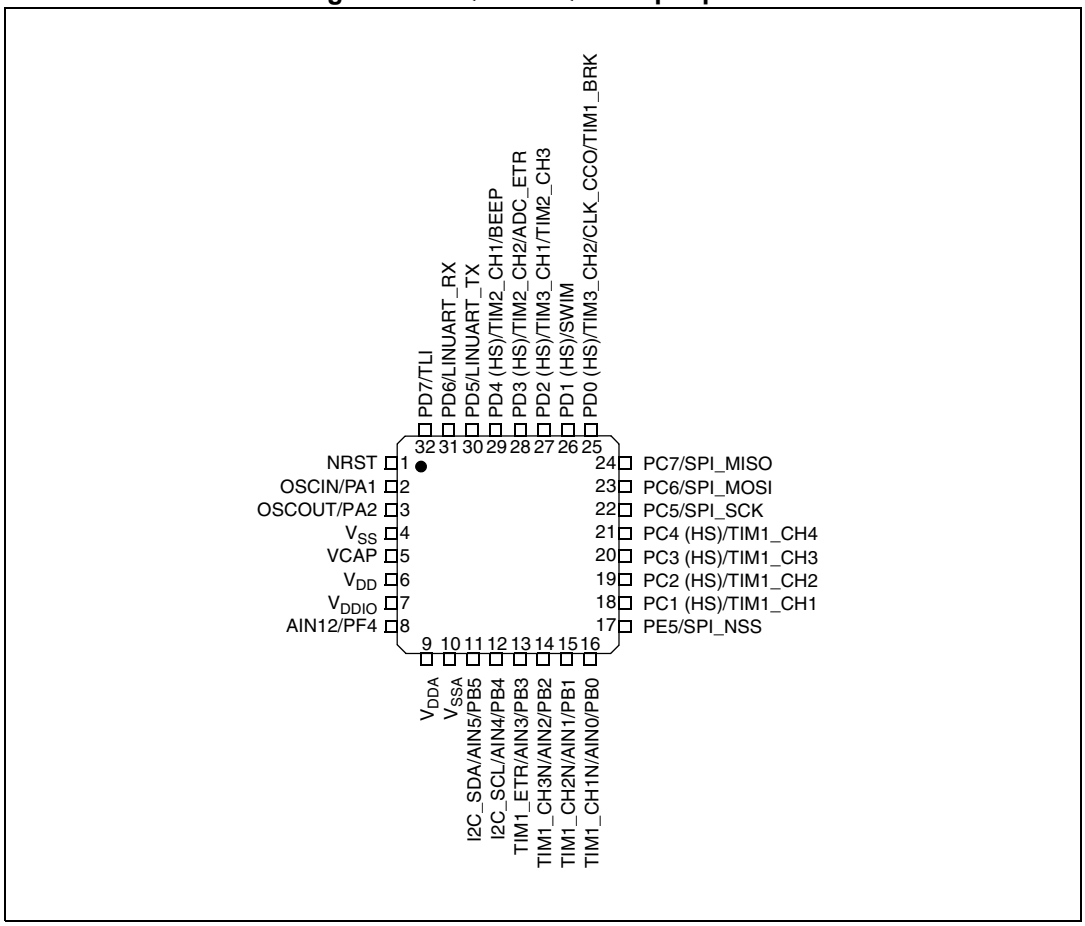
Slave mode:

- Autonomous header handling – one single interrupt per valid header
- Mute mode to filter responses
- Identifier parity error checking
- LIN automatic resynchronization, allowing operation with internal RC oscillator (HSI) clock source
- Break detection at any time, even during a byte reception
- Header errors detection:
  - Delimiter too short
  - Synch field error
  - Deviation error (if automatic resynchronization is enabled)
  - Framing error in synch field or identifier field
  - Header time-out

6 Pinouts and pin description

6.1 Package pinouts

Figure 3. VFQFPN/LQFP 32-pin pinout



1. (HS) high sink capability.

Table 8. STM8AF6246/48/66/68 (32 Kbyte) microcontroller pin description(1)(2)

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	VFQFPN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
2	2	PA1/OSCIN(3)	I/O	**X**	X	-	-	O1	X	X	**Port A1**	Resonator/crystal in	-
3	3	PA2/OSCOUT	I/O	**X**	X	X	-	O1	X	X	**Port A2**	Resonator/crystal out	-
4	-	V_{SSIO_1}	S	-	-	-	-	-	-	-	I/O ground		-
5	4	V_{SS}	S	-	-	-	-	-	-	-	Digital ground		-
6	5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
7	6	V_{DD}	S	-	-	-	-	-	-	-	Digital power supply		-
8	7	V_{DDIO_1}	S	-	-	-	-	-	-	-	I/O power supply		-
-	8	PF4/AIN12(4)(5)	I/O	**X**	X		-	O1	X	X	**Port F4**	Analog input 12	-
9	-	PA3/TIM2_CH3	I/O	**X**	X	X	-	O1	X	X	**Port A3**	Timer 2 - channel 3	TIM3_CH1 [AFR1]
10	-	PA4	I/O	**X**	X	X	-	O3	X	X	**Port A4**		-
11	-	PA5	I/O	**X**	X	X	-	O3	X	X	**Port A5**		-
12	-	PA6	I/O	**X**	X	X	-	O3	X	X	**Port A6**		-
13	9	V_{DDA}	S	-	-	-	-	-	-	-	Analog power supply		-
14	10	V_{SSA}	S	-	-	-	-	-	-	-	Analog ground		-
15	-	PB7/AIN7	I/O	**X**	X	X	-	O1	X	X	**Port B7**	Analog input 7	-
16	-	PB6/AIN6	I/O	**X**	X	X	-	O1	X	X	**Port B6**	Analog input 6	-
17	11	PB5/AIN5	I/O	**X**	X	X	-	O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
18	12	PB4/AIN4	I/O	**X**	X	X	-	O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]
19	13	PB3/AIN3	I/O	**X**	X	X	-	O1	X	X	**Port B3**	Analog input 3	TIM1_ETR [AFR5]
20	14	PB2/AIN2	I/O	**X**	X	X	-	O1	X	X	**Port B2**	Analog input	TIM1_NCC3 [AFR5]
21	15	PB1/AIN1	I/O	**X**	X	X	-	O1	X	X	**Port B1**	Analog input 1	TIM1_NCC2 [AFR5]
22	16	PB0/AIN0	I/O	**X**	X	X	-	O1	X	X	**Port B0**	Analog input 0	TIM1_NCC1 [AFR5]
23	-	PE7/AIN8	I/O	**X**	X		-	O1	X	X	**Port E7**	Analog input 8	-

Table 8. STM8AF6246/48/66/68 (32 Kbyte) microcontroller pin description(1)(2) (continued)

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	VFQFPN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
24		PE6/AIN9	I/O	**X**	X	X	-	O1	X	X	**Port E7**	Analog input 9	-
25	17	PE5/SPI_NSS	I/O	**X**	X	X	-	O1	X	X	**Port E5**	SPI master/slave select	-
26	18	PC1/TIM1_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1	-
27	19	PC2/TIM1_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1- channel 2	-
28	20	PC3/TIM1_CH3	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	-
29	21	PC4/TIM1_CH4	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4	-
30	22	PC5/SPI_SCK	I/O	**X**	X	X		O3	X	X	**Port C5**	SPI clock	-
31	-	V_{SSIO_2}	S	-	-	-	-	-	-	-	I/O ground		-
32	-	V_{DDIO_2}	S	-	-	-	-	-	-	-	I/O power supply		-
33	23	PC6/SPI_MOSI	I/O	**X**	X	X	-	O3	X	X	**Port C6**	SPI master out/ slave in	-
34	24	PC7/SPI_MISO	I/O	**X**	X	X	-	O3	X	X	**Port C7**	SPI master in/ slave out	-
35	-	PG0	I/O	**X**	X	-	-	O1	X	X	**Port G0**	-	-
36	-	PG1	I/O	**X**	X	-	-	O1	X	X	**Port G1**	-	-
37	-	PE3/TIM1_BKIN	I/O	**X**	X	X	-	O1	X	X	**Port E3**	Timer 1 - break input	-
38	-	PE2/I^2C_SDA	I/O	**X**	-	X	-	O1	T(6)	-	**Port E2**	I^2C data	-
39	-	PE1/I^2C_SCL	I/O	**X**	-	X	-	O1	T(6)	-	**Port E1**	I^2C clock	-
40	-	PE0/CLK_CCO	I/O	**X**	X	X	-	O3	X	X	**Port E0**	Configurable clock output	-
41	25	PD0/TIM3_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 3 - channel 2	TIM1_BKIN [AFR3]/ CLK_CCO [AFR2]
42	26	PD1/SWIM(7)	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	-
43	27	PD2/TIM3_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	Timer 3 - channel 1	TIM2_CH3 [AFR1]
44	28	PD3/TIM2_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2	ADC_ETR [AFR0]
45	29	PD4/TIM2_CH1/ BEEP	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1	BEEP output [AFR7]
46	30	PD5/ LINUART_TX	I/O	**X**	X	X	-	O1	X	X	**Port D5**	LINUART data transmit	-

7 Memory and register map

7.1 Memory map

Figure 5. Register and memory map of STM8A products

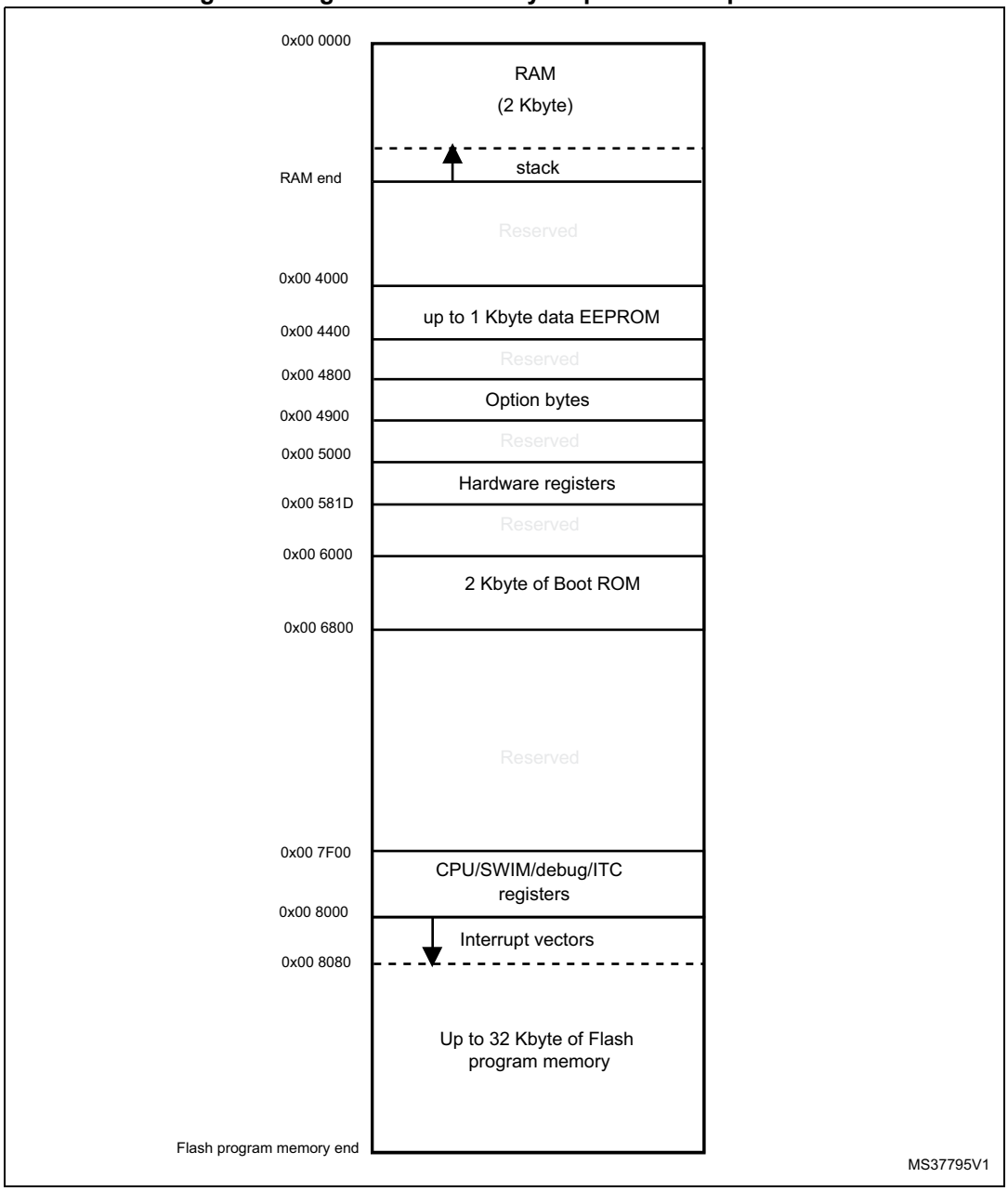


Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5240	LINUART	UART2_SR	LINUART status register	0xC0
0x00 5241		UART2_DR	LINUART data register	0xXX
0x00 5242		UART2_BRR1	LINUART baud rate register 1	0x00
0x00 5243		UART2_BRR2	LINUART baud rate register 2	0x00
0x00 5244		UART2_CR1	LINUART control register 1	0x00
0x00 5245		UART2_CR2	LINUART control register 2	0x00
0x00 5246		UART2_CR3	LINUART control register 3	0x00
0x00 5247		UART2_CR4	LINUART control register 4	0x00
0x00 5248		Reserved		
0x00 5249		UART2_CR6	LINUART control register 6	0x00
0x00 524A to 0x00 524F	Reserved area (6 bytes)			
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00

Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5265	TIM1	TIM1_CCR1H	TIM1 capture/compare register 1 high	0x00
0x00 5266		TIM1_CCR1L	TIM1 capture/compare register 1 low	0x00
0x00 5267		TIM1_CCR2H	TIM1 capture/compare register 2 high	0x00
0x00 5268		TIM1_CCR2L	TIM1 capture/compare register 2 low	0x00
0x00 5269		TIM1_CCR3H	TIM1 capture/compare register 3 high	0x00
0x00 526A		TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 bytes)			
0x00 5300	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5301		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5302		TIM2_SR1	TIM2 status register 1	0x00
0x00 5303		TIM2_SR2	TIM2 status register 2	0x00
0x00 5304		TIM2_EGR	TIM2 event generation register	0x00
0x00 5305		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5306		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 5307		TIM2_CCMR3	TIM2 capture/compare mode register 3	0x00
0x00 5308		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 5309		TIM2_CCER2	TIM2 capture/compare enable register 2	0x00
0x00 530A		TIM2_CNTRH	TIM2 counter high	0x00
0x00 530B		TIM2_CNTRL	TIM2 counter low	0x00
00 530C0x		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 530D		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 530E		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 530F		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5310		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5311		TIM2_CCR2H	TIM2 capture/compare reg. 2 high	0x00
0x00 5312		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5313		TIM2_CCR3H	TIM2 capture/compare register 3 high	0x00

Table 18. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDDIO}	Total current into V_{DDIO} power lines (source)(1)(2)(3)	100	mA
I_{VSSIO}	Total current out of $V_{SS\ IO}$ ground lines (sink)(1)(2)(3)	100	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	-20	
$I_{INJ(PIN)}$(4)	Injected current on any pin	±10	
$I_{INJ(TOT)}$	Sum of injected currents	50	

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external supply.
2. The total limit applies to the sum of operation and injected currents.
3. V_{DDIO} includes the sum of the positive injection currents. V_{SSIO} includes the sum of the negative injection currents.
4. This condition is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current allowed and the corresponding V_{IN} maximum must always be respected.

Table 19. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	160	

Table 20. Operating lifetime(1)

Symbol	Ratings	Value	Unit
OLF	Conforming to AEC-Q100 rev G	-40 to 125 °C	Grade 1
		-40 to 150 °C	Grade 0

1. For detailed mission profile analysis, please contact the nearest local ST Sales Office.

10.3.5 Memory characteristics

Flash program memory/data EEPROM memory

General conditions: T_A = -40 to 150 °C.

Table 32. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	f_{CPU} is 0 to 16 MHz with 0 ws	3.0	-	5.5	V
V_{DD}	Operating voltage (code execution)	f_{CPU} is 0 to 16 MHz with 0 ws	2.6	-	5.5	
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/128 bytes)	-	-	6	6.6	ms
	Fast programming time for 1 block (128 bytes)	-	-	3	3.3	
t_{erase}	Erase time for 1 block (128 bytes)	-	-	3	3.3	

Table 33. Flash program memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Flash program memory endurance (erase/write cycles)(1)	T_A = 25 °C	1000	-	cycles
t_{RET}	Data retention time	T_A = 25 °C	40	-	years
		T_A = 55 °C	20	-	

1. The physical granularity of the memory is four bytes, so cycling is performed on four bytes even when a write/erase operation addresses a single byte.

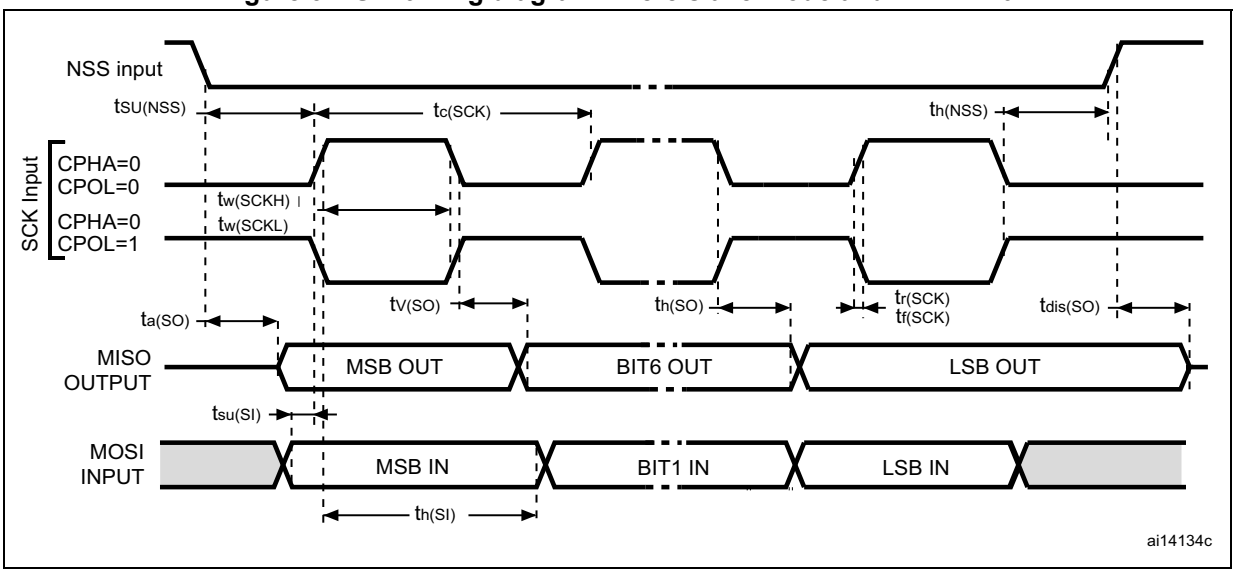
Table 34. Data memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Data memory endurance(1) (erase/write cycles)	T_A = 25 °C	300 k	-	cycles
		T_A = -40°C to 125 °C	100 k(2)	-	
t_{RET}	Data retention time	T_A = 25 °C	40(2)(3)	-	years
		T_A = 55 °C	20(2)(3)	-	

1. The physical granularity of the memory is four bytes, so cycling is performed on four bytes even when a write/erase operation addresses a single byte.
2. More information on the relationship between data retention time and number of write/erase cycles is available in a separate technical document.
3. Retention time for 256B of data memory after up to 1000 cycles at 125 °C.

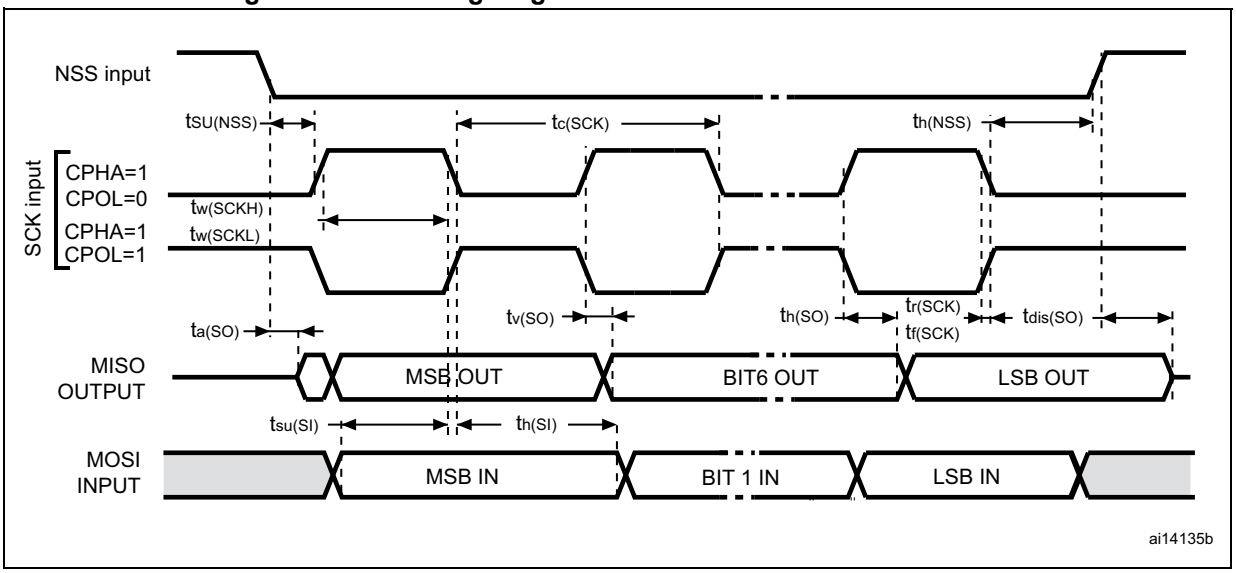
3. Values based on design simulation and/or characterization results, and not tested in production.
4. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
5. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 37. SPI timing diagram where slave mode and CPHA = 0



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 38. SPI timing diagram where slave mode and CPHA = 1



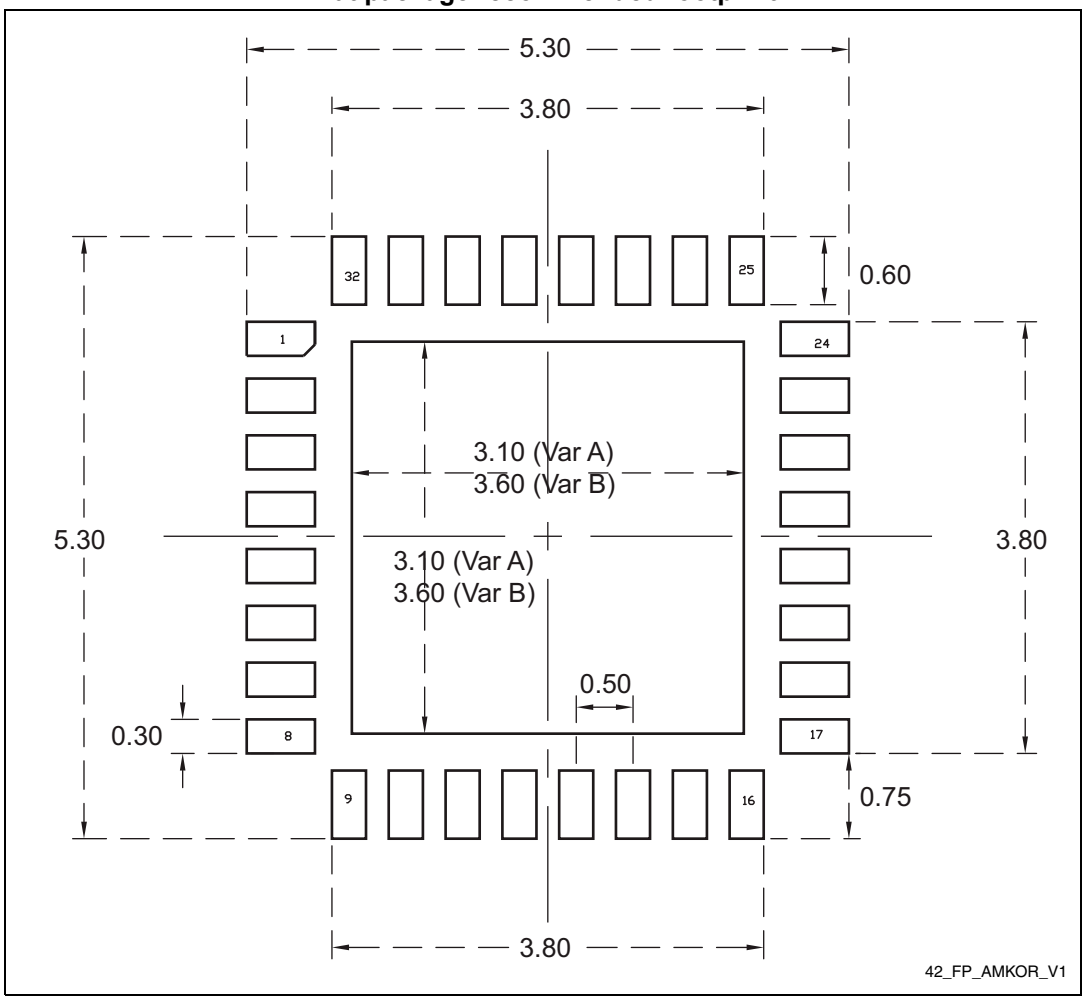
1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Table 46. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.200	-	-	0.0079	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D2	3.500	3.600	3.700	0.1378	0.1417	0.1457
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E2	3.500	3.600	3.700	0.1378	0.1417	0.1457
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 43. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Table 48. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.