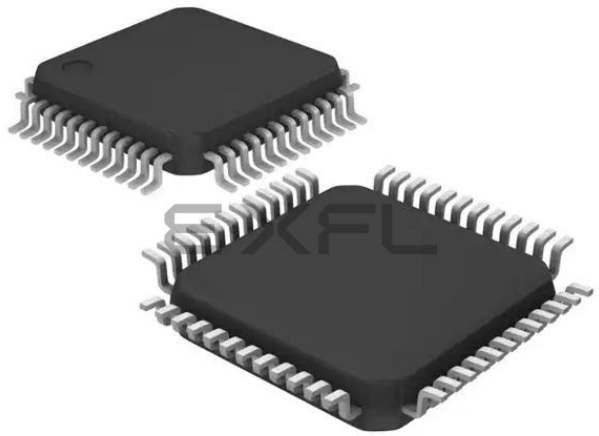

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6248tcy

1 Introduction

This datasheet refers to the STM8AF6246, STM8AF6248, STM8AF6266 and STM8AF6268 products with 16 to 32 Kbyte of Flash program memory.

In the order code, the letter ‘F’ refers to product versions with data EEPROM and ‘H’ refers to product versions without data EEPROM. The identifiers ‘F’ and ‘H’ do not coexist in a given order code.

The datasheet contains the description of family features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8A microcontroller memory, registers and peripherals, please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8 Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

5.5.3 128 kHz low-speed internal RC oscillator (LSI)

The frequency of this clock is 128 kHz and it is independent from the main clock. It drives the independent watchdog or the AWU wakeup timer.

In systems which do not need independent clock sources for the watchdog counters, the 128 kHz signal can be used as the system clock. This configuration has to be enabled by setting an option byte (OPT3/OPT3N, bit LSI_EN).

5.5.4 16 MHz high-speed external crystal oscillator (HSE)

The external high-speed crystal oscillator can be selected to deliver the main clock in normal Run mode. It operates with quartz crystals and ceramic resonators.

- Frequency range: 1 MHz to 16 MHz
- Crystal oscillation mode: preferred fundamental
- I/Os: standard I/O pins multiplexed with OSCIN, OSCOUT

5.5.5 External clock input

An external clock signal can be applied to the OSCIN input pin of the crystal oscillator. The frequency range is 0 to 16 MHz.

5.5.6 Clock security system (CSS)

The clock security system protects against a system stall in case of an external crystal clock failure.

In case of a clock failure an interrupt is generated and the high-speed internal clock (HSI) is automatically selected with a frequency of 2 MHz (16 MHz/8).

Table 2. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers

Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock
PCKEN17	TIM1	PCKEN13	LINUART	PCKEN27	Reserved	PCKEN23	ADC
PCKEN16	TIM3	PCKEN12	Reserved	PCKEN26	Reserved	PCKEN22	AWU
PCKEN15	TIM2	PCKEN11	SPI	PCKEN25	Reserved	PCKEN21	Reserved
PCKEN14	TIM4	PCKEN10	I^2C	PCKEN24	Reserved	PCKEN20	Reserved

5.6 Low-power operating modes

For efficient power management, the application can be put in one of four different low power modes. Users can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- Wait mode

  In this mode, the CPU is stopped but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.

- Active-halt mode with regulator on

  In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in Active-halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.

- Active-halt mode with regulator off

  This mode is the same as Active-halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.

- Halt mode

  CPU and peripheral clocks are stopped, the main voltage regulator is powered off.

  Wakeup is triggered by external event or reset.

In all modes the CPU and peripherals remain permanently powered on, the system clock is applied only to selected modules. The RAM content is preserved and the brown-out reset circuit remains activated.

5.7 Timers

5.7.1 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications. The watchdog timer activity is controlled by the application program or option bytes. Once the watchdog is activated, it cannot be disabled by the user program without going through reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application timing perfectly. The application software must refresh the counter before time-out and during a limited time window. If the counter is refreshed outside this time window, a reset is issued.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure. If the hardware watchdog feature is enabled through the device option bits, the watchdog is automatically enabled at power-on, and generates a reset unless the key register is written by software before the counter reaches the end of count.

5.7.2 Auto-wakeup counter

This counter is used to cyclically wakeup the device in Active-halt mode. It can be clocked by the internal 128 kHz internal low-frequency RC oscillator or external clock.

LSI clock can be internally connected to TIM3 input capture channel 1 for calibration.

5.7.3 Beeper

This function generates a rectangular signal in the range of 1, 2 or 4 kHz which can be output on a pin. This is useful when audible sounds without interference need to be generated for use in the application.

5.7.4 Advanced control and general purpose timers

STM8A devices described in this datasheet, contain up to three 16-bit advanced control and general purpose timers providing nine CAPCOM channels in total. A CAPCOM channel can be used either as input compare, output compare or PWM channel. These timers are named TIM1, TIM2 and TIM3.

Table 3. Advanced control and general purpose timers

Timer	Counter width	Counter type	Prescaler factor	Channels	Inverted outputs	Repetition counter	trigger unit	External trigger	Break input
TIM1	16-bit	Up/down	1 to 65536	4	3	Yes	Yes	Yes	Yes
TIM2	16-bit	Up	2^n n = 0 to 15	3	None	No	No	No	No
TIM3	16-bit	Up	2^n n = 0 to 15	2	None	No	No	No	No

Table 8. STM8AF6246/48/66/68 (32 Kbyte) microcontroller pin description(1)(2) (continued)

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	VFQFPN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
24		PE6/AIN9	I/O	**X**	X	X	-	O1	X	X	**Port E7**	Analog input 9	-
25	17	PE5/SPI_NSS	I/O	**X**	X	X	-	O1	X	X	**Port E5**	SPI master/slave select	-
26	18	PC1/TIM1_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1	-
27	19	PC2/TIM1_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1- channel 2	-
28	20	PC3/TIM1_CH3	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	-
29	21	PC4/TIM1_CH4	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4	-
30	22	PC5/SPI_SCK	I/O	**X**	X	X		O3	X	X	**Port C5**	SPI clock	-
31	-	V_{SSIO_2}	S	-	-	-	-	-	-	-	I/O ground		-
32	-	V_{DDIO_2}	S	-	-	-	-	-	-	-	I/O power supply		-
33	23	PC6/SPI_MOSI	I/O	**X**	X	X	-	O3	X	X	**Port C6**	SPI master out/ slave in	-
34	24	PC7/SPI_MISO	I/O	**X**	X	X	-	O3	X	X	**Port C7**	SPI master in/ slave out	-
35	-	PG0	I/O	**X**	X	-	-	O1	X	X	**Port G0**	-	-
36	-	PG1	I/O	**X**	X	-	-	O1	X	X	**Port G1**	-	-
37	-	PE3/TIM1_BKIN	I/O	**X**	X	X	-	O1	X	X	**Port E3**	Timer 1 - break input	-
38	-	PE2/I^2C_SDA	I/O	**X**	-	X	-	O1	T(6)	-	**Port E2**	I^2C data	-
39	-	PE1/I^2C_SCL	I/O	**X**	-	X	-	O1	T(6)	-	**Port E1**	I^2C clock	-
40	-	PE0/CLK_CCO	I/O	**X**	X	X	-	O3	X	X	**Port E0**	Configurable clock output	-
41	25	PD0/TIM3_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 3 - channel 2	TIM1_BKIN [AFR3]/ CLK_CCO [AFR2]
42	26	PD1/SWIM(7)	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	-
43	27	PD2/TIM3_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	Timer 3 - channel 1	TIM2_CH3 [AFR1]
44	28	PD3/TIM2_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2	ADC_ETR [AFR0]
45	29	PD4/TIM2_CH1/ BEEP	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1	BEEP output [AFR7]
46	30	PD5/ LINUART_TX	I/O	**X**	X	X	-	O1	X	X	**Port D5**	LINUART data transmit	-

Table 9. Memory model for the devices covered in this datasheet

Flash program memory size	Flash program memory end address	RAM size	RAM end address	Stack roll-over address
32K	0x00 0FFFF	2K	0x00 07FF	0x00 0600
16K	0x00 0BFFF			

7.2 Register map

In this section the memory and register map of the devices covered by this datasheet is described. For a detailed description of the functionality of the registers, refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016.

Table 10. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX(1)
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX(1)
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0xXX(1)
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX(1)
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00

Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 50FF	Reserved area (12 bytes)			
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07
0x00 5206		SPI_RXCRCR	SPI Rx CRC register	0xFF
0x00 5207		SPI_TXCRCR	SPI Tx CRC register	0xFF
0x00 5208 to 0x00 520F	Reserved area (8 bytes)			
0x00 5210	I2C	I2C_CR1	I2C control register 1	0x00
0x00 5211		I2C_CR2	I2C control register 2	0x00
0x00 5212		I2C_FREQR	I2C frequency register	0x00
0x00 5213		I2C_OARL	I2C own address register low	0x00
0x00 5214		I2C_OARH	I2C own address register high	0x00
0x00 5215		Reserved area (1 byte)		
0x00 5216		I2C_DR	I2C data register	0x00
0x00 5217		I2C_SR1	I2C status register 1	0x00
0x00 5218		I2C_SR2	I2C status register 2	0x00
0x00 5219		I2C_SR3	I2C status register 3	0x00
0x00 521A		I2C_ITR	I2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I2C clock control register low	0x00
0x00 521C		I2C_CCRH	I2C clock control register high	0x00
0x00 521D		I2C_TRISER	I2C TRISE register	0x02
0x00 521E to 0x00 523F	Reserved area (24 bytes)			

Table 12. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F81 to 0x00 7F8F	Reserved area (15 bytes)			
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM debug module control register 1	0x00
0x00 7F97		DM_CR2	DM debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 bytes)			

1. Accessible by debug module only
2. Product dependent value, see *Figure 5: Register and memory map of STM8A products*.

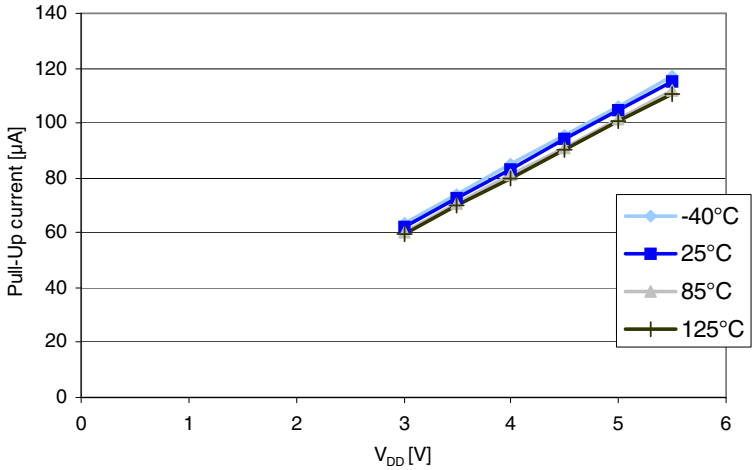
Table 13. Temporary memory unprotection registers

Address	Block	Register label	Register name	Reset status
0x00 5800	TMU	TMU_K1	Temporary memory unprotection key register 1	0x00
0x00 5801		TMU_K2	Temporary memory unprotection key register 2	0x00
0x00 5802		TMU_K3	Temporary memory unprotection key register 3	0x00
0x00 5803		TMU_K4	Temporary memory unprotection key register 4	0x00
0x00 5804		TMU_K5	Temporary memory unprotection key register 5	0x00
0x00 5805		TMU_K6	Temporary memory unprotection key register 6	0x00
0x00 5806		TMU_K7	Temporary memory unprotection key register 7	0x00
0x00 5807		TMU_K8	Temporary memory unprotection key register 8	0x00
0x00 5808		TMU_CSR	Temporary memory unprotection control and status register	0x00

Table 16. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]: Memory readout protection (ROP)** 0xAA: Enable readout protection (write access via SWIM protocol) *Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[5:0]: User boot code area** 0x00: No UBC, no write-protection 0x01: Page 0 to 1 defined as UBC, memory write-protected 0x02: Page 0 to 3 defined as UBC, memory write-protected 0x03 to 0x3F: Pages 4 to 63 defined as UBC, memory write-protected *Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM write protection for more details.*
OPT2	**AFR7: Alternate function remapping option 7** 0: Port D4 alternate function = TIM2_CH1 1: Port D4 alternate function = BEEP **AFR6: Alternate function remapping option 6** 0: Port B5 alternate function = AIN5, port B4 alternate function = AIN4 1: Port B5 alternate function = I^2C_SDA, port B4 alternate function = I^2C_SCL. **AFR5: Alternate function remapping option 5** 0: Port B3 alternate function = AIN3, port B2 alternate function = AIN2, port B1 alternate function = AIN1, port B0 alternate function = AIN0. 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_CH3N, port B1 alternate function = TIM1_CH2N, port B0 alternate function = TIM1_CH1N. **AFR4: Alternate function remapping option 4** Reserved, bit must be kept at “0” **AFR3: Alternate function remapping option 3** 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = TIM1_BKIN **AFR2: Alternate function remapping option 2** 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = CLK_CCO *Note: AFR2 option has priority over AFR3 if both are activated* **AFR1: Alternate function remapping option 1** 0: Port A3 alternate function = TIM2_CH3, port D2 alternate function TIM3_CH1. 1: Port A3 alternate function = TIM3_CH1, port D2 alternate function TIM2_CH3. **AFR0: Alternate function remapping option 0** 0: Port D3 alternate function = TIM2_CH2 1: Port D3 alternate function = ADC_ETR

Figure 22. Typical pull-up current I_{pu} vs V_{DD} @ four temperatures



Note: The pull-up is a pure resistor (slope goes through 0).

Typical output level curves

Figure 23 to *Figure 32* show typical output level curves measured with output on a single pin.

Figure 23. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)

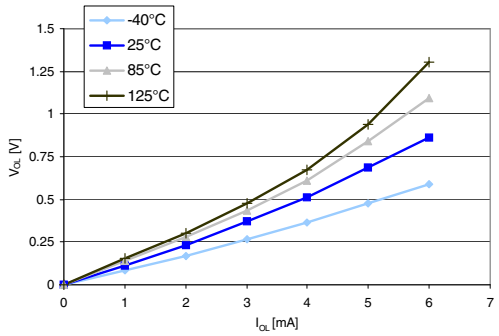


Figure 24. Typ. V_{OL} @ V_{DD} = 5.0 V (standard ports)

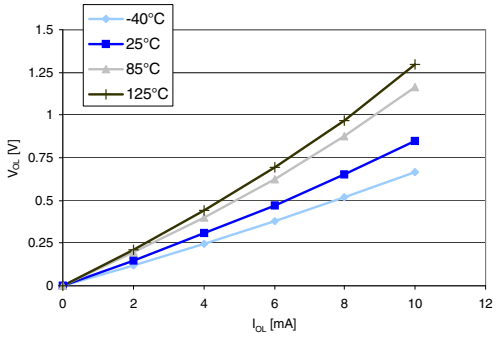


Figure 25. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports)

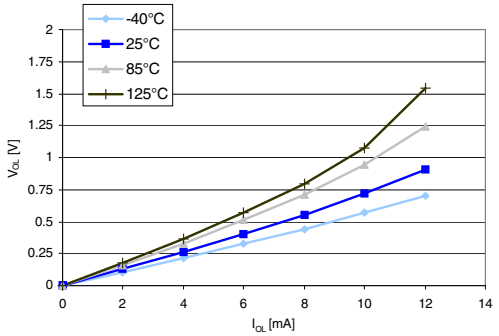


Figure 26. Typ. V_{OL} @ V_{DD} = 5.0 V (true open drain ports)

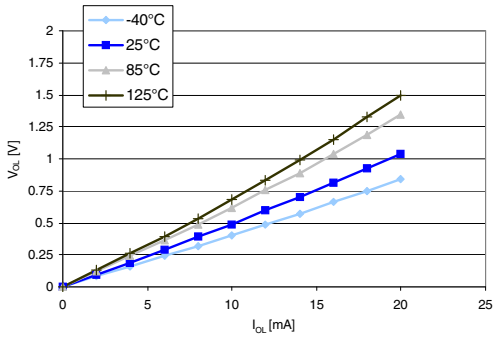


Figure 27. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports)

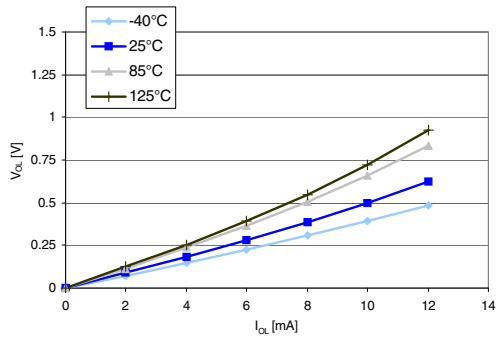


Figure 28. Typ. V_{OL} @ V_{DD} = 5.0 V (high sink ports)

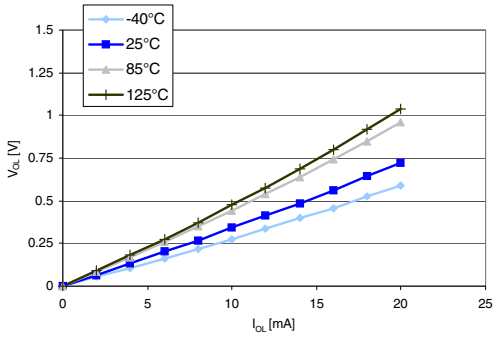


Figure 29. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports)

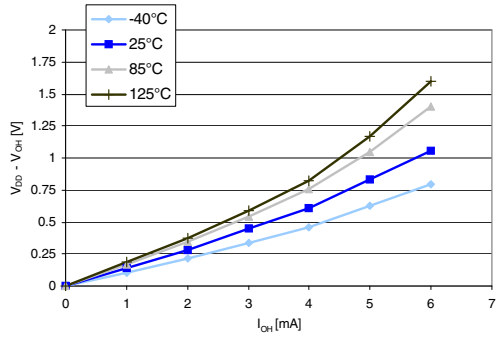


Figure 30. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (standard ports)

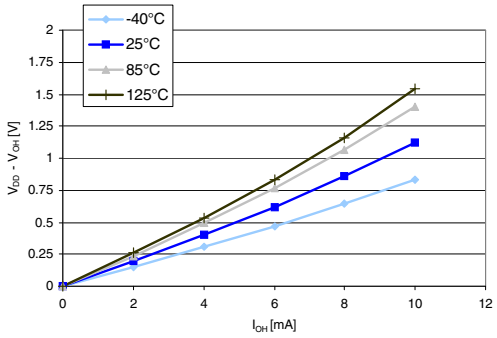


Figure 31. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports)

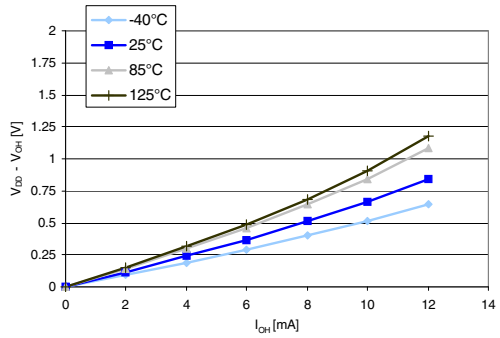
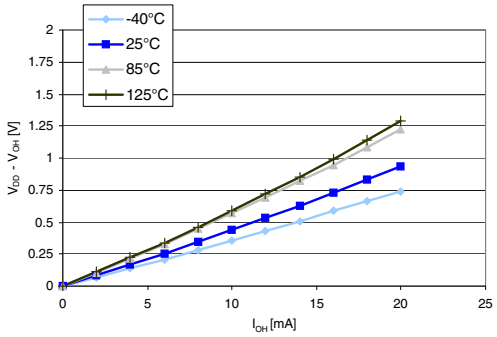
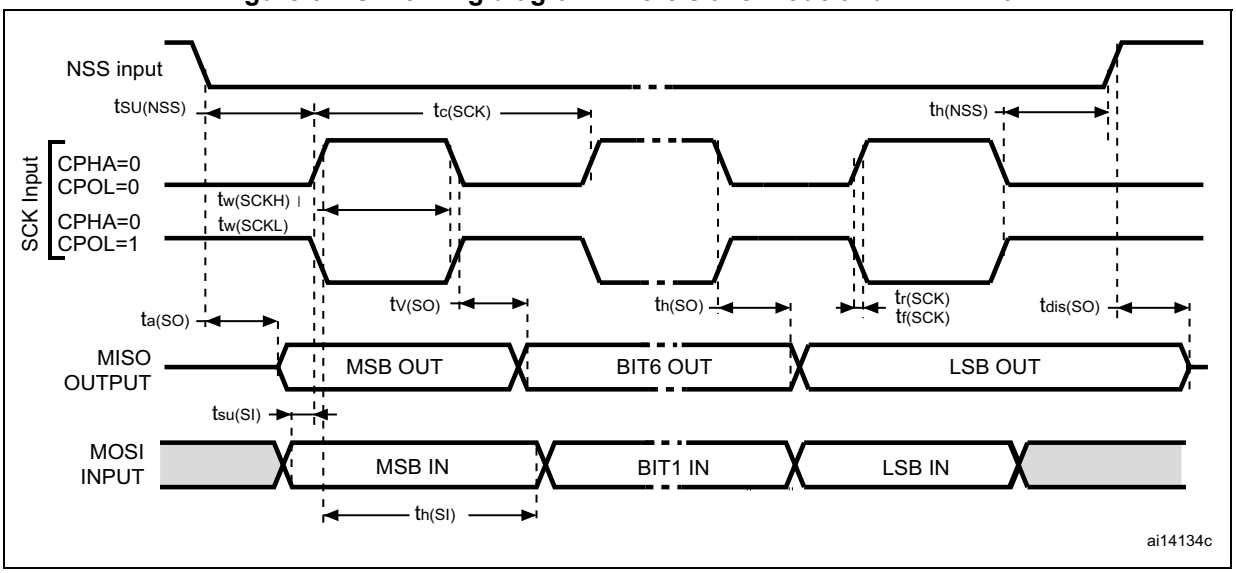


Figure 32. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (high sink ports)



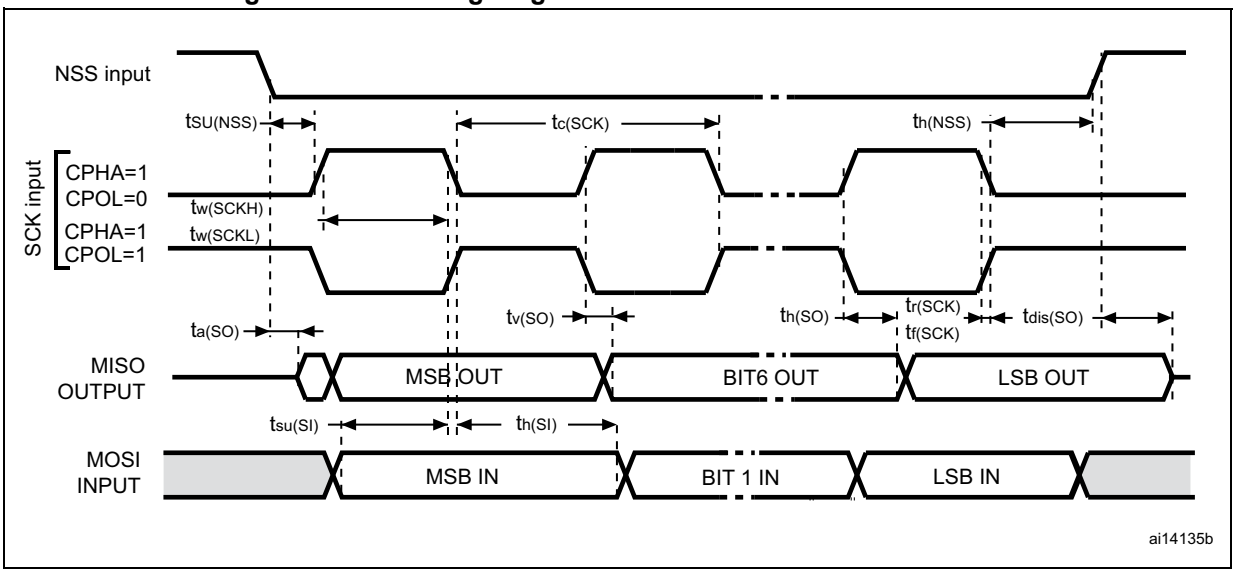
3. Values based on design simulation and/or characterization results, and not tested in production.
4. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
5. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 37. SPI timing diagram where slave mode and CPHA = 0



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 38. SPI timing diagram where slave mode and CPHA = 1

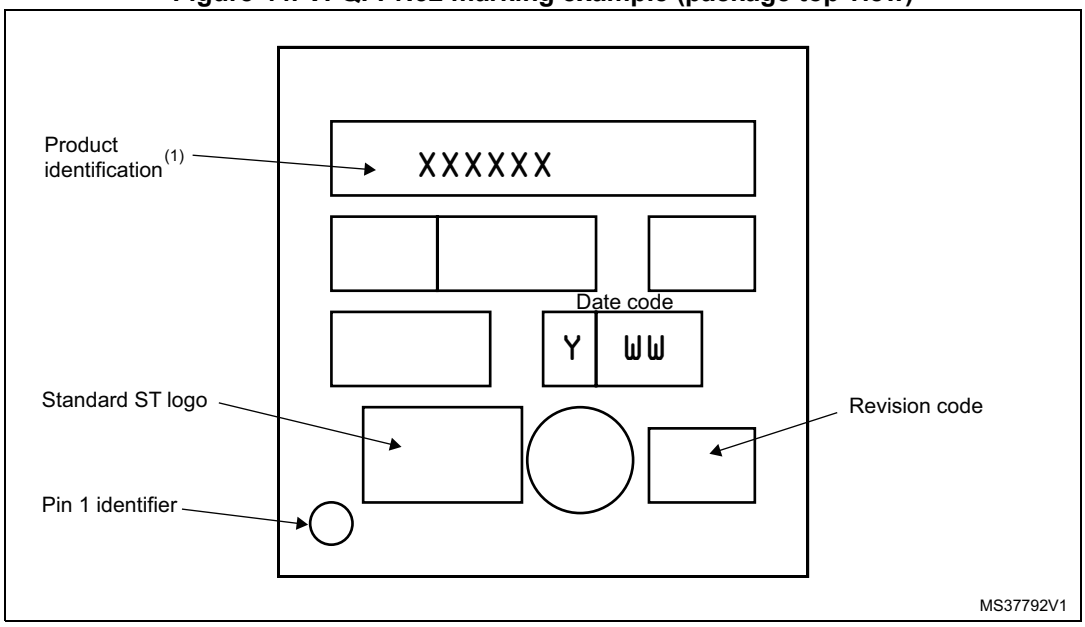


1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Device marking

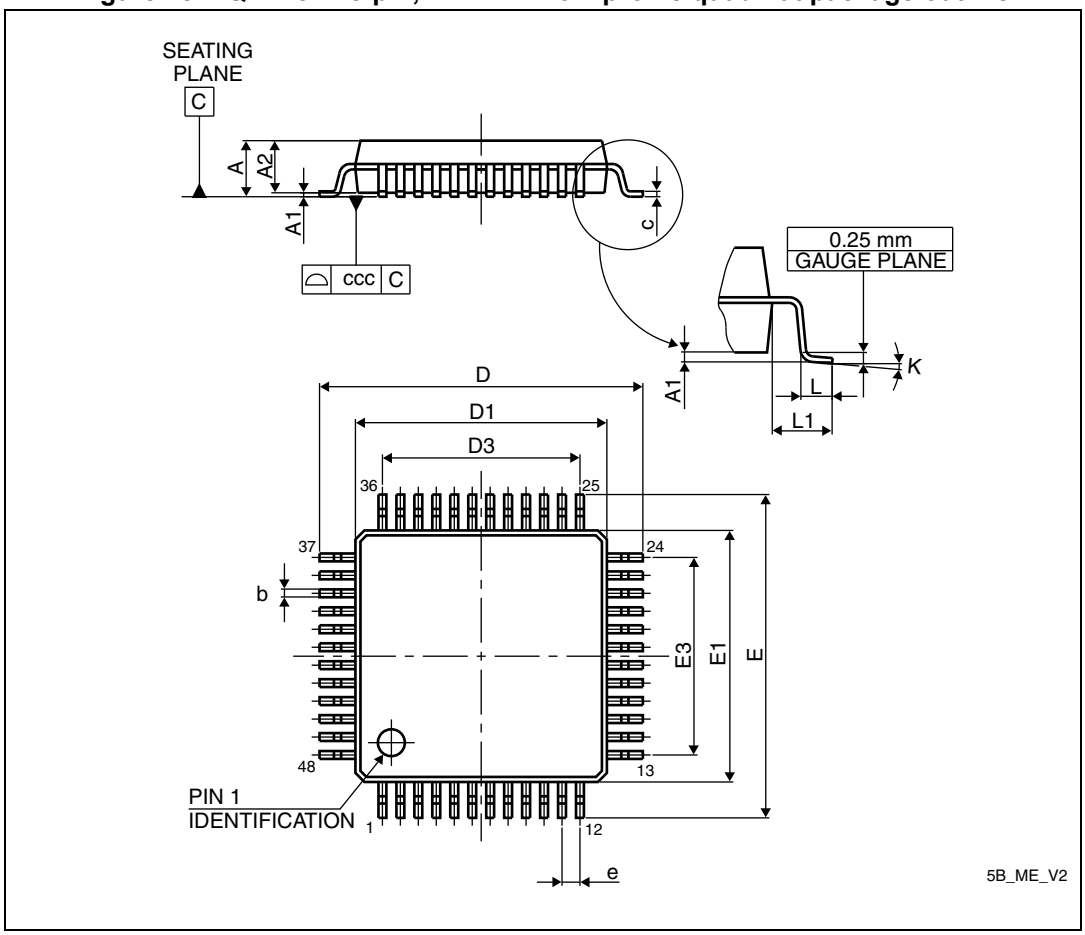
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 44. VFQFPN32 marking example (package top view)



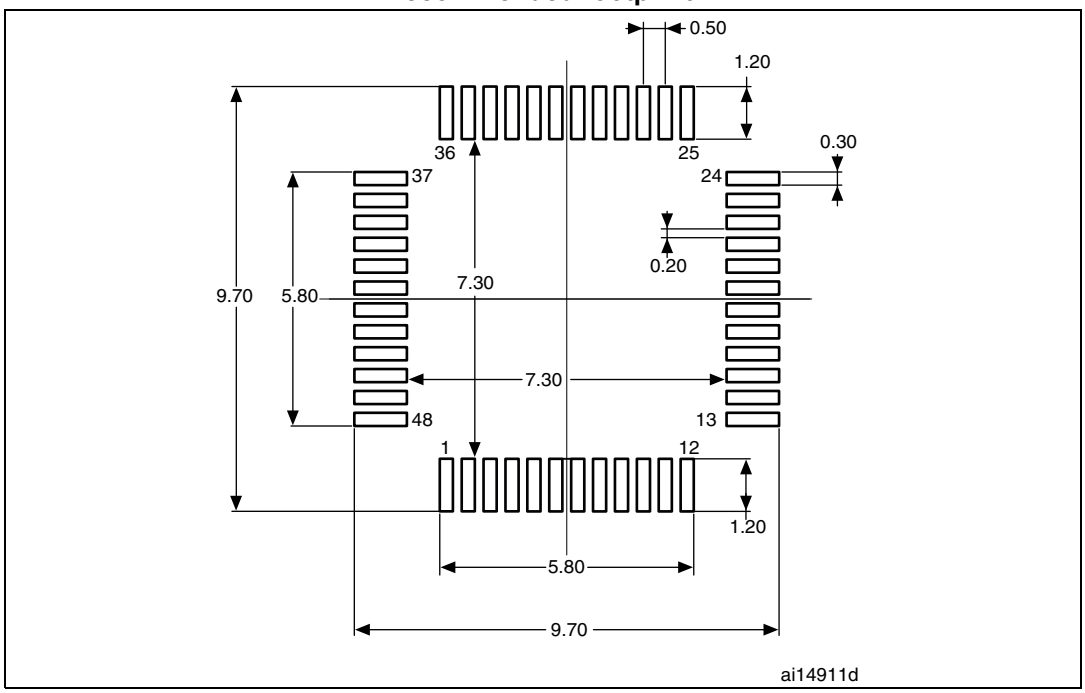
11.2 LQFP48 package information

Figure 45. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Figure 46. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 47. LQFP48 marking example (package top view)

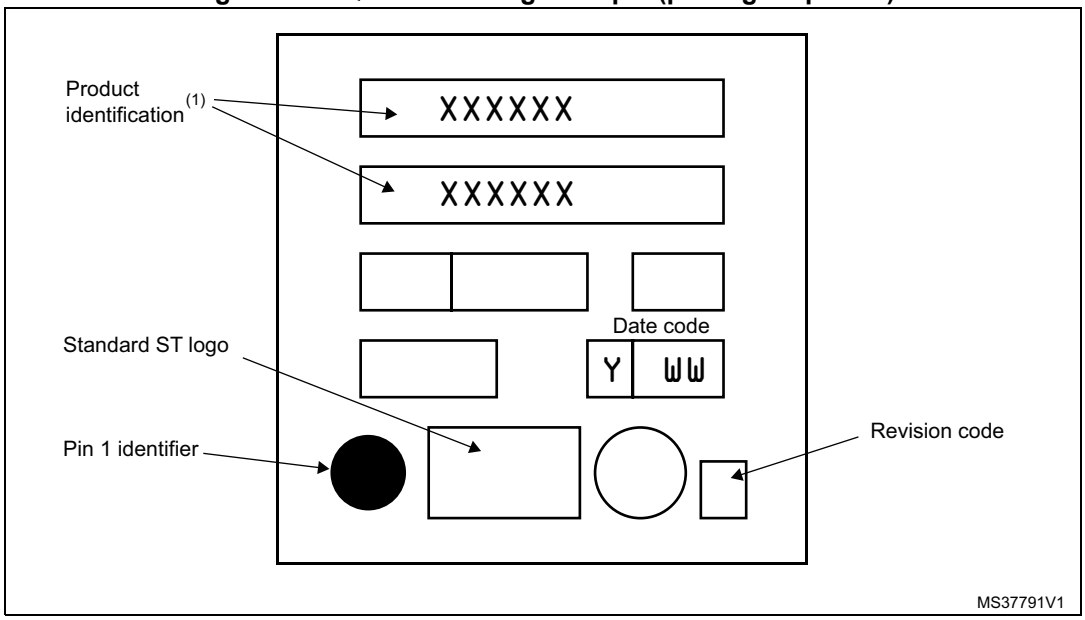
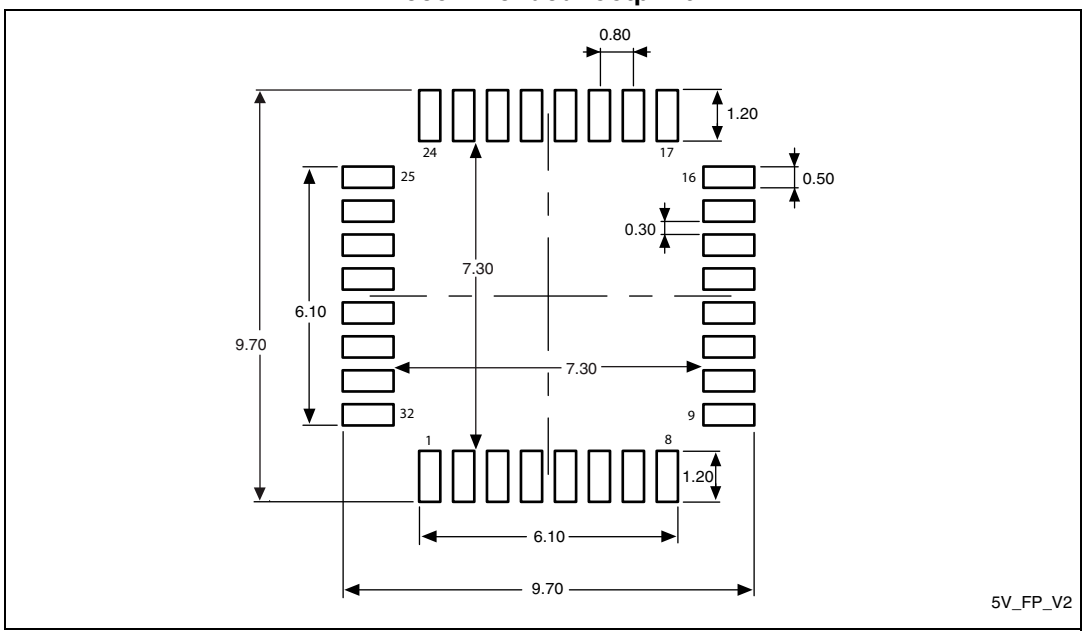


Figure 49. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint

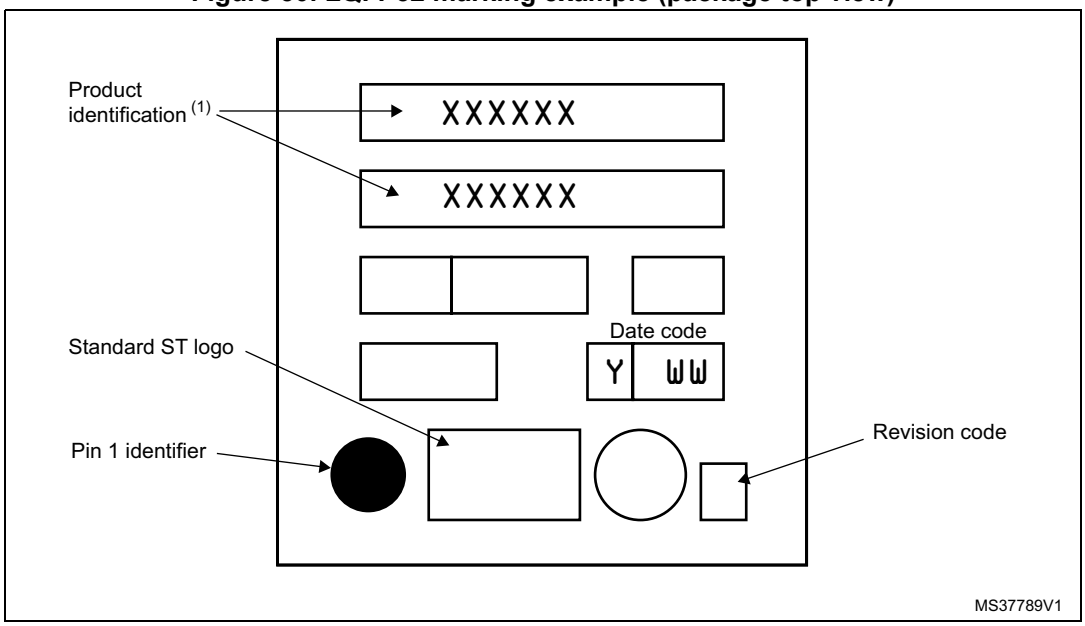


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 50. LQFP32 marking example (package top view)



11.4 Thermal characteristics

In case the maximum chip junction temperature (T_{Jmax}) specified in *Table 21: General operating conditions on page 52* is exceeded, the functionality of the device cannot be guaranteed.

T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 49. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm	57	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	59	°C/W
Θ_{JA}	Thermal resistance junction-ambient VFQFPN32	25	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

11.4.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

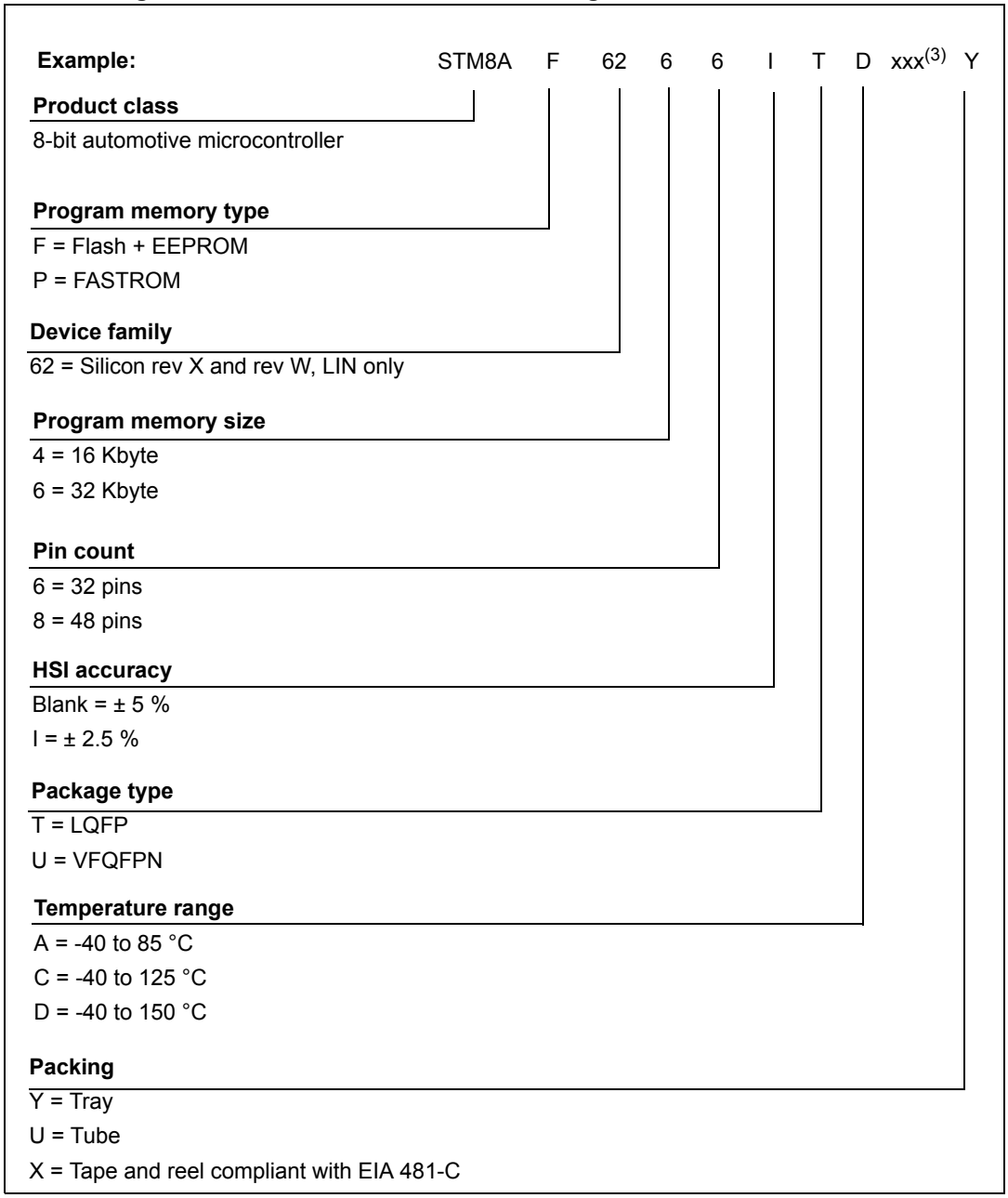
11.4.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see *Section 12: Ordering information*).

The following example shows how to calculate the temperature range needed for a given application.

12 Ordering information

Figure 51. STM8AF6246/48/66/68 ordering information scheme(1) (2)



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the nearest ST Sales Office.
2. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.
3. Customer specific FASTROM code or custom device configuration. This field shows ‘SSS’ if the device contains a super set silicon, usually equipped with bigger memory and more I/Os. This silicon is supposed to be replaced later by the target silicon.

13.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST visual develop (STVD) IDE and the ST visual programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8.

13.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at www.st.com. This package includes:

ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8A microcontroller Flash memory. STVP also offers project mode for saving programming configurations and automating programming sequences.

13.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of the application directly from an easy-to-use graphical interface.

Available toolchains include:

C compiler for STM8

All compilers are available in free version with a limited code size depending on the compiler. For more information, refer to www.cosmic-software.com, www.raisonance.com, and www.iar.com.

STM8 assembler linker

Free assembly toolchain included in the STM8 toolset, which allows users to assemble and link the application source code.