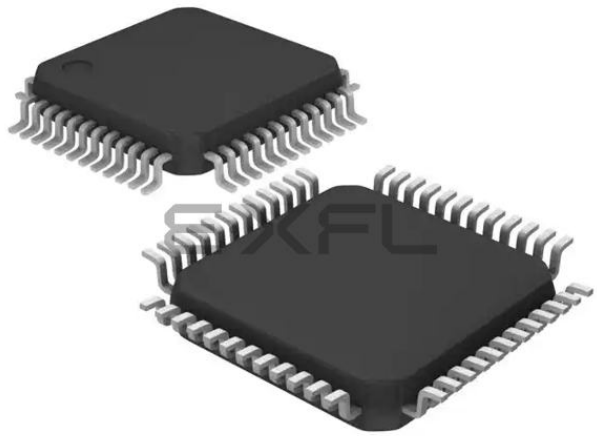

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6248tdy

1 Introduction

This datasheet refers to the STM8AF6246, STM8AF6248, STM8AF6266 and STM8AF6268 products with 16 to 32 Kbyte of Flash program memory.

In the order code, the letter ‘F’ refers to product versions with data EEPROM and ‘H’ refers to product versions without data EEPROM. The identifiers ‘F’ and ‘H’ do not coexist in a given order code.

The datasheet contains the description of family features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8A microcontroller memory, registers and peripherals, please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8 Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

3 Product line-up

Table 1. STM8AF6246/48/66/68 product line-up

Order code	Package	Medium density Flash program memory (byte)	RAM (byte)	Data EE (byte)	10-bit A/D ch.	Timers (IC/OC/PWM)	Serial interfaces	I/0 wakeup pins
STM8AF/P6268	LQFP48 (7x7)	32 K	2 K	1 K	10	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	LIN(UART), SPI, I²C	38/35
STM8AF/P6248		16 K		0.5 K				
STM8AF/P6266	LQFP32 (7x7)	32 K		1 K	7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	LIN(UART), SPI, I²C	25/23
STM8AF/P6246		16 K		0.5 K				
STM8AF/P6266	VFQFPN32	32 K		1 K	7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	LIN(UART), SPI, I²C	25/23
STM8AF/P6246		16 K		0.5 K				

5.4.2 Write protection (WP)

Write protection in application mode is intended to avoid unintentional overwriting of the memory. The write protection can be removed temporarily by executing a specific sequence in the user software.

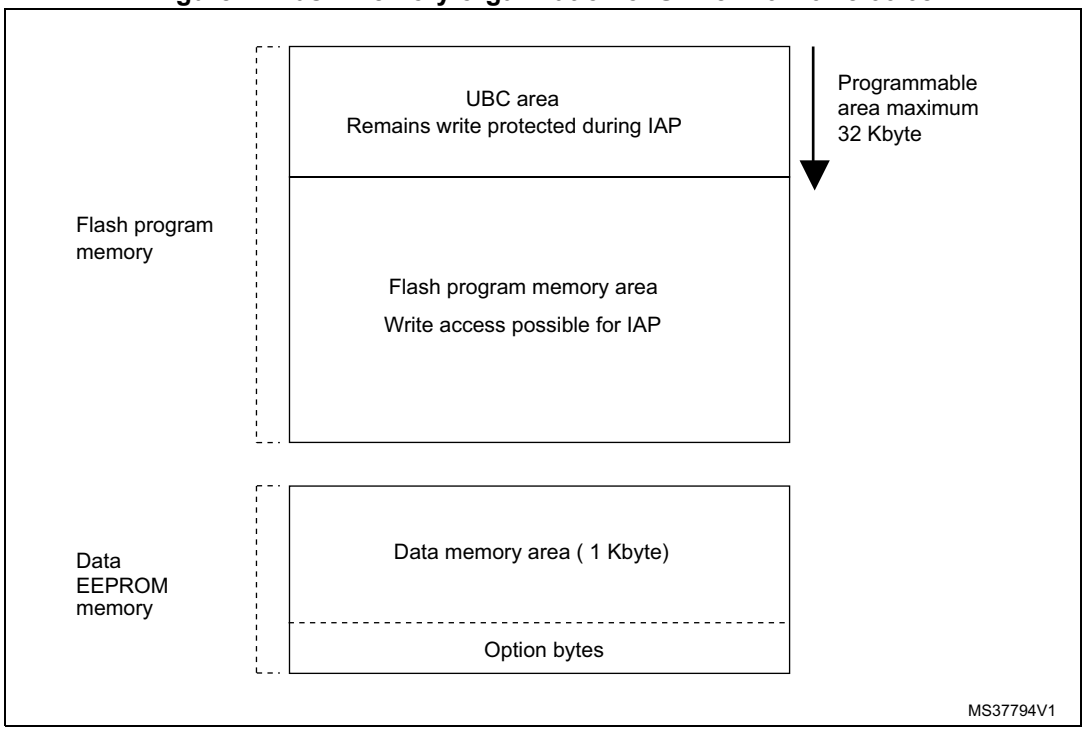
5.4.3 Protection of user boot code (UBC)

If the user chooses to update the Flash program memory using a specific boot code to perform in application programming (IAP), this boot code needs to be protected against unwanted modification.

In the STM8A a memory area of up to 32 Kbyte can be protected from overwriting at user option level. Other than the standard write protection, the UBC protection can exclusively be modified via the debug interface, the user software cannot modify the UBC protection status.

The UBC memory area contains the reset and interrupt vectors and its size can be adjusted in increments of 512 bytes by programming the UBC and NUBC option bytes (see *Section 9: Option bytes on page 44*).

Figure 2. Flash memory organization of STM8AF6246/48/66/68



5.4.4 Read-out protection (ROP)

The STM8A provides a read-out protection of the code and data memory which can be activated by an option byte setting (see the ROP option byte in section 10).

The read-out protection prevents reading and writing Flash program memory, data memory and option bytes via the debug module and SWIM interface. This protection is active in all device operation modes. Any attempt to remove the protection by overwriting the ROP option byte triggers a global erase of the program and data memory.

The ROP circuit may provide a temporary access for debugging or failure analysis. The temporary read access is protected by a user defined, 8-byte keyword stored in the option bytes area. This keyword must be entered via the SWIM interface to temporarily unlock the device.

If desired, the temporary unlock mechanism can be permanently disabled by the user through OPT6/NOPT6 option bytes.

5.5 Clock controller

The clock controller distributes the system clock coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

5.5.1 Features

- **Clock sources**
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
  - 1-16 MHz high-speed external crystal (HSE)
  - Up to 16 MHz high-speed user-external clock (HSE user-ext)
- **Reset**: After reset the microcontroller restarts by default with an internal 2-MHz clock (16 MHz/8). The clock source and speed can be changed by the application program as soon as the code execution starts.
- **Safe clock switching**: Clock sources can be changed safely on the fly in Run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management**: To reduce power consumption, the clock controller can stop the clock to the core or individual peripherals.
- **Wakeup**: In case the device wakes up from low-power modes, the internal RC oscillator (16 MHz/8) is used for quick startup. After a stabilization time, the device switches to the clock source that was selected before Halt mode was entered.
- **Clock security system (CSS)**: The CSS permits monitoring of external clock sources and automatic switching to the internal RC (16 MHz/8) in case of a clock failure.
- **Configurable main clock output (CCO)**: This feature permits to output a clock signal for use by the application.

5.5.2 16 MHz high-speed internal RC oscillator (HSI)

- Default clock after reset 2 MHz (16 MHz/8)
- Fast wakeup time

User trimming

The register CLK_HSITRIMR with three trimming bits plus one additional bit for the sign permits frequency tuning by the application program. The adjustment range covers all possible frequency variations versus supply voltage and temperature. This trimming does not change the initial production setting.

For reason of compatibility with other devices from the STM8A family, a special mode with only two trimming bits plus sign can be selected. This selection is controlled with the HSITRIM0 bit in the option byte registers OPT3 and NOPT3.

5.5.3 128 kHz low-speed internal RC oscillator (LSI)

The frequency of this clock is 128 kHz and it is independent from the main clock. It drives the independent watchdog or the AWU wakeup timer.

In systems which do not need independent clock sources for the watchdog counters, the 128 kHz signal can be used as the system clock. This configuration has to be enabled by setting an option byte (OPT3/OPT3N, bit LSI_EN).

5.5.4 16 MHz high-speed external crystal oscillator (HSE)

The external high-speed crystal oscillator can be selected to deliver the main clock in normal Run mode. It operates with quartz crystals and ceramic resonators.

- Frequency range: 1 MHz to 16 MHz
- Crystal oscillation mode: preferred fundamental
- I/Os: standard I/O pins multiplexed with OSCIN, OSCOUT

5.5.5 External clock input

An external clock signal can be applied to the OSCIN input pin of the crystal oscillator. The frequency range is 0 to 16 MHz.

5.5.6 Clock security system (CSS)

The clock security system protects against a system stall in case of an external crystal clock failure.

In case of a clock failure an interrupt is generated and the high-speed internal clock (HSI) is automatically selected with a frequency of 2 MHz (16 MHz/8).

Table 2. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers

Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock
PCKEN17	TIM1	PCKEN13	LINUART	PCKEN27	Reserved	PCKEN23	ADC
PCKEN16	TIM3	PCKEN12	Reserved	PCKEN26	Reserved	PCKEN22	AWU
PCKEN15	TIM2	PCKEN11	SPI	PCKEN25	Reserved	PCKEN21	Reserved
PCKEN14	TIM4	PCKEN10	I^2C	PCKEN24	Reserved	PCKEN20	Reserved

Table 8. STM8AF6246/48/66/68 (32 Kbyte) microcontroller pin description(1)(2)

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	VFQFPN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
2	2	PA1/OSCIN(3)	I/O	**X**	X	-	-	O1	X	X	**Port A1**	Resonator/crystal in	-
3	3	PA2/OSCOUT	I/O	**X**	X	X	-	O1	X	X	**Port A2**	Resonator/crystal out	-
4	-	V_{SSIO_1}	S	-	-	-	-	-	-	-	I/O ground		-
5	4	V_{SS}	S	-	-	-	-	-	-	-	Digital ground		-
6	5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
7	6	V_{DD}	S	-	-	-	-	-	-	-	Digital power supply		-
8	7	V_{DDIO_1}	S	-	-	-	-	-	-	-	I/O power supply		-
-	8	PF4/AIN12(4)(5)	I/O	**X**	X		-	O1	X	X	**Port F4**	Analog input 12	-
9	-	PA3/TIM2_CH3	I/O	**X**	X	X	-	O1	X	X	**Port A3**	Timer 2 - channel 3	TIM3_CH1 [AFR1]
10	-	PA4	I/O	**X**	X	X	-	O3	X	X	**Port A4**		-
11	-	PA5	I/O	**X**	X	X	-	O3	X	X	**Port A5**		-
12	-	PA6	I/O	**X**	X	X	-	O3	X	X	**Port A6**		-
13	9	V_{DDA}	S	-	-	-	-	-	-	-	Analog power supply		-
14	10	V_{SSA}	S	-	-	-	-	-	-	-	Analog ground		-
15	-	PB7/AIN7	I/O	**X**	X	X	-	O1	X	X	**Port B7**	Analog input 7	-
16	-	PB6/AIN6	I/O	**X**	X	X	-	O1	X	X	**Port B6**	Analog input 6	-
17	11	PB5/AIN5	I/O	**X**	X	X	-	O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
18	12	PB4/AIN4	I/O	**X**	X	X	-	O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]
19	13	PB3/AIN3	I/O	**X**	X	X	-	O1	X	X	**Port B3**	Analog input 3	TIM1_ETR [AFR5]
20	14	PB2/AIN2	I/O	**X**	X	X	-	O1	X	X	**Port B2**	Analog input	TIM1_NCC3 [AFR5]
21	15	PB1/AIN1	I/O	**X**	X	X	-	O1	X	X	**Port B1**	Analog input 1	TIM1_NCC2 [AFR5]
22	16	PB0/AIN0	I/O	**X**	X	X	-	O1	X	X	**Port B0**	Analog input 0	TIM1_NCC1 [AFR5]
23	-	PE7/AIN8	I/O	**X**	X		-	O1	X	X	**Port E7**	Analog input 8	-

Table 8. STM8AF6246/48/66/68 (32 Kbyte) microcontroller pin description(1)(2) (continued)

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	VFQFPN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
47	31	PD6/ LINUART_RX	I/O	**X**	X	X	-	O1	X	X	**Port D6**	LINUART data receive	-
48	32	PD7/TLI(8)	I/O	**X**	X	X	-	O1	X	X	**Port D7**	Top level interrupt	-

1. Refer to *Table 7* for the definition of the abbreviations.
2. Reset state is shown in bold.
3. In Halt/Active-halt mode this pad behaves in the following way:
   - the input/output path is disabled
   - if the HSE clock is used for wakeup, the internal weak pull up is disabled
   - if the HSE clock is off, internal weak pull up setting from corresponding OR bit is used
   By managing the OR bit correctly, it must be ensured that the pad is not left floating during Halt/Active-halt.
4. On this pin, a pull-up resistor as specified in *Table 35*. I/O static characteristics is enabled during the reset phase of the product.
5. AIN12 is not selectable in ADC scan mode or with analog watchdog.
6. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, week pull-up, and protection diode to V_{DD} are not implemented)
7. The PD1 pin is in input pull-up during the reset phase and after reset release.
8. If this pin is configured as interrupt pin, it will trigger the TLI.

6.2 Alternate function remapping

As shown in the rightmost column of *Table 8*, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. Refer to *Section 9: Option bytes on page 44*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016).

Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5314	TIM2	TIM2_CCR3L	TIM2 capture/compare register 3 low	0x00
0x00 5315 to 0x00 531F	Reserved area (11 bytes)			
0x00 5320	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5321		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5322		TIM3_SR1	TIM3 status register 1	0x00
0x00 5323		TIM3_SR2	TIM3 status register 2	0x00
0x00 5324		TIM3_EGR	TIM3 event generation register	0x00
0x00 5325		TIM3_CCMR1	TIM3 capture/compare mode register 1	0x00
0x00 5326		TIM3_CCMR2	TIM3 capture/compare mode register 2	0x00
0x00 5327		TIM3_CCER1	TIM3 capture/compare enable register 1	0x00
0x00 5328		TIM3_CNTRH	TIM3 counter high	0x00
0x00 5329		TIM3_CNTRL	TIM3 counter low	0x00
0x00 532A		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 532B		TIM3_ARRH	TIM3 auto-reload register high	0xFF
0x00 532C		TIM3_ARRL	TIM3 auto-reload register low	0xFF
0x00 532D		TIM3_CCR1H	TIM3 capture/compare register 1 high	0x00
0x00 532E		TIM3_CCR1L	TIM3 capture/compare register 1 low	0x00
0x00 532F		TIM3_CCR2H	TIM3 capture/compare register 2 high	0x00
0x00 5330		TIM3_CCR2L	TIM3 capture/compare register 2 low	0x00
0x00 5331 to 0x00 533F	Reserved area (15 bytes)			
0x00 5340	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 5341		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 5342		TIM4_SR	TIM4 status register	0x00
0x00 5343		TIM4_EGR	TIM4 event generation register	0x00
0x00 5344		TIM4_CNTR	TIM4 counter	0x00
0x00 5345		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 5346		TIM4_ARR	TIM4 auto-reload register	0xFF
0x00 5347 to 0x00 53DF	Reserved area (185 bytes)			

8 Interrupt table

Table 14. STM8A interrupt table

Priority	Source block	Description	Interrupt vector address	Wakeup from Halt	Comments
-	Reset	Reset	0x00 8000	Yes	User RESET vector
-	TRAP	SW interrupt	0x00 8004	-	-
0	TLI	External top level interrupt	0x00 8008	-	-
1	AWU	Auto-wakeup from Halt	0x00 800C	Yes	-
2	Clock controller	Main clock controller	0x00 8010	-	-
3	MISC	Ext interrupt E0	0x00 8014	Yes	Port A interrupts
4	MISC	Ext interrupt E1	0x00 8018	Yes	Port B interrupts
5	MISC	Ext interrupt E2	0x00 801C	Yes	Port C interrupts
6	MISC	Ext interrupt E3	0x00 8020	Yes	Port D interrupts
7	MISC	Ext interrupt E4	0x00 8024	Yes	Port E interrupts
8	Reserved(1)	-	-	-	-
9	Reserved(1)	-	-	-	-
10	SPI	End of transfer	0x00 8030	Yes	-
11	Timer 1	Update/overflow/ trigger/break	0x00 8034	-	-
12	Timer 1	Capture/compare	0x00 8038	-	-
13	Timer 2	Update/overflow	0x00 803C	-	-
14	Timer 2	Capture/compare	0x00 8040	-	-
15	Timer 3	Update/overflow	0x00 8044	-	-
16	Timer 3	Capture/compare	0x00 8048	-	-
17	Reserved(1)	-	-	-	-
18	Reserved(1)	-	-	-	-
19	I^2C	I^2C interrupts	0x00 8054	Yes	-
20	LINUART	Tx complete/error	0x00 8058	-	-
21	LINUART	Receive data full reg.	0x00 805C	-	-
22	ADC	End of conversion	0x00 8060	-	-
23	Timer 4	Update/overflow	0x00 8064	-	-
24	EEPROM	End of Programming/ Write in not allowed area	0x00 8068	-	-

1. All reserved and unused interrupts must be initialized with ‘IRET’ for robust programming.

Table 15. Option bytes (continued)

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 480B	TMU	OPT6	TMU[3:0]								0x00
0x00 480C		NOPT6	NTMU[3:0]								0xFF
0x00 480D	Flash wait states	OPT7	Reserved							WAIT STATE	0x00
0x00 480E		NOPT7	Reserved							NWAIT STATE	0xFF
0x00 480F	Reserved										
0x00 4810	TMU	OPT8	TMU_KEY 1 [7:0]								0x00
0x00 4811		OPT9	TMU_KEY 2 [7:0]								0x00
0x00 4812		OPT10	TMU_KEY 3 [7:0]								0x00
0x00 4813		OPT11	TMU_KEY 4 [7:0]								0x00
0x00 4814		OPT12	TMU_KEY 5 [7:0]								0x00
0x00 4815		OPT13	TMU_KEY 6 [7:0]								0x00
0x00 4816		OPT14	TMU_KEY 7 [7:0]								0x00
0x00 4817		OPT15	TMU_KEY 8 [7:0]								0x00
0x00 4818		OPT16	TMU_MAXATT [7:0]								0xC7
0x00 4819 to 487D	Reserved										
0x00 487E	Boot-loader(1)	OPT17	BL [7:0]								0x00
0x00 487F		NOPT17	NBL[7:0]								0xFF

1. This option consists of two bytes that must have a complementary value in order to be valid. If the option is invalid, it has no effect on EMC reset.

Figure 12. Typ. $I_{DD(RUN)HSI}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripheral = off

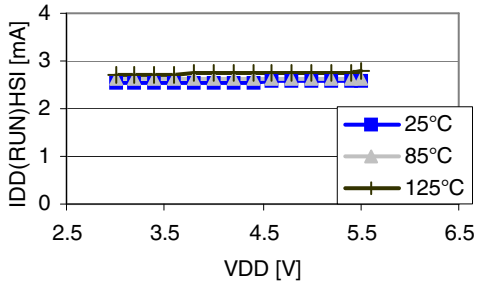


Figure 13. Typ. $I_{DD(WFI)HSE}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripheral = on

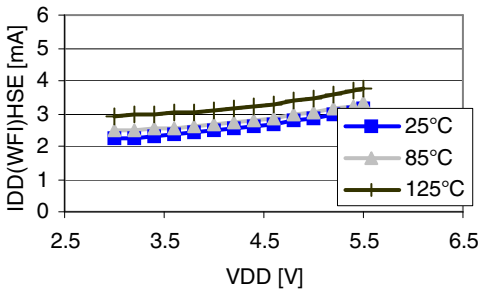


Figure 14. Typ. $I_{DD(WFI)HSE}$ vs. f_{CPU} @ V_{DD} = 5.0 V, peripheral = on

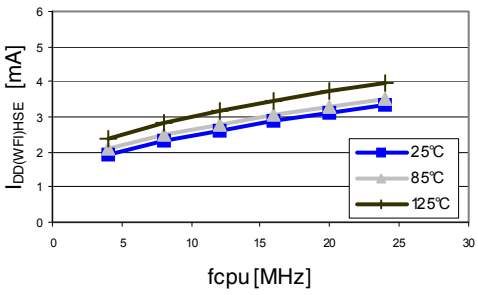
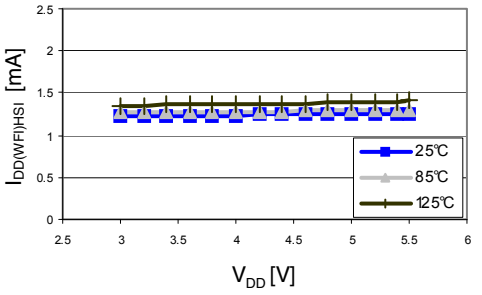


Figure 15. Typ. $I_{DD(WFI)HSI}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripheral = off



10.3.3 External clock sources and timing characteristics

HSE user external clock

Subject to general operating conditions for V_{DD} and T_A.

Table 28. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	T_A is -40 to 150 °C	0(1)	-	16	MHz
V_{HSEdHL}	Comparator hysteresis	-	0.1 x V_{DD}	-	-	V
V_{HSEH}	OSCIN input pin high level voltage	-	0.7 x V_{DD}	-	V_{DD}	
V_{HSEL}	OSCIN input pin low level voltage	-	V_{SS}	-	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	-	+1	µA

1. In CSS is used, the external clock must have a frequency above 500 kHz.

Figure 27. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports)

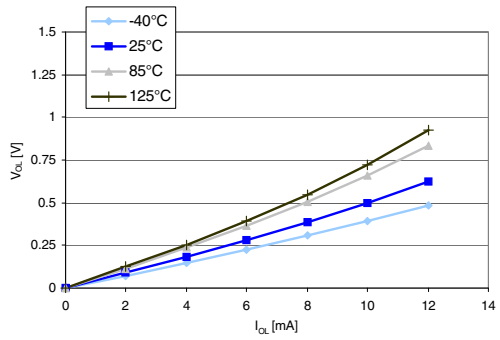


Figure 28. Typ. V_{OL} @ V_{DD} = 5.0 V (high sink ports)

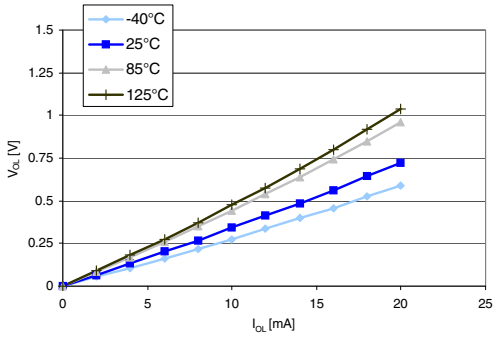


Figure 29. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports)

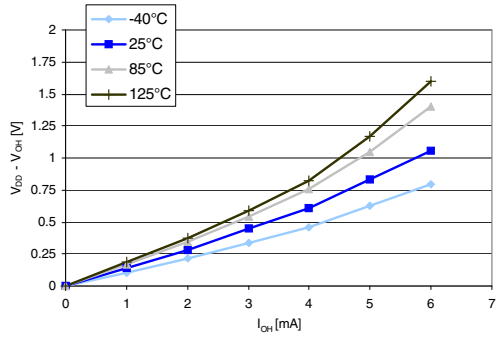


Figure 30. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (standard ports)

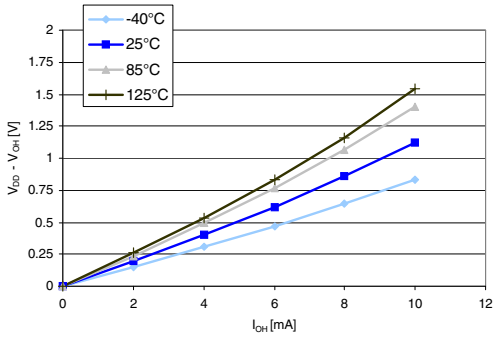


Figure 31. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports)

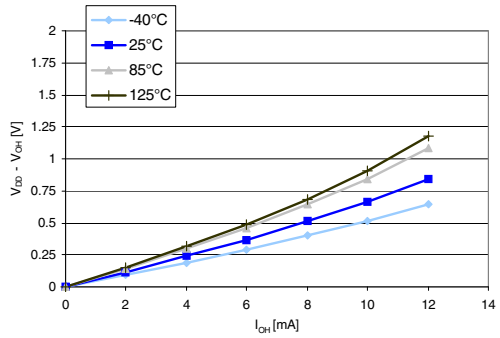


Figure 32. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (high sink ports)

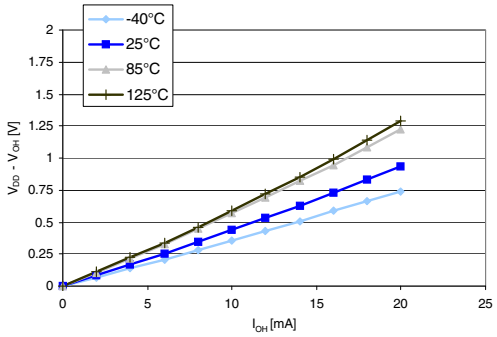


Figure 34. Typical NRST pull-up resistance R_{PU} vs V_{DD}

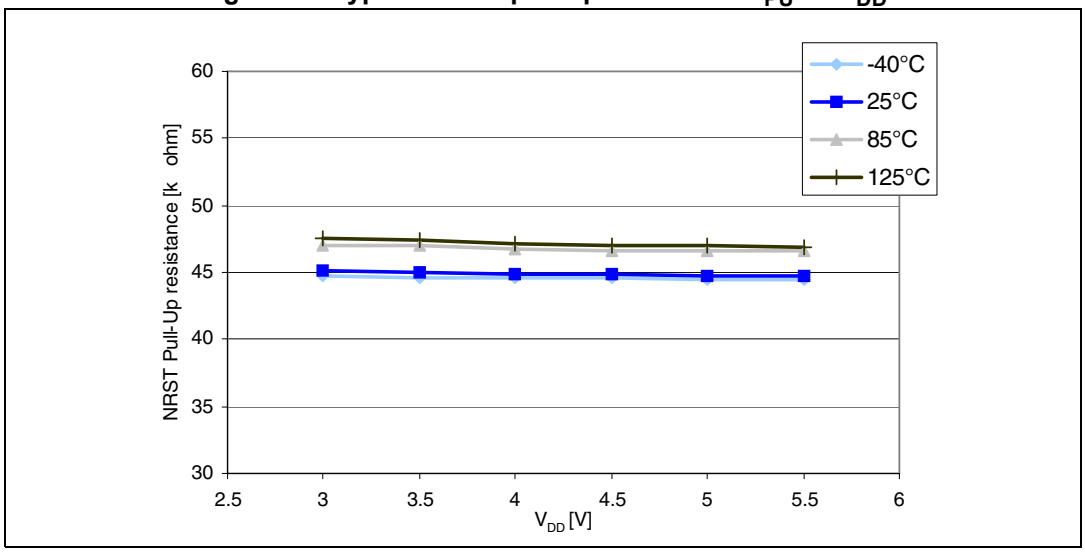
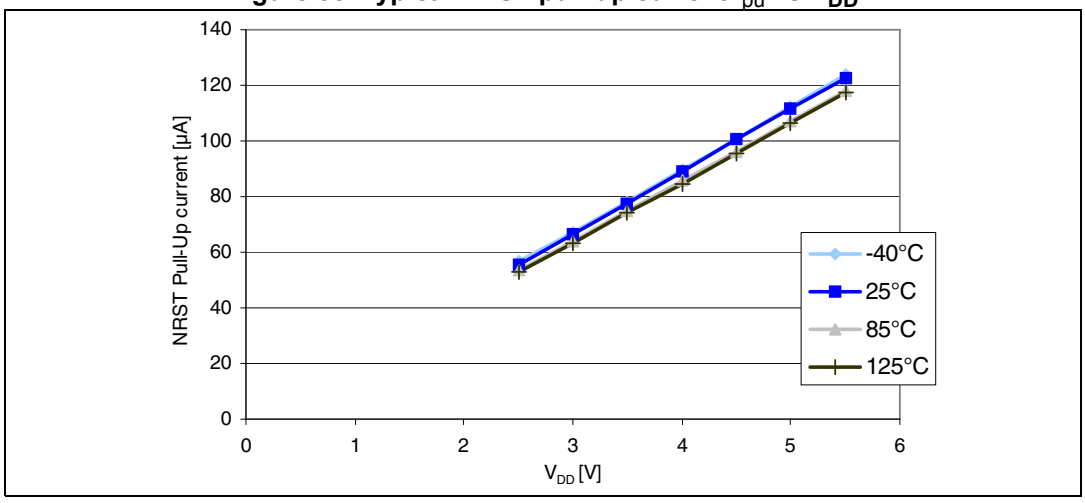


Figure 35. Typical NRST pull-up current I_{pu} vs V_{DD}



The reset network shown in *Figure 36* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below $V_{IL(NRST)}$ max (see *Table 36: NRST pin characteristics*), otherwise the reset is not taken into account internally.

Figure 36. Recommended reset pin protection

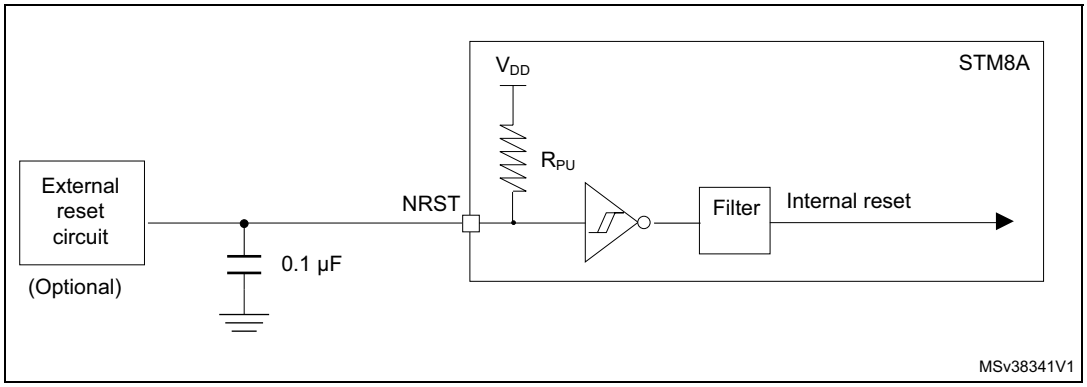
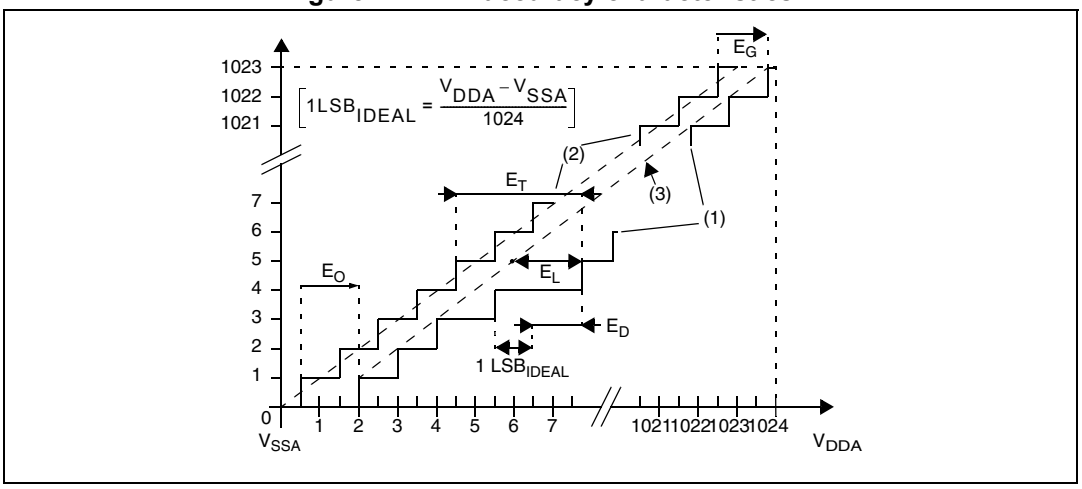


Table 41. ADC accuracy for V_{DDA} = 5 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.4	3(3)	LSB
$\|E_O\|$	Offset error(2)		0.8	3	
$\|E_G\|$	Gain error(2)		0.1	2	
$\|E_D\|$	Differential linearity error(2)		0.9	1	
$\|E_L\|$	Integral linearity error(2)		0.7	1.5	
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 4 MHz	1.9(4)	4(4)	
$\|E_O\|$	Offset error(2)		1.3(4)	4(4)	
$\|E_G\|$	Gain error(2)		0.6(4)	3(4)	
$\|E_D\|$	Differential linearity error(2)		1.5(4)	2(4)	
$\|E_L\|$	Integral linearity error(2)		1.2(4)	1.5(4)	

1. Max value is based on characterization, not tested in production.
2. ADC accuracy vs. injection current: Any positive or negative injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.
3. TUE 2LSB can be reached on specific sales types on the whole temperature range.
4. Target values.

Figure 41. ADC accuracy characteristics



1. Example of an actual transfer curve
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: Maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: Deviation between the first actual transition and the first ideal one.
   E_G = Gain error: Deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: Maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: Maximum deviation between any actual transition and the end point correlation line.

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin) and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

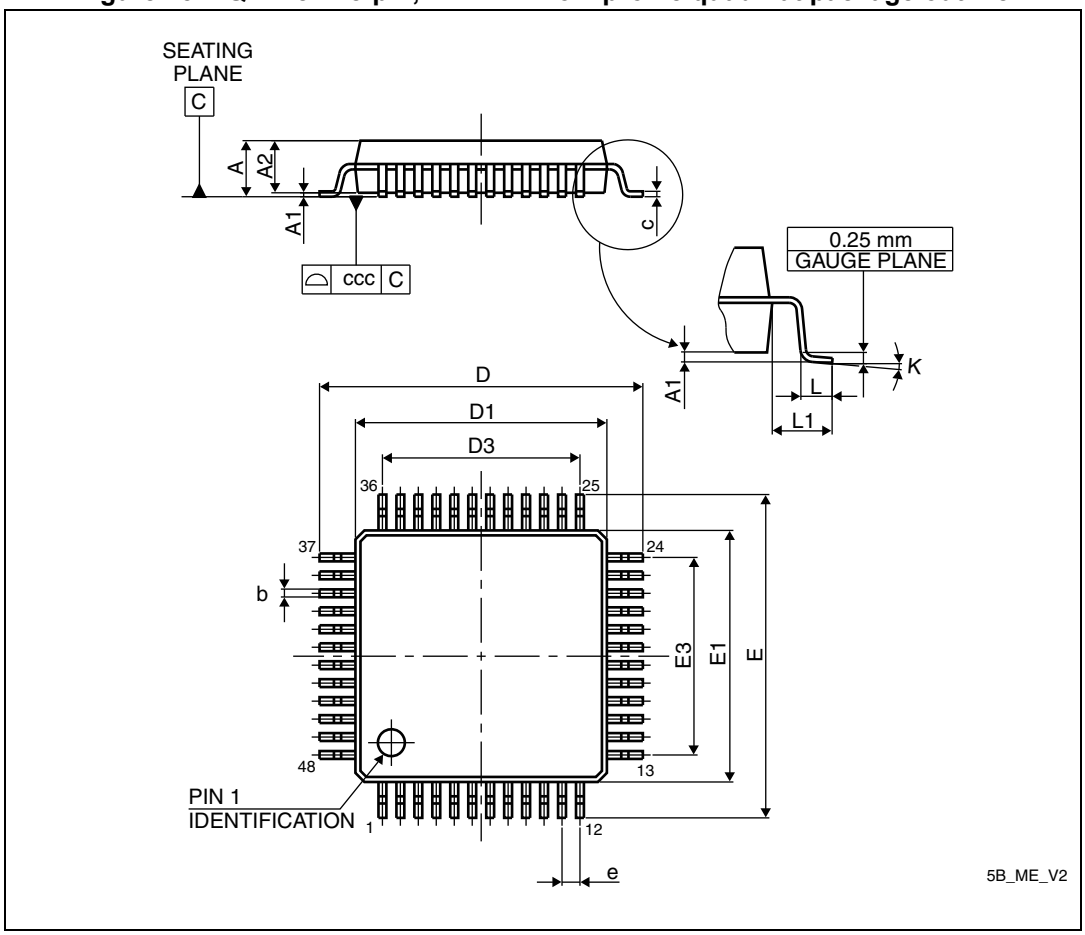
Table 45. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A = 25 °C	A
		T_A = 85 °C	
		T_A = 125 °C	
		T_A = 150 °C	

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

11.2 LQFP48 package information

Figure 45. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 47. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 48. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.