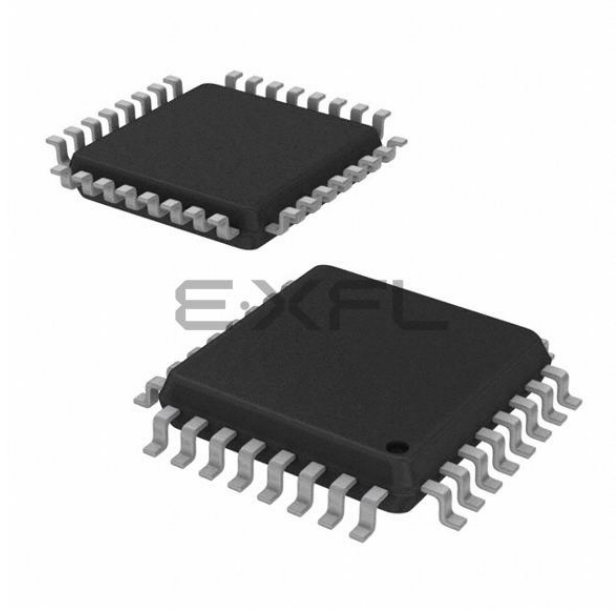

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6266itcx

3 Product line-up

Table 1. STM8AF6246/48/66/68 product line-up

Order code	Package	Medium density Flash program memory (byte)	RAM (byte)	Data EE (byte)	10-bit A/D ch.	Timers (IC/OC/PWM)	Serial interfaces	I/0 wakeup pins
STM8AF/P6268	LQFP48 (7x7)	32 K	2 K	1 K	10	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	LIN(UART), SPI, I²C	38/35
STM8AF/P6248		16 K		0.5 K				
STM8AF/P6266	LQFP32 (7x7)	32 K		1 K	7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	LIN(UART), SPI, I²C	25/23
STM8AF/P6246		16 K		0.5 K				
STM8AF/P6266	VFQFPN32	32 K		1 K	7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	LIN(UART), SPI, I²C	25/23
STM8AF/P6246		16 K		0.5 K				

1. Legend:
   ADC: Analog-to-digital converter
   beCAN: Controller area network
   BOR: Brownout reset
   I²C: Inter-integrated circuit multimaster interface
   IWDG: Independent window watchdog
   LINUART: Local interconnect network universal asynchronous receiver transmitter
   POR: Power on reset
   SPI: Serial peripheral interface
   SWIM: Single wire interface module
   USART: Universal synchronous asynchronous receiver transmitter
   Window WDG: Window watchdog

5.5.2 16 MHz high-speed internal RC oscillator (HSI)

- Default clock after reset 2 MHz (16 MHz/8)
- Fast wakeup time

User trimming

The register CLK_HSITRIMR with three trimming bits plus one additional bit for the sign permits frequency tuning by the application program. The adjustment range covers all possible frequency variations versus supply voltage and temperature. This trimming does not change the initial production setting.

For reason of compatibility with other devices from the STM8A family, a special mode with only two trimming bits plus sign can be selected. This selection is controlled with the HSITRIM0 bit in the option byte registers OPT3 and NOPT3.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure. If the hardware watchdog feature is enabled through the device option bits, the watchdog is automatically enabled at power-on, and generates a reset unless the key register is written by software before the counter reaches the end of count.

5.7.2 Auto-wakeup counter

This counter is used to cyclically wakeup the device in Active-halt mode. It can be clocked by the internal 128 kHz internal low-frequency RC oscillator or external clock.

LSI clock can be internally connected to TIM3 input capture channel 1 for calibration.

5.7.3 Beeper

This function generates a rectangular signal in the range of 1, 2 or 4 kHz which can be output on a pin. This is useful when audible sounds without interference need to be generated for use in the application.

5.7.4 Advanced control and general purpose timers

STM8A devices described in this datasheet, contain up to three 16-bit advanced control and general purpose timers providing nine CAPCOM channels in total. A CAPCOM channel can be used either as input compare, output compare or PWM channel. These timers are named TIM1, TIM2 and TIM3.

Table 3. Advanced control and general purpose timers

Timer	Counter width	Counter type	Prescaler factor	Channels	Inverted outputs	Repetition counter	trigger unit	External trigger	Break input
TIM1	16-bit	Up/down	1 to 65536	4	3	Yes	Yes	Yes	Yes
TIM2	16-bit	Up	2^n n = 0 to 15	3	None	No	No	No	No
TIM3	16-bit	Up	2^n n = 0 to 15	2	None	No	No	No	No

Table 16. Option byte description (continued)

Option byte no.	Description
OPT3	**HSITRIM: Trimming option for 16 MHz internal RC oscillator** 0: 3-bit on-the-fly trimming (compatible with devices based on the 128K silicon) 1: 4-bit on-the-fly trimming
	LSI_EN: Low speed internal clock enable 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: Independent watchdog 0: IWDG independent watchdog activated by software 1: IWDG independent watchdog activated by hardware
	WWDG_HW: Window watchdog activation 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: Window watchdog reset on Halt 0: No reset generated on Halt if WWDG active 1: Reset generated on Halt if WWDG active
OPT4	**EXTCLK: External clock selection** 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: Auto-wakeup unit/clock 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for AWU
	PRSC[1:0]: AWU clock prescaler 00: Reserved 01: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]: HSE crystal oscillator stabilization time** This configures the stabilization time to 0.5, 8, 128, and 2048 HSE cycles with corresponding option byte values of 0xE1, 0xD2, 0xB4, and 0x00.
OPT6	**TMU**[3:0]: Enable temporary memory unprotection 0101: TMU disabled (permanent ROP). Any other value: TMU enabled.
OPT7	**Reserved**
OPT8	**TMU_KEY 1 [7:0]: Temporary unprotection key 0** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT9	**TMU_KEY 2 [7:0]: Temporary unprotection key 1** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT10	**TMU_KEY 3 [7:0]: Temporary unprotection key 2** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT11	**TMU_KEY 4 [7:0]: Temporary unprotection key 3** Temporary unprotection key: Must be different from 0x00 or 0xFF

10 Electrical characteristics

10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = -40 °C, T_A = 25 °C, and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

10.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

10.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

Figure 6. Pin loading conditions

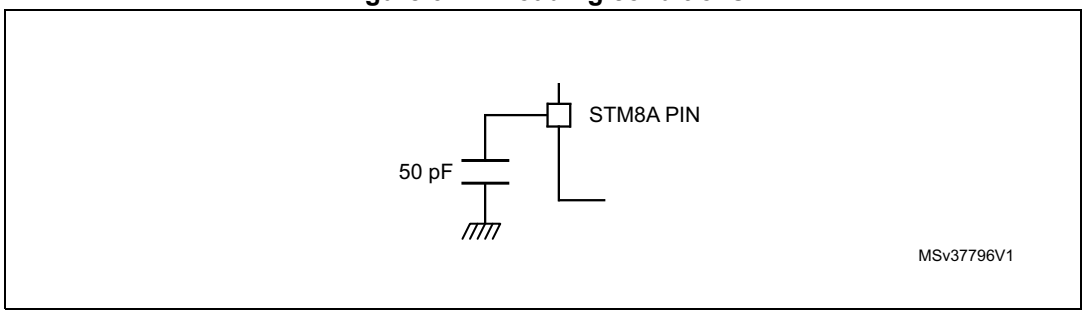


Figure 12. Typ. $I_{DD(RUN)HSI}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripheral = off

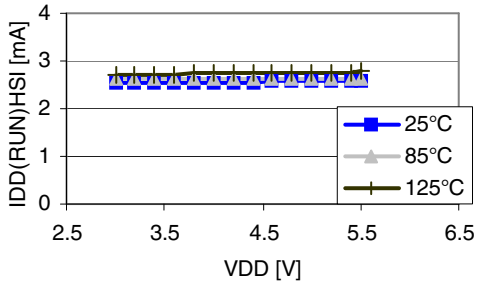


Figure 13. Typ. $I_{DD(WFI)HSE}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripheral = on

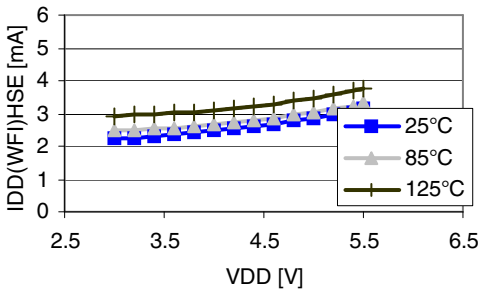


Figure 14. Typ. $I_{DD(WFI)HSE}$ vs. f_{CPU} @ V_{DD} = 5.0 V, peripheral = on

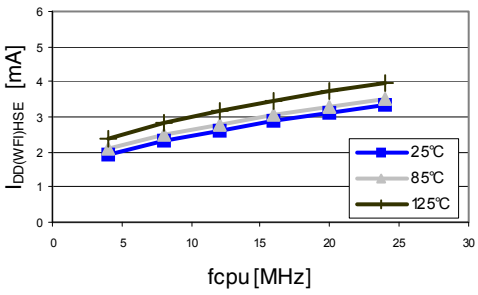
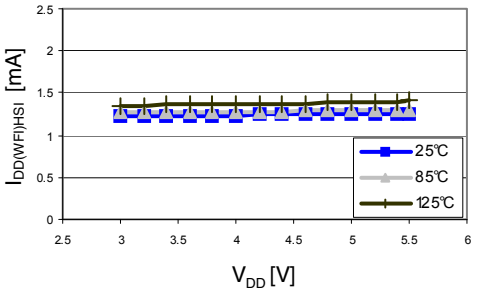


Figure 15. Typ. $I_{DD(WFI)HSI}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripheral = off



10.3.3 External clock sources and timing characteristics

HSE user external clock

Subject to general operating conditions for V_{DD} and T_A.

Table 28. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	T_A is -40 to 150 °C	0(1)	-	16	MHz
V_{HSEdHL}	Comparator hysteresis	-	0.1 x V_{DD}	-	-	V
V_{HSEH}	OSCIN input pin high level voltage	-	0.7 x V_{DD}	-	V_{DD}	
V_{HSEL}	OSCIN input pin low level voltage	-	V_{SS}	-	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	-	+1	µA

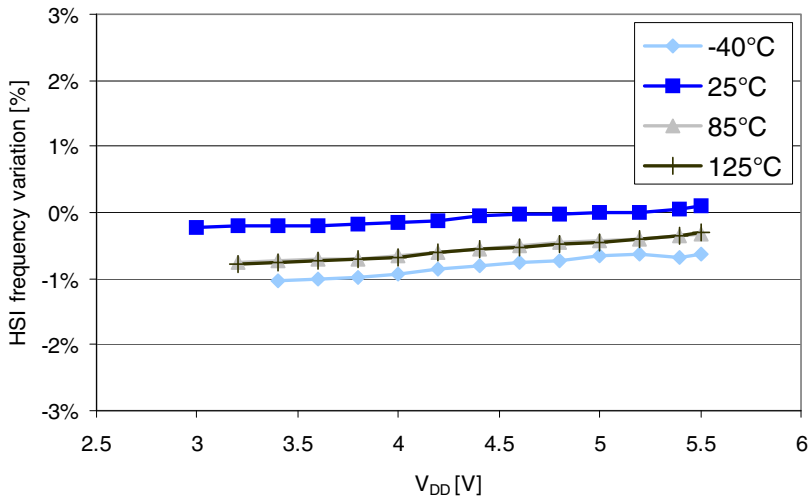
1. In CSS is used, the external clock must have a frequency above 500 kHz.

Table 30. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ACC_{HS}	HSI oscillator user trimming accuracy	Trimmed by the application for any V_{DD} and T_A conditions	-1(1)	-	1(1)	%
			-0.5(1)	-	0.5(1)	
	HSI oscillator accuracy (factory calibrated)	3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 150 °C	-5	-	5	
		3.0V ≤ V_{DD} ≤ 5.5V, -40°C ≤ T_A ≤ 125 °C	-2.5(2)	-	2.5(2)	
$t_{su(HSI)}$	HSI oscillator wakeup time	-	-	-	2(3)	µs

1. Depending on option byte setting (OPT3 and NOPT3)
2. These values are guaranteed for STM8AF62x6ITx order codes only.
3. Guaranteed by characterization, not tested in production

Figure 18. Typical HSI frequency vs V_{DD}



Low speed internal RC oscillator (LSI)

Subject to general operating conditions for V_{DD} and T_A.

Table 31. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	112	128	144	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	7(1)	µs

1. Data based on characterization results, not tested in production.

Figure 19. Typical LSI frequency vs V_{DD}

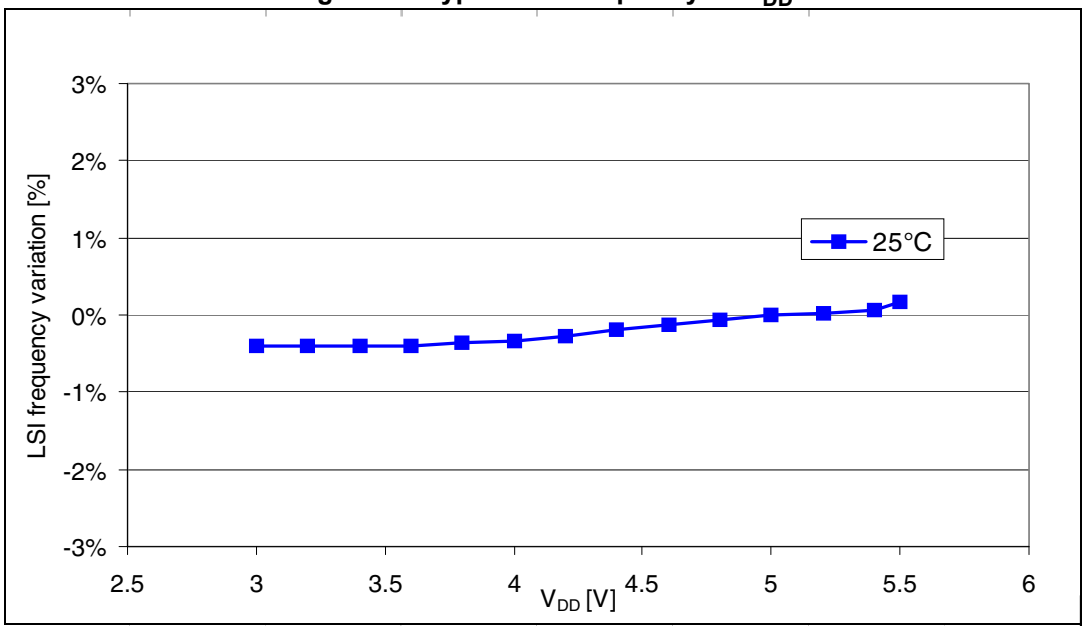
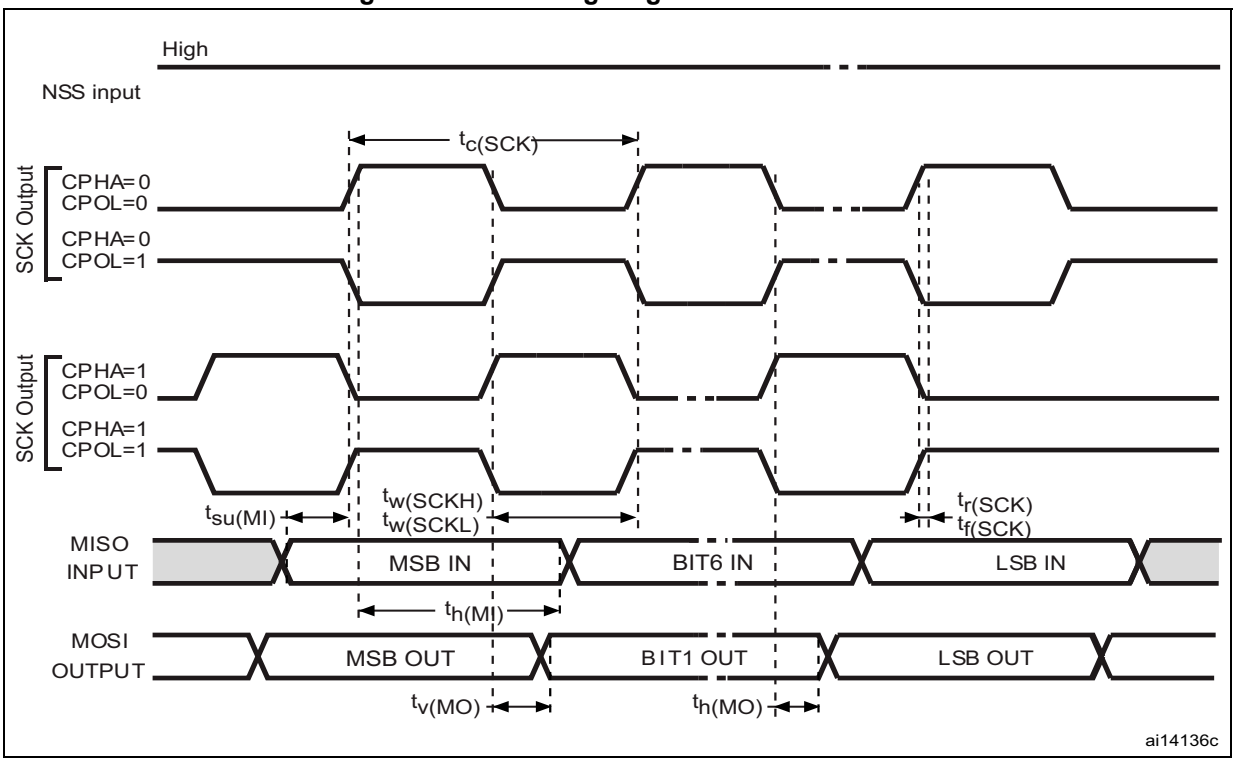


Figure 39. SPI timing diagram - master mode



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

10.3.10 I²C interface characteristics

Table 39. I²C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	-	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time (V_{DD} = 3 to 5.5 V)	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time (V_{DD} = 3 to 5.5 V)	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

10.3.11 10-bit ADC characteristics

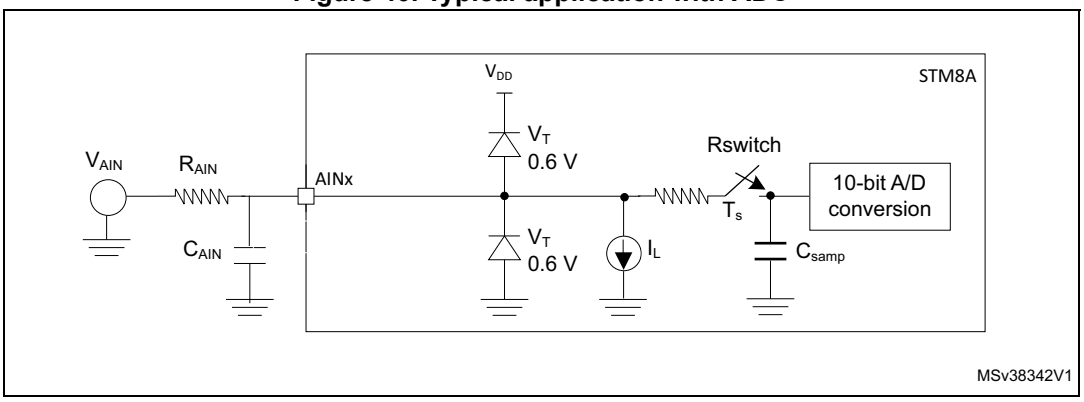
Subject to general operating conditions for V_{DDA}, f_{MASTER}, and T_A unless otherwise specified.

Table 40. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	-	111 kHz	-	4 MHz	kHz/MHz
V_{DDA}	Analog supply	-	3	-	5.5	V
V_{REF+}	Positive reference voltage	-	2.75	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	V_{SSA}	-	0.5	
V_{AIN}	Conversion voltage range(1)	-	V_{SSA}	-	V_{DDA}	
		Devices with external V_{REF+}/ V_{REF-} pins	V_{REF-}	-	V_{REF+}	
C_{samp}	Internal sample and hold capacitor	-	-	-	3	pF
t_S(1)	Sampling time (3 x 1/f_{ADC})	f_{ADC} = 2 MHz	-	1.5	-	µs
		f_{ADC} = 4 MHz	-	0.75	-	
t_{STAB}	Wakeup time from standby	f_{ADC} = 2 MHz	-	7	-	
		f_{ADC} = 4 MHz	-	3.5	-	
t_{CONV}	Total conversion time including sampling time (14 x 1/f_{ADC})	f_{ADC} = 2 MHz	-	7	-	
		f_{ADC} = 4 MHz	-	3.5	-	
R_{switch}	Equivalent switch resistance	-	-	-	30	kΩ

1. During the sample time, the sampling capacitance, C_{samp} (3 pF typ), can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

Figure 40. Typical application with ADC



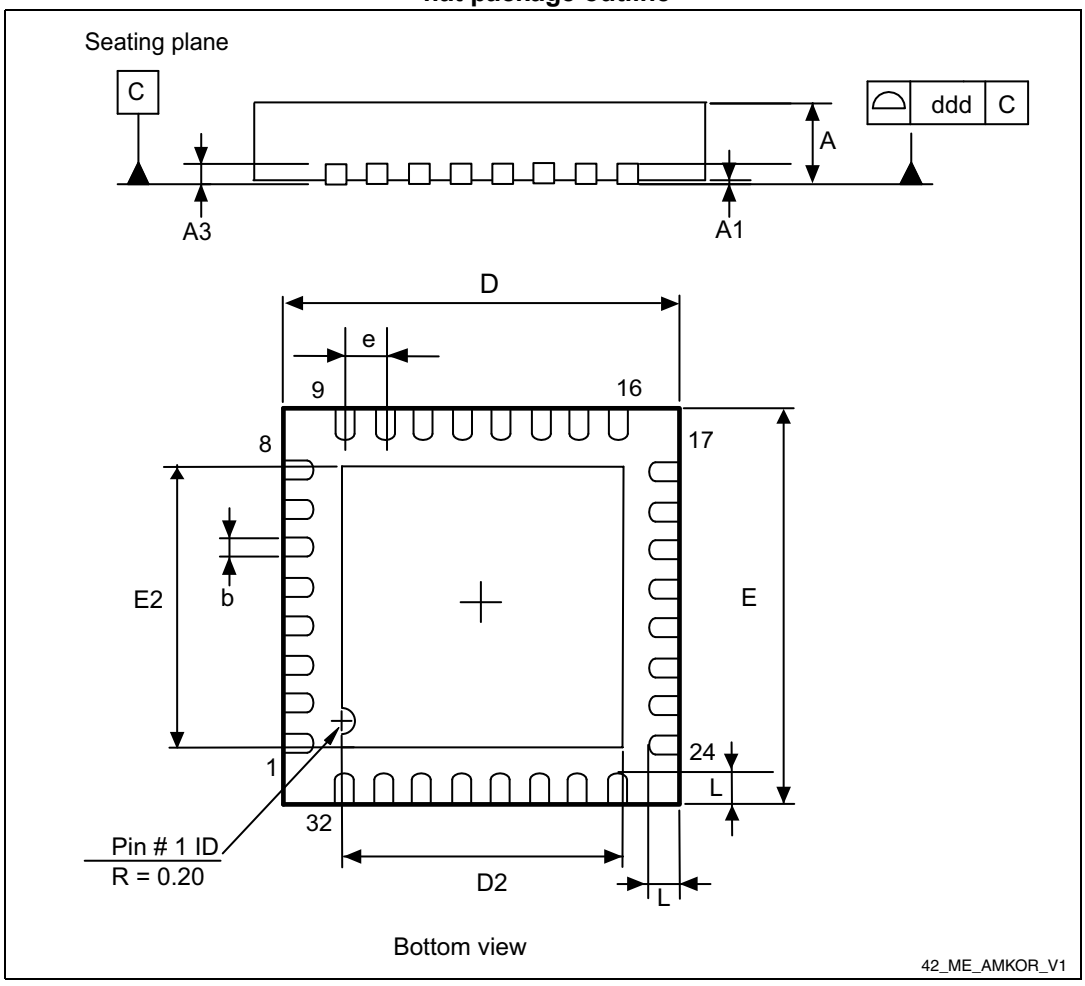
1. Legend: R_{AIN} = external resistance, C_{AIN} = capacitors, C_{samp} = internal sample and hold capacitor.

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

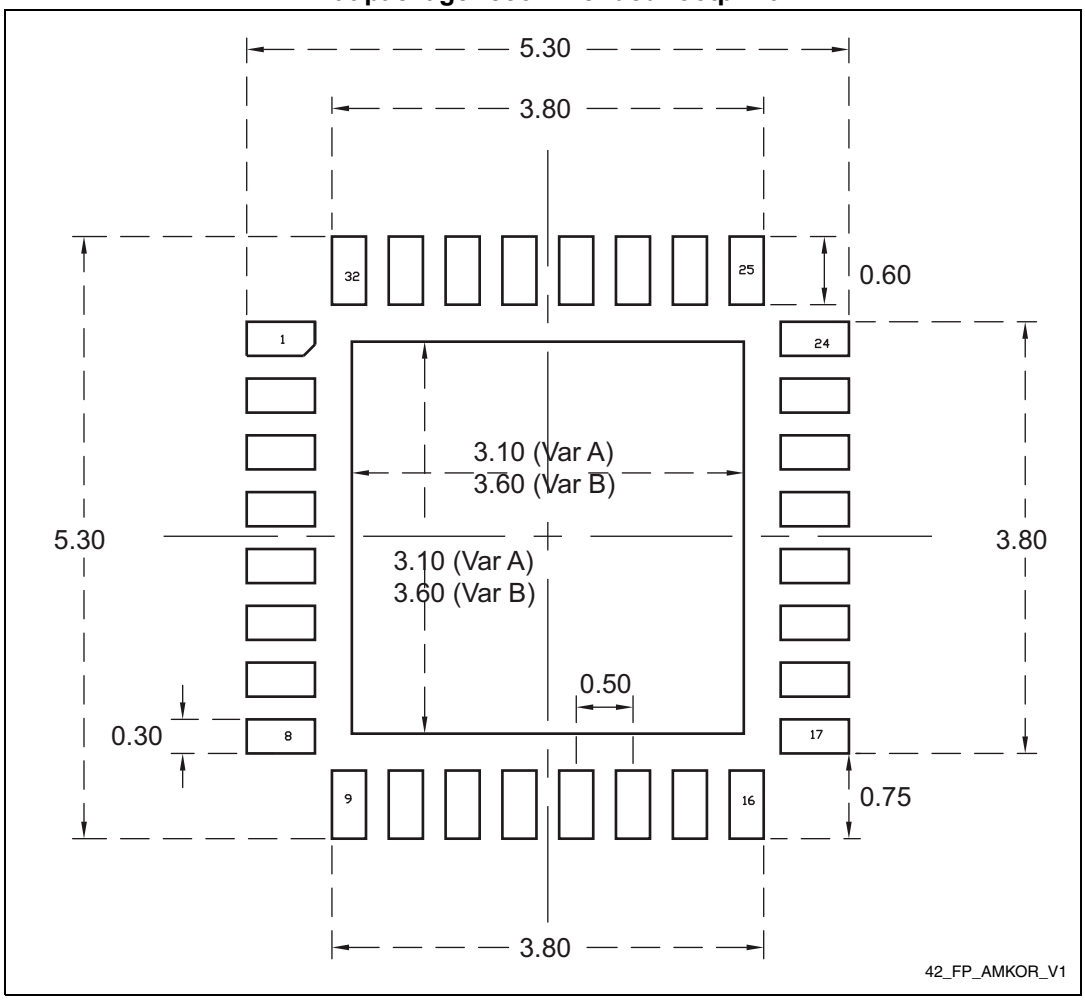
11.1 VFQFPN32 package information

Figure 42. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline



1. Drawing is not to scale.

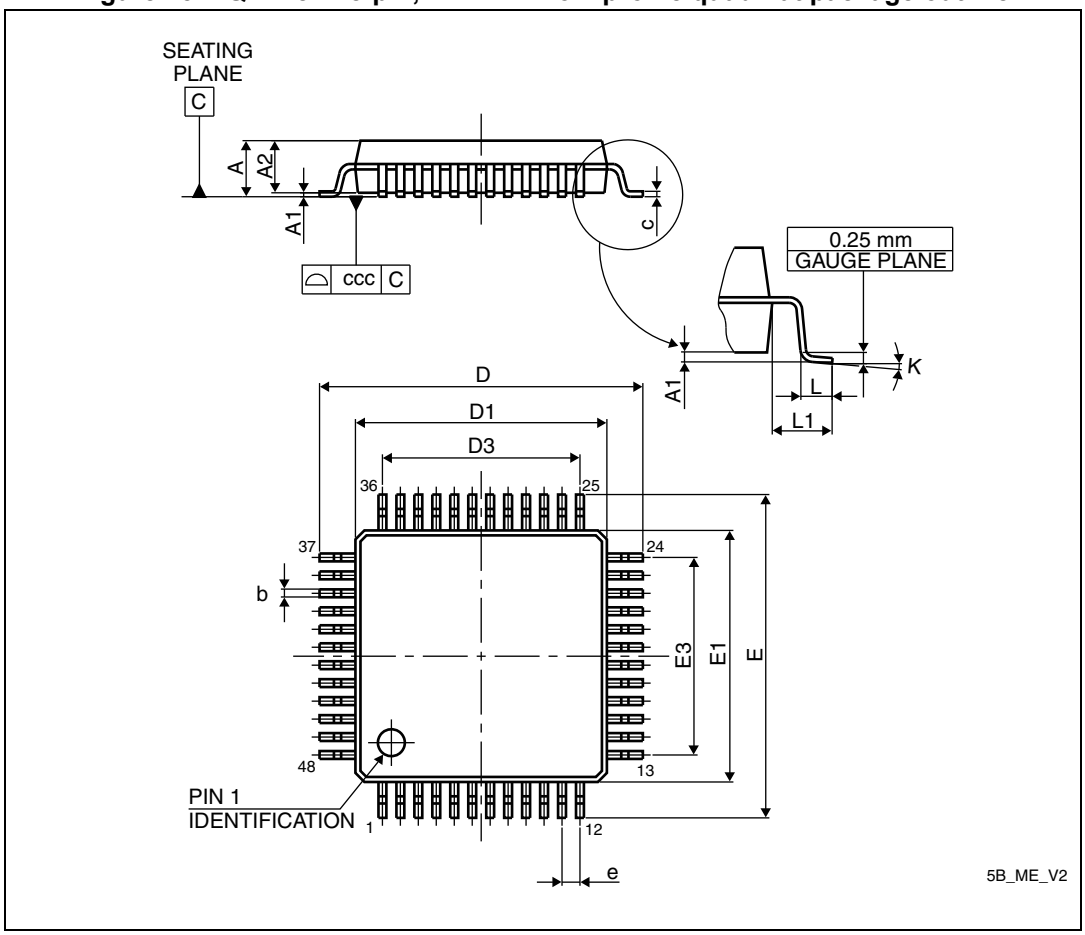
Figure 43. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

11.2 LQFP48 package information

Figure 45. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

13.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8A Flash microcontroller on the user application board via the SWIM protocol. Additional tools are used to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the user STM8A.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

14 Revision history

Table 50. Document revision history

Date	Revision	Changes
22-Aug-2008	1	Initial release
10-Aug-2009	2	Document revised as the following: Updated *Features*; Updated *Table: Device summary;* Updated *Section: Product line-up;* Changed *Section: Product overview*; Updated *Section: Pinouts and pin description;* Changed *Section: Register map;* Updated *Section: Interrupt table;* Updated *Section: Option bytes;* Updated *Section: Electrical characteristics;* Updated *Section: Package information;* Updated *Section: Ordering information;* Added *Section: STM8 development tools.*
22-Oct-2009	3	Adapted *Table: STM8AF61xx/62xx (32 Kbyte) microcontroller pin description.* Added *Section: LIN header error when automatic resynchronization is enabled.*
08-Jul-2010	4	Updated title on cover page. Added VFQFPN32 5x 5 mm package. Added STM8AF62xx devices, and modified cover page header to clarify the part numbers covered by the datasheets. Updated *Note 1* below *Table: Device summary.* Updated D temperature range to -40 to 150°C. Content of *Section: Product overview* reorganized. Renamed *Section: Memory and register map*, and content merged with Register map section. Renamed BL_EN and NBL_EN, BL and NBL, respectively, in *Table: Option bytes.* Added *Table: Operating lifetime.* Added CEXT and P_D (power dissipation) in *Table: General operating conditions*, and *Section: VCAP external capacitor.* Suffix D maximum junction temperature (T_J) updated in *Table: General operating conditions.* Update t_{VDD} in *Table: Operating conditions at power-up/power-down*. Moved *Table: Typical peripheral current consumption VDD = 5.0 V* to *Section: Current consumption for on-chip peripherals* and removed $I_{DD(CAN)}$. Updated *Section: Ordering information* for the devices supported by the datasheet. Updated *Section: STM8 development tools.*

Table 50. Document revision history (continued)

Date	Revision	Changes
31-Jan-2011	5 (continued)	Renamed Fast Active Halt mode to Active-halt mode with regulator on, and Slow Active Halt mode to Active-halt mode with regulator off. Updated *Table: Total current consumption in Halt and Active-halt modes. General conditions for VDD apply, TA = -40 to 55 °C*, in particular $I_{DD(FAH)}$ and $I_{DD(SAH)}$ renamed $I_{DD(AH)}$; $t_{WU(FAH)}$ and $t_{WU(SAH)}$ renamed $t_{WU(AH)}$, and temperature condition added. Removed $I_{DD(USART)}$ from *Table: Typical peripheral current consumption VDD = 5.0 V.* Updated general conditions in *Section: Memory characteristics.* Modified T_{WE} maximum value in *Table: Flash program memory* and *Table: Data memory.* Update $I_{lkg\ ana}$ maximum value for T_A ranging from -40 to 150 °C in *Table: I/O static characteristics*. Added $t_{IFP(NRST)}$ and renamed $V_{F(NRST)}$ t_{IFP} in *Table: NRST pin characteristics.* Added recommendations concerning NRST pin level above *Figure: Recommended reset pin protection,* and updated external capacitor value. Added Raisonance compiler in *Section: Software tools.* Moved know limitations to separate errata sheet.
18-Jul-2012	6	Updated wildcards of document part numbers. *Table: Device summary: u*pdated the footnotes to all STM8AF61xx part numbers. *Section: Introduction:* small text change in first paragraph. *Table: STM8AF62xx product line-up*: added “P” version for all order codes; updated RAM. *Table: STM8AF/H61xx product line-up*: added “P” version for all order codes. *Figure: STM8A block diagram*: updated POR, BOR and WDG; updated LINUART input; added legend. *Section: Flash program and data EEPROM:* removed non relevant bullet points and added a sentence about the factory programmer. *Table: Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers:* updated *ADC features:* updated ADC input range. *Table: Memory model for the devices covered in this datasheet:* updated 16 Kbyte and 8 Kbyte information. *Table: Option bytes*: updated factory default setting for NOPT17; added footnote *1*. *Section: Minimum and maximum values:* T_A = -40 °C (not 40 °C). *Table: General operating conditions:* updated V_{CAP}. *Table: Total current consumption in Run, Wait and Slow mode General conditions for VDD apply, TA = -40 to 150 °C*: updated conditions for $I_{DD(RUN)}$. *Table: I/O static characteristics*: added new condition and new max values for rise and fall time; updated the footnote.