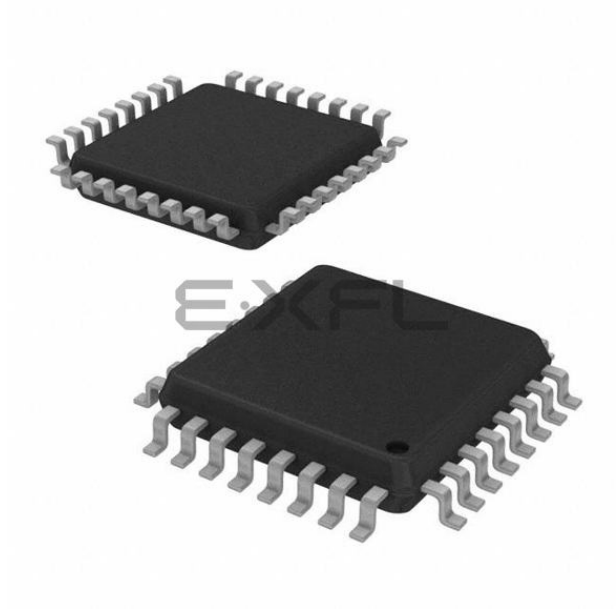

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6266tax

List of figures

5.4.2 Write protection (WP)

Write protection in application mode is intended to avoid unintentional overwriting of the memory. The write protection can be removed temporarily by executing a specific sequence in the user software.

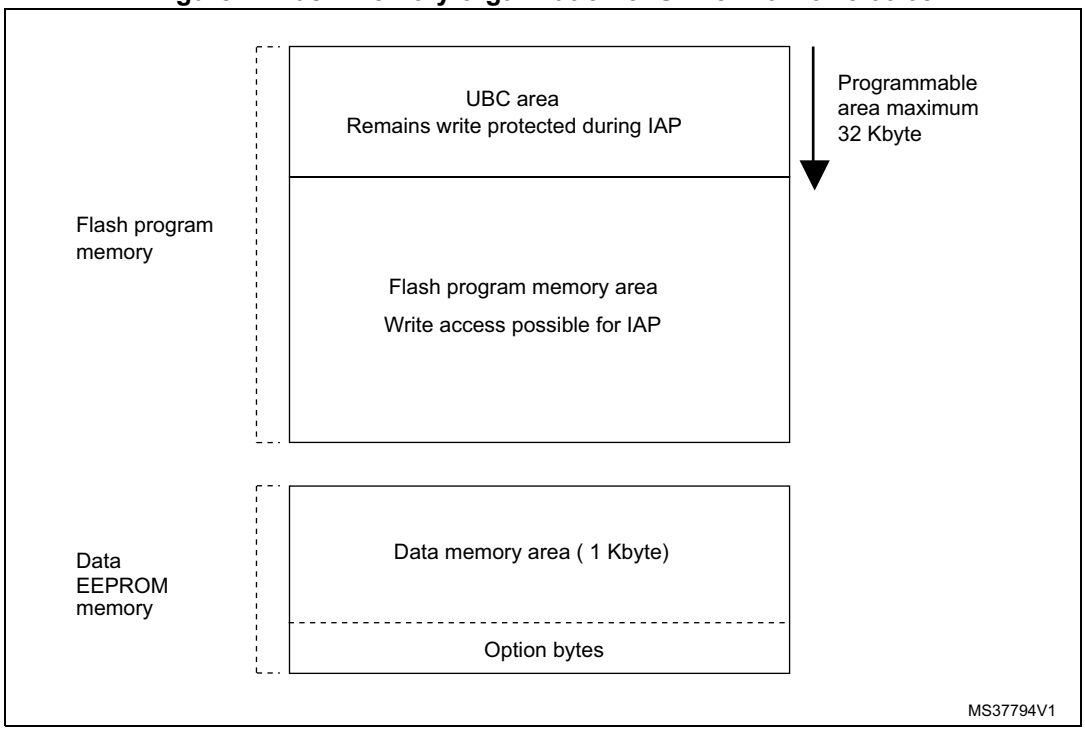
5.4.3 Protection of user boot code (UBC)

If the user chooses to update the Flash program memory using a specific boot code to perform in application programming (IAP), this boot code needs to be protected against unwanted modification.

In the STM8A a memory area of up to 32 Kbyte can be protected from overwriting at user option level. Other than the standard write protection, the UBC protection can exclusively be modified via the debug interface, the user software cannot modify the UBC protection status.

The UBC memory area contains the reset and interrupt vectors and its size can be adjusted in increments of 512 bytes by programming the UBC and NUBC option bytes (see *Section 9: Option bytes on page 44*).

Figure 2. Flash memory organization of STM8AF6246/48/66/68



5.4.4 Read-out protection (ROP)

The STM8A provides a read-out protection of the code and data memory which can be activated by an option byte setting (see the ROP option byte in section 10).

The read-out protection prevents reading and writing Flash program memory, data memory and option bytes via the debug module and SWIM interface. This protection is active in all device operation modes. Any attempt to remove the protection by overwriting the ROP option byte triggers a global erase of the program and data memory.

The ROP circuit may provide a temporary access for debugging or failure analysis. The temporary read access is protected by a user defined, 8-byte keyword stored in the option bytes area. This keyword must be entered via the SWIM interface to temporarily unlock the device.

If desired, the temporary unlock mechanism can be permanently disabled by the user through OPT6/NOPT6 option bytes.

5.5 Clock controller

The clock controller distributes the system clock coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

5.5.1 Features

- **Clock sources**
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
  - 1-16 MHz high-speed external crystal (HSE)
  - Up to 16 MHz high-speed user-external clock (HSE user-ext)
- **Reset**: After reset the microcontroller restarts by default with an internal 2-MHz clock (16 MHz/8). The clock source and speed can be changed by the application program as soon as the code execution starts.
- **Safe clock switching**: Clock sources can be changed safely on the fly in Run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management**: To reduce power consumption, the clock controller can stop the clock to the core or individual peripherals.
- **Wakeup**: In case the device wakes up from low-power modes, the internal RC oscillator (16 MHz/8) is used for quick startup. After a stabilization time, the device switches to the clock source that was selected before Halt mode was entered.
- **Clock security system (CSS)**: The CSS permits monitoring of external clock sources and automatic switching to the internal RC (16 MHz/8) in case of a clock failure.
- **Configurable main clock output (CCO)**: This feature permits to output a clock signal for use by the application.

5.5.3 128 kHz low-speed internal RC oscillator (LSI)

The frequency of this clock is 128 kHz and it is independent from the main clock. It drives the independent watchdog or the AWU wakeup timer.

In systems which do not need independent clock sources for the watchdog counters, the 128 kHz signal can be used as the system clock. This configuration has to be enabled by setting an option byte (OPT3/OPT3N, bit LSI_EN).

5.5.4 16 MHz high-speed external crystal oscillator (HSE)

The external high-speed crystal oscillator can be selected to deliver the main clock in normal Run mode. It operates with quartz crystals and ceramic resonators.

- Frequency range: 1 MHz to 16 MHz
- Crystal oscillation mode: preferred fundamental
- I/Os: standard I/O pins multiplexed with OSCIN, OSCOUT

5.5.5 External clock input

An external clock signal can be applied to the OSCIN input pin of the crystal oscillator. The frequency range is 0 to 16 MHz.

5.5.6 Clock security system (CSS)

The clock security system protects against a system stall in case of an external crystal clock failure.

In case of a clock failure an interrupt is generated and the high-speed internal clock (HSI) is automatically selected with a frequency of 2 MHz (16 MHz/8).

Table 2. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers

Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock
PCKEN17	TIM1	PCKEN13	LINUART	PCKEN27	Reserved	PCKEN23	ADC
PCKEN16	TIM3	PCKEN12	Reserved	PCKEN26	Reserved	PCKEN22	AWU
PCKEN15	TIM2	PCKEN11	SPI	PCKEN25	Reserved	PCKEN21	Reserved
PCKEN14	TIM4	PCKEN10	I^2C	PCKEN24	Reserved	PCKEN20	Reserved

Independent watchdog timer

The independent watchdog peripheral can be used to resolve malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure. If the hardware watchdog feature is enabled through the device option bits, the watchdog is automatically enabled at power-on, and generates a reset unless the key register is written by software before the counter reaches the end of count.

5.7.2 Auto-wakeup counter

This counter is used to cyclically wakeup the device in Active-halt mode. It can be clocked by the internal 128 kHz internal low-frequency RC oscillator or external clock.

LSI clock can be internally connected to TIM3 input capture channel 1 for calibration.

5.7.3 Beeper

This function generates a rectangular signal in the range of 1, 2 or 4 kHz which can be output on a pin. This is useful when audible sounds without interference need to be generated for use in the application.

5.7.4 Advanced control and general purpose timers

STM8A devices described in this datasheet, contain up to three 16-bit advanced control and general purpose timers providing nine CAPCOM channels in total. A CAPCOM channel can be used either as input compare, output compare or PWM channel. These timers are named TIM1, TIM2 and TIM3.

Table 3. Advanced control and general purpose timers

Timer	Counter width	Counter type	Prescaler factor	Channels	Inverted outputs	Repetition counter	trigger unit	External trigger	Break input
TIM1	16-bit	Up/down	1 to 65536	4	3	Yes	Yes	Yes	Yes
TIM2	16-bit	Up	2^n n = 0 to 15	3	None	No	No	No	No
TIM3	16-bit	Up	2^n n = 0 to 15	2	None	No	No	No	No

5.8 Analog-to-digital converter (ADC)

The STM8A products described in this datasheet contain a 10-bit successive approximation ADC with up to 16 multiplexed input channels, depending on the package.

The ADC name differs between the datasheet and STM8S series and STM8AF series 8-bit microcontrollers reference manual (see *Table 5*).

Table 5. ADC naming

Peripheral name in datasheet	Peripheral name in reference manual (RM0016)
ADC	ADC1

ADC features

- 10-bit resolution
- Single and continuous conversion modes
- Programmable prescaler: f_{MASTER} divided by 2 to 18
- Conversion trigger on timer events and external events
- Interrupt generation at end of conversion
- Selectable alignment of 10-bit data in 2 x 8 bit result register
- Shadow registers for data consistency
- ADC input range: $V_{SSA} \leq V_{IN} \leq V_{DDA}$
- Analog watchdog
- Schmitt-trigger on analog inputs can be disabled to reduce power consumption
- Scan mode (single and continuous)
- Dedicated result register for each conversion channel
- Buffer mode for continuous conversion

Note: An additional AIN12 analog input is not selectable in ADC scan mode or with analog watchdog. Values converted from AIN12 are stored only into the ADC_DRH/ADC_DRL registers.

5.9 Communication interfaces

The following sections give a brief overview of the communication peripheral. Some peripheral names differ between the datasheet and STM8S series and STM8AF series 8-bit microcontrollers reference manual (see *Table 6*).

Table 6. Communication peripheral naming correspondence

Peripheral name in datasheet	Peripheral name in reference manual (RM0016)
LINUART	UART2

Table 9. Memory model for the devices covered in this datasheet

Flash program memory size	Flash program memory end address	RAM size	RAM end address	Stack roll-over address
32K	0x00 0FFFF	2K	0x00 07FF	0x00 0600
16K	0x00 0BFFF			

7.2 Register map

In this section the memory and register map of the devices covered by this datasheet is described. For a detailed description of the functionality of the registers, refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016.

Table 10. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX(1)
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX(1)
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0xXX(1)
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX(1)
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00

Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5240	LINUART	UART2_SR	LINUART status register	0xC0
0x00 5241		UART2_DR	LINUART data register	0xXX
0x00 5242		UART2_BRR1	LINUART baud rate register 1	0x00
0x00 5243		UART2_BRR2	LINUART baud rate register 2	0x00
0x00 5244		UART2_CR1	LINUART control register 1	0x00
0x00 5245		UART2_CR2	LINUART control register 2	0x00
0x00 5246		UART2_CR3	LINUART control register 3	0x00
0x00 5247		UART2_CR4	LINUART control register 4	0x00
0x00 5248		Reserved		
0x00 5249		UART2_CR6	LINUART control register 6	0x00
0x00 524A to 0x00 524F	Reserved area (6 bytes)			
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00

Table 16. Option byte description (continued)

Option byte no.	Description
OPT3	**HSITRIM: Trimming option for 16 MHz internal RC oscillator** 0: 3-bit on-the-fly trimming (compatible with devices based on the 128K silicon) 1: 4-bit on-the-fly trimming
	LSI_EN: Low speed internal clock enable 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: Independent watchdog 0: IWDG independent watchdog activated by software 1: IWDG independent watchdog activated by hardware
	WWDG_HW: Window watchdog activation 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: Window watchdog reset on Halt 0: No reset generated on Halt if WWDG active 1: Reset generated on Halt if WWDG active
OPT4	**EXTCLK: External clock selection** 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: Auto-wakeup unit/clock 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for AWU
	PRSC[1:0]: AWU clock prescaler 00: Reserved 01: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]: HSE crystal oscillator stabilization time** This configures the stabilization time to 0.5, 8, 128, and 2048 HSE cycles with corresponding option byte values of 0xE1, 0xD2, 0xB4, and 0x00.
OPT6	**TMU**[3:0]: Enable temporary memory unprotection 0101: TMU disabled (permanent ROP). Any other value: TMU enabled.
OPT7	**Reserved**
OPT8	**TMU_KEY 1 [7:0]: Temporary unprotection key 0** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT9	**TMU_KEY 2 [7:0]: Temporary unprotection key 1** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT10	**TMU_KEY 3 [7:0]: Temporary unprotection key 2** Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT11	**TMU_KEY 4 [7:0]: Temporary unprotection key 3** Temporary unprotection key: Must be different from 0x00 or 0xFF

10.3 Operating conditions

Table 21. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	T_A = -40 °C to 150 °C	0	16	MHz
V_{DD}/V_{DDIO}	Standard operating voltage	-	3.0	5.5	V
V_{CAP}(1)	C_{EXT}: capacitance of external capacitor	-	470	3300	nF
	ESR of external capacitor	at 1 MHz(2)	-	0.3	Ω
	ESL of external capacitor		-	15	nH
P_D	Power dissipation (all temperature ranges)	LQFP32	-	85	mW
		VFQFPN32	-	200	
		LQFP48	-	88	
T_A	Ambient temperature	Suffix A	-40	85	°C
		Suffix C		125	
		Suffix D		150	
T_J	Junction temperature range	Suffix A		90	
		Suffix C		130	
		Suffix D		155	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
2. This frequency of 1 MHz as a condition for V_{CAP} parameters is given by design of internal regulator.

Figure 8. f_{CPUmax} versus V_{DD}

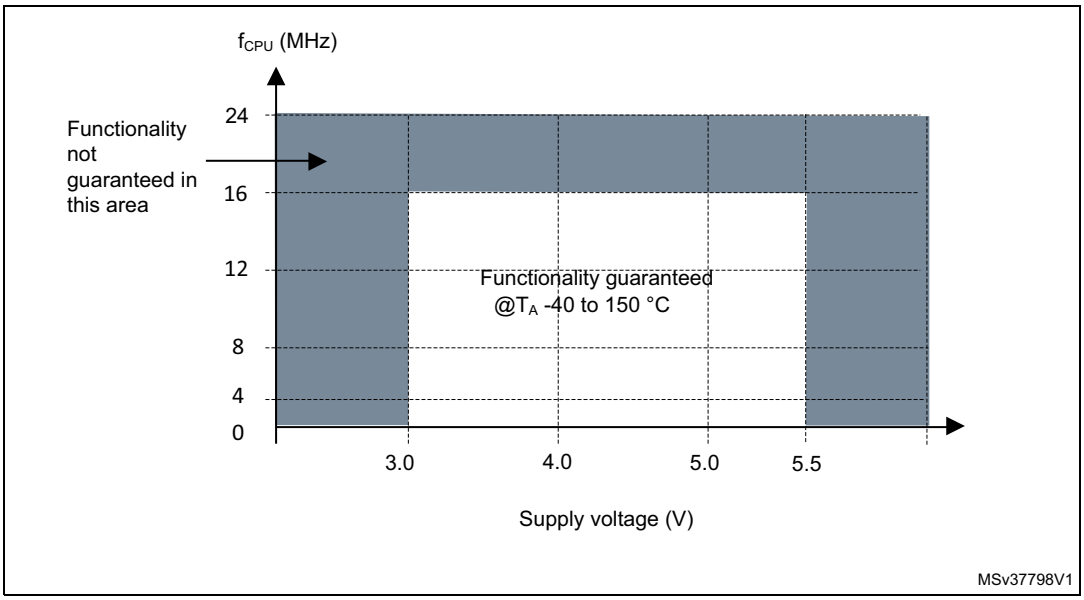
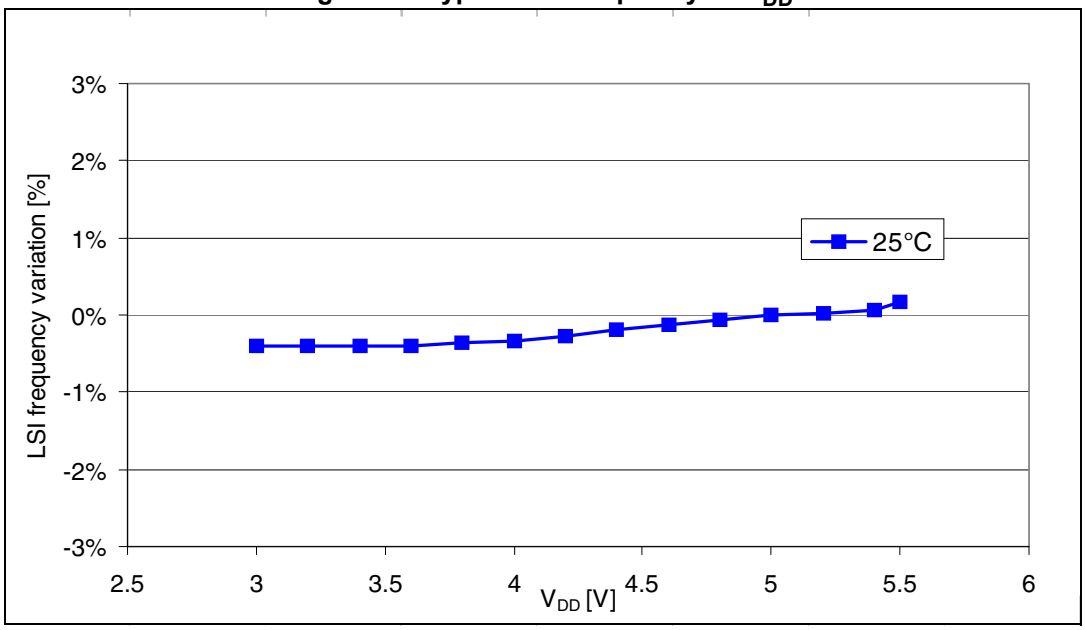


Figure 19. Typical LSI frequency vs V_{DD}



10.3.5 Memory characteristics

Flash program memory/data EEPROM memory

General conditions: T_A = -40 to 150 °C.

Table 32. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	f_{CPU} is 0 to 16 MHz with 0 ws	3.0	-	5.5	V
V_{DD}	Operating voltage (code execution)	f_{CPU} is 0 to 16 MHz with 0 ws	2.6	-	5.5	
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/128 bytes)	-	-	6	6.6	ms
	Fast programming time for 1 block (128 bytes)	-	-	3	3.3	
t_{erase}	Erase time for 1 block (128 bytes)	-	-	3	3.3	

Table 33. Flash program memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Flash program memory endurance (erase/write cycles)(1)	T_A = 25 °C	1000	-	cycles
t_{RET}	Data retention time	T_A = 25 °C	40	-	years
		T_A = 55 °C	20	-	

1. The physical granularity of the memory is four bytes, so cycling is performed on four bytes even when a write/erase operation addresses a single byte.

Table 34. Data memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Data memory endurance(1) (erase/write cycles)	T_A = 25 °C	300 k	-	cycles
		T_A = -40°C to 125 °C	100 k(2)	-	
t_{RET}	Data retention time	T_A = 25 °C	40(2)(3)	-	years
		T_A = 55 °C	20(2)(3)	-	

1. The physical granularity of the memory is four bytes, so cycling is performed on four bytes even when a write/erase operation addresses a single byte.
2. More information on the relationship between data retention time and number of write/erase cycles is available in a separate technical document.
3. Retention time for 256B of data memory after up to 1000 cycles at 125 °C.

10.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage, using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 35. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	-	-0.3 V	-	0.3 x V_{DD}	V
V_{IH}	Input high level voltage		0.7 x V_{DD}	-	V_{DD} + 0.3 V	
V_{hys}	Hysteresis(1)		-	0.1 x V_{DD}	-	
V_{OH}	Output high level voltage	Standard I/0, V_{DD} = 5 V, I = 3 mA	V_{DD} - 0.5 V	-	-	
		Standard I/0, V_{DD} = 3 V, I = 1.5 mA	V_{DD} - 0.4 V	-	-	
V_{OL}	Output low level voltage	High sink and true open drain I/0, V_{DD} = 5 V I = 8 mA	-	-	0.5	
		Standard I/0, V_{DD} = 5 V I = 3 mA	-	-	0.6	
		Standard I/0, V_{DD} = 3 V I = 1.5 mA	-	-	0.4	
R_{pu}	Pull-up resistor	V_{DD} = 5 V, V_{IN} = V_{SS}	35	50	65	kΩ
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 50 pF	-	-	35(2)	ns
		Standard and high sink I/Os Load = 50 pF	-	-	125(2)	
		Fast I/Os Load = 20 pF	-	-	20(2)	
		Standard and high sink I/Os Load = 20 pF	-	-	50(2)	
I_{lkg}	Digital input pad leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA
$I_{lkg\ ana}$	Analog input pad leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$ -40 °C < T_A < 125 °C	-	-	±250	nA
		$V_{SS} \leq V_{IN} \leq V_{DD}$ -40 °C < T_A < 150 °C	-	-	±500	
$I_{lkg(inj)}$	Leakage current in adjacent I/O(3)	Injection current ±4 mA	-	-	±1(3)	µA
I_{DDIO}	Total current on either V_{DDIO} or V_{SSIO}	Including injection currents	-	-	60	mA

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.

Electromagnetic interference (EMI)

Emission tests conform to the IEC 61967-2 standard for test software, board layout and pin loading.

Table 43. EMI data

Symbol	Parameter	Conditions				Unit
		General conditions	Monitored frequency band	Max f_{CPU}(1)		
				8 MHz	16 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP80 package conforming to IEC 61967-2	0.1 MHz to 30 MHz	15	17	dBµV
			30 MHz to 130 MHz	18	22	
			130 MHz to 1 GHz	-1	3	
	EMI level		-	2	2.5	

1. Data based on characterization results, not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 44. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to JESD22-A114	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A= 25°C, conforming to JESD22-C101	3	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine model)	T_A= 25°C, conforming to JESD22-A115	B	200	

1. Data based on characterization results, not tested in production

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin) and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

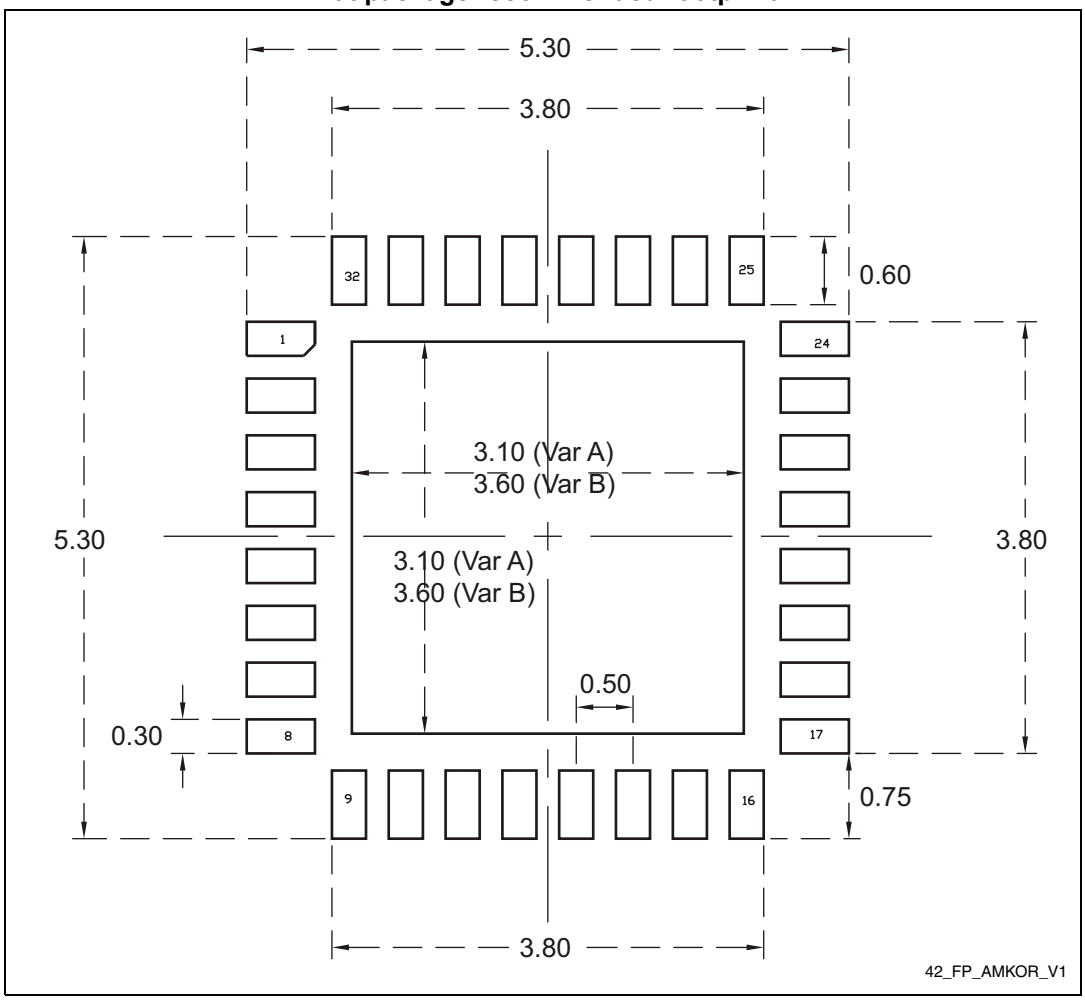
This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 45. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A = 25 °C	A
		T_A = 85 °C	
		T_A = 125 °C	
		T_A = 150 °C	

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

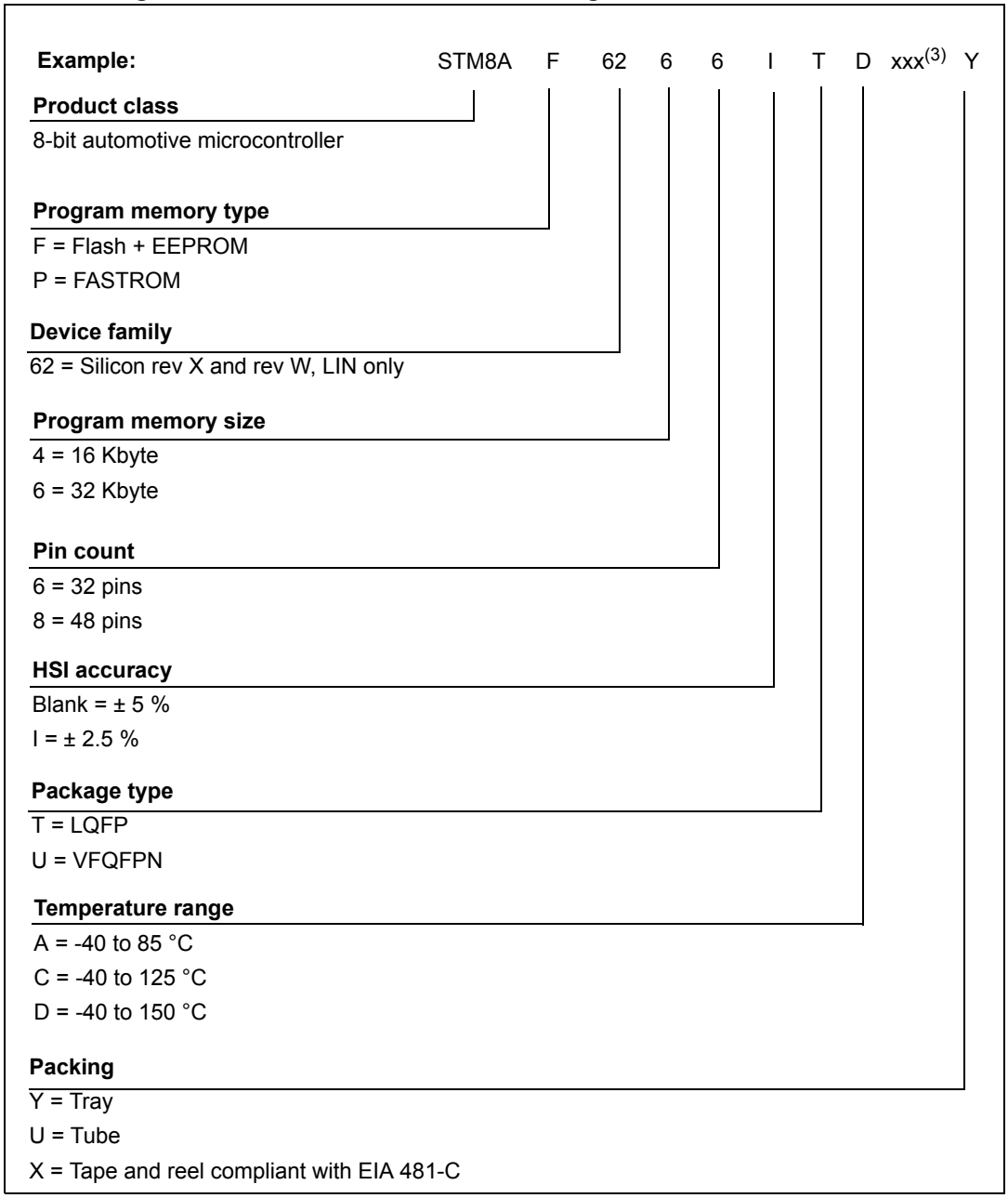
Figure 43. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

12 Ordering information

Figure 51. STM8AF6246/48/66/68 ordering information scheme(1) (2)



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the nearest ST Sales Office.
2. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.
3. Customer specific FASTROM code or custom device configuration. This field shows ‘SSS’ if the device contains a super set silicon, usually equipped with bigger memory and more I/Os. This silicon is supposed to be replaced later by the target silicon.

13.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8A Flash microcontroller on the user application board via the SWIM protocol. Additional tools are used to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the user STM8A.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

14 Revision history

Table 50. Document revision history

Date	Revision	Changes
22-Aug-2008	1	Initial release
10-Aug-2009	2	Document revised as the following: Updated *Features*; Updated *Table: Device summary;* Updated *Section: Product line-up;* Changed *Section: Product overview*; Updated *Section: Pinouts and pin description;* Changed *Section: Register map;* Updated *Section: Interrupt table;* Updated *Section: Option bytes;* Updated *Section: Electrical characteristics;* Updated *Section: Package information;* Updated *Section: Ordering information;* Added *Section: STM8 development tools.*
22-Oct-2009	3	Adapted *Table: STM8AF61xx/62xx (32 Kbyte) microcontroller pin description.* Added *Section: LIN header error when automatic resynchronization is enabled.*
08-Jul-2010	4	Updated title on cover page. Added VFQFPN32 5x 5 mm package. Added STM8AF62xx devices, and modified cover page header to clarify the part numbers covered by the datasheets. Updated *Note 1* below *Table: Device summary.* Updated D temperature range to -40 to 150°C. Content of *Section: Product overview* reorganized. Renamed *Section: Memory and register map*, and content merged with Register map section. Renamed BL_EN and NBL_EN, BL and NBL, respectively, in *Table: Option bytes.* Added *Table: Operating lifetime.* Added CEXT and P_D (power dissipation) in *Table: General operating conditions*, and *Section: VCAP external capacitor.* Suffix D maximum junction temperature (T_J) updated in *Table: General operating conditions.* Update t_{VDD} in *Table: Operating conditions at power-up/power-down*. Moved *Table: Typical peripheral current consumption VDD = 5.0 V* to *Section: Current consumption for on-chip peripherals* and removed $I_{DD(CAN)}$. Updated *Section: Ordering information* for the devices supported by the datasheet. Updated *Section: STM8 development tools.*

Table 50. Document revision history (continued)

Date	Revision	Changes
31-Jan-2011	5 (continued)	Renamed Fast Active Halt mode to Active-halt mode with regulator on, and Slow Active Halt mode to Active-halt mode with regulator off. Updated *Table: Total current consumption in Halt and Active-halt modes. General conditions for VDD apply, TA = -40 to 55 °C*, in particular $I_{DD(FAH)}$ and $I_{DD(SAH)}$ renamed $I_{DD(AH)}$; $t_{WU(FAH)}$ and $t_{WU(SAH)}$ renamed $t_{WU(AH)}$, and temperature condition added. Removed $I_{DD(USART)}$ from *Table: Typical peripheral current consumption VDD = 5.0 V.* Updated general conditions in *Section: Memory characteristics.* Modified T_{WE} maximum value in *Table: Flash program memory* and *Table: Data memory.* Update $I_{lkg\ ana}$ maximum value for T_A ranging from -40 to 150 °C in *Table: I/O static characteristics*. Added $t_{IFP(NRST)}$ and renamed $V_{F(NRST)}$ t_{IFP} in *Table: NRST pin characteristics.* Added recommendations concerning NRST pin level above *Figure: Recommended reset pin protection,* and updated external capacitor value. Added Raisonance compiler in *Section: Software tools.* Moved know limitations to separate errata sheet.
18-Jul-2012	6	Updated wildcards of document part numbers. *Table: Device summary: u*pdated the footnotes to all STM8AF61xx part numbers. *Section: Introduction:* small text change in first paragraph. *Table: STM8AF62xx product line-up*: added “P” version for all order codes; updated RAM. *Table: STM8AF/H61xx product line-up*: added “P” version for all order codes. *Figure: STM8A block diagram*: updated POR, BOR and WDG; updated LINUART input; added legend. *Section: Flash program and data EEPROM:* removed non relevant bullet points and added a sentence about the factory programmer. *Table: Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers:* updated *ADC features:* updated ADC input range. *Table: Memory model for the devices covered in this datasheet:* updated 16 Kbyte and 8 Kbyte information. *Table: Option bytes*: updated factory default setting for NOPT17; added footnote *1*. *Section: Minimum and maximum values:* T_A = -40 °C (not 40 °C). *Table: General operating conditions:* updated V_{CAP}. *Table: Total current consumption in Run, Wait and Slow mode General conditions for VDD apply, TA = -40 to 150 °C*: updated conditions for $I_{DD(RUN)}$. *Table: I/O static characteristics*: added new condition and new max values for rise and fall time; updated the footnote.