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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6266tay

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3 Product line-up

Table 1. STM8AF6246/48/66/68 product line-up

Order code	Package	Medium density Flash program memory (byte)	RAM (byte)	Data EE (byte)	10-bit A/D ch.	Timers (IC/OC/PWM)	Serial interfaces	I/O wakeup pins
STM8AF/P6268	LQFP48 (7x7)	32 K	2 K	1 K	10	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	LIN(UART), SPI, I ² C	38/35
STM8AF/P6248		16 K		0.5 K				
STM8AF/P6266	LQFP32 (7x7)	32 K		1 K	7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	LIN(UART), SPI, I ² C	25/23
STM8AF/P6246		16 K		0.5 K				
STM8AF/P6266	VFQFPN32	32 K		1 K	7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	LIN(UART), SPI, I ² C	25/23
STM8AF/P6246		16 K		0.5 K				

5 Product overview

This section describes the family features that are implemented in the products covered by this datasheet.

For more detailed information on each feature please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).

5.1 STM8A central processing unit (CPU)

The 8-bit STM8A core is a modern CISC core and has been designed for code efficiency and performance. It contains 21 internal registers (six directly addressable in each execution context), 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

5.1.1 Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus with single cycle fetching for most instructions
- X and Y 16-bit index registers, enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter with 16-Mbyte linear memory space
- 16-bit stack pointer with access to a 64 Kbyte stack
- 8-bit condition code register with seven condition flags for the result of the last instruction.

5.1.2 Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for efficient implementation of local variables and parameter passing

5.1.3 Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

5.6 Low-power operating modes

For efficient power management, the application can be put in one of four different low power modes. Users can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- **Wait mode**
In this mode, the CPU is stopped but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- **Active-halt mode with regulator on**
In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in Active-halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- **Active-halt mode with regulator off**
This mode is the same as Active-halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- **Halt mode**
CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

In all modes the CPU and peripherals remain permanently powered on, the system clock is applied only to selected modules. The RAM content is preserved and the brown-out reset circuit remains activated.

5.7 Timers

5.7.1 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications. The watchdog timer activity is controlled by the application program or option bytes. Once the watchdog is activated, it cannot be disabled by the user program without going through reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application timing perfectly. The application software must refresh the counter before time-out and during a limited time window. If the counter is refreshed outside this time window, a reset is issued.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure. If the hardware watchdog feature is enabled through the device option bits, the watchdog is automatically enabled at power-on, and generates a reset unless the key register is written by software before the counter reaches the end of count.

5.7.2 Auto-wakeup counter

This counter is used to cyclically wakeup the device in Active-halt mode. It can be clocked by the internal 128 kHz internal low-frequency RC oscillator or external clock.

LSI clock can be internally connected to TIM3 input capture channel 1 for calibration.

5.7.3 Beeper

This function generates a rectangular signal in the range of 1, 2 or 4 kHz which can be output on a pin. This is useful when audible sounds without interference need to be generated for use in the application.

5.7.4 Advanced control and general purpose timers

STM8A devices described in this datasheet, contain up to three 16-bit advanced control and general purpose timers providing nine CAPCOM channels in total. A CAPCOM channel can be used either as input compare, output compare or PWM channel. These timers are named TIM1, TIM2 and TIM3.

Table 3. Advanced control and general purpose timers

Timer	Counter width	Counter type	Prescaler factor	Channels	Inverted outputs	Repetition counter	trigger unit	External trigger	Break input
TIM1	16-bit	Up/down	1 to 65536	4	3	Yes	Yes	Yes	Yes
TIM2	16-bit	Up	2^n $n = 0$ to 15	3	None	No	No	No	No
TIM3	16-bit	Up	2^n $n = 0$ to 15	2	None	No	No	No	No

- Interrupt:
 - Successful address/data communication
 - Error condition
 - Wakeup from Halt
- Wakeup from Halt on address detection in slave mode

5.9.3 Universal asynchronous receiver/transmitter with LIN support (LINUART)

The devices covered by this datasheet contain one LINUART interface. The interface is available on all the supported packages. The LINUART is an asynchronous serial communication interface which supports extensive LIN functions tailored for LIN slave applications. In LIN mode it is compliant to the LIN standards rev 1.2 to rev 2.2.

Detailed feature list:

LIN mode

Master mode:

- LIN break and delimiter generation
- LIN break and delimiter detection with separate flag and interrupt source for read back checking.

Slave mode:

- Autonomous header handling – one single interrupt per valid header
- Mute mode to filter responses
- Identifier parity error checking
- LIN automatic resynchronization, allowing operation with internal RC oscillator (HSI) clock source
- Break detection at any time, even during a byte reception
- Header errors detection:
 - Delimiter too short
 - Synch field error
 - Deviation error (if automatic resynchronization is enabled)
 - Framing error in synch field or identifier field
 - Header time-out

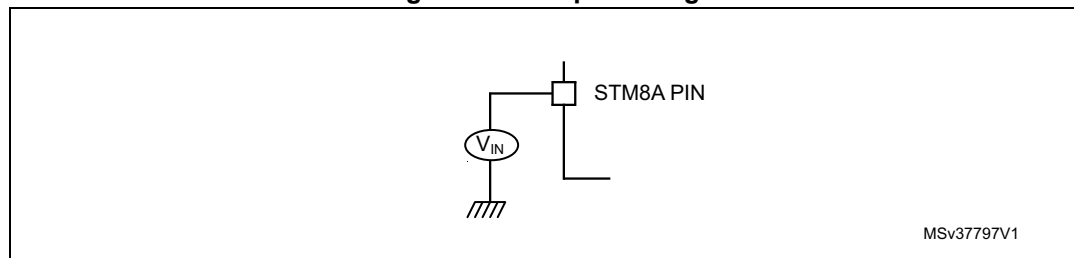
Table 8. STM8AF6246/48/66/68 (32 Kbyte) microcontroller pin description⁽¹⁾⁽²⁾

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	VFQFPN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	NRST	I/O	-	X	-	-	-	-	-	Reset		-
2	2	PA1/OSCIN ⁽³⁾	I/O	X	X	-	-	O1	X	X	Port A1	Resonator/crystal in	-
3	3	PA2/OSCOU	I/O	X	X	X	-	O1	X	X	Port A2	Resonator/crystal out	-
4	-	V _{SSIO_1}	S	-	-	-	-	-	-	-	I/O ground		-
5	4	V _{SS}	S	-	-	-	-	-	-	-	Digital ground		-
6	5	V _{CAP}	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
7	6	V _{DD}	S	-	-	-	-	-	-	-	Digital power supply		-
8	7	V _{DDIO_1}	S	-	-	-	-	-	-	-	I/O power supply		-
-	8	PF4/AIN12 ⁽⁴⁾⁽⁵⁾	I/O	X	X		-	O1	X	X	Port F4	Analog input 12	-
9	-	PA3/TIM2_CH3	I/O	X	X	X	-	O1	X	X	Port A3	Timer 2 - channel 3	TIM3_CH1 [AFR1]
10	-	PA4	I/O	X	X	X	-	O3	X	X	Port A4		-
11	-	PA5	I/O	X	X	X	-	O3	X	X	Port A5		-
12	-	PA6	I/O	X	X	X	-	O3	X	X	Port A6		-
13	9	V _{DDA}	S	-	-	-	-	-	-	-	Analog power supply		-
14	10	V _{SSA}	S	-	-	-	-	-	-	-	Analog ground		-
15	-	PB7/AIN7	I/O	X	X	X	-	O1	X	X	Port B7	Analog input 7	-
16	-	PB6/AIN6	I/O	X	X	X	-	O1	X	X	Port B6	Analog input 6	-
17	11	PB5/AIN5	I/O	X	X	X	-	O1	X	X	Port B5	Analog input 5	I ² C_SDA [AFR6]
18	12	PB4/AIN4	I/O	X	X	X	-	O1	X	X	Port B4	Analog input 4	I ² C_SCL [AFR6]
19	13	PB3/AIN3	I/O	X	X	X	-	O1	X	X	Port B3	Analog input 3	TIM1_ETR [AFR5]
20	14	PB2/AIN2	I/O	X	X	X	-	O1	X	X	Port B2	Analog input	TIM1_NCC3 [AFR5]
21	15	PB1/AIN1	I/O	X	X	X	-	O1	X	X	Port B1	Analog input 1	TIM1_NCC2 [AFR5]
22	16	PB0/AIN0	I/O	X	X	X	-	O1	X	X	Port B0	Analog input 0	TIM1_NCC1 [AFR5]
23	-	PE7/AIN8	I/O	X	X		-	O1	X	X	Port E7	Analog input 8	-

10.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 7](#).

Figure 7. Pin input voltage



10.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 17. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DDx} - V_{SS}$	Supply voltage (including V_{DDA} and V_{DDIO}) ⁽¹⁾	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (PE1, PE2) ⁽²⁾	$V_{SS} - 0.3$	6.5	V
	Input voltage on any other pin ⁽²⁾	$V_{SS} - 0.3$	$V_{DD} + 0.3$	
$ V_{DDx} - V_{DD} $	Variations between different power pins	-	50	mV
$ V_{SSx} - V_{SS} $	Variations between all the different ground pins	-	50	
V_{ESD}	Electrostatic discharge voltage	see <i>Absolute maximum ratings (electrical sensitivity) on page 76</i>		

1. All power (V_{DD} , V_{DDIO} , V_{DDA}) and ground (V_{SS} , V_{SSIO} , V_{SSA}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Table 22. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	2 ⁽¹⁾	-	∞	$\mu\text{s/V}$
	V_{DD} fall time rate	-	2 ⁽¹⁾	-	∞	
t_{TEMP}	Reset release delay	V_{DD} rising	-	1	1.7	ms
	Reset generation delay	V_{DD} falling	-	3	-	μs
V_{IT+}	Power-on reset threshold ^{(2) (3)}	-	2.65	2.8	2.95	V
V_{IT-}	Brown-out reset threshold	-	2.58	2.73	2.88	
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70 ⁽¹⁾	-	mV

1. Guaranteed by design, not tested in production
2. If V_{DD} is below 3 V, the code execution is guaranteed above the V_{IT-} and V_{IT+} thresholds. RAM content is kept. The EEPROM programming sequence must not be initiated.
3. There is inrush current into V_{DD} present after device power on to charge C_{EXT} capacitor. This inrush energy depends from C_{EXT} capacitor value. For example, a C_{EXT} of 1 μF requires $Q=1 \mu\text{F} \times 1.8\text{V} = 1.8 \mu\text{C}$.

Table 26. Programming current consumption

Symbol	Parameter	Conditions	Typ	Max	Unit
$I_{DD(Prog)}$	Programming current	$V_{DD} = 5\text{ V}$, $-40\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$, erasing and programming data or Flash program memory	1.0	1.7	mA

Table 27. Typical peripheral current consumption $V_{DD} = 5.0\text{ V}^{(1)}$

Symbol	Parameter	Typ. $f_{master} = 2\text{ MHz}$	Typ. $f_{master} = 16\text{ MHz}$	Unit
$I_{DD(TIM1)}$	TIM1 supply current ⁽²⁾	0.03	0.23	mA
$I_{DD(TIM2)}$	TIM2 supply current ⁽²⁾	0.02	0.12	
$I_{DD(TIM3)}$	TIM3 supply current ⁽²⁾	0.01	0.1	
$I_{DD(TIM4)}$	TIM4 supply current ⁽²⁾	0.004	0.03	
$I_{DD(LINUART)}$	LINUART supply current ⁽²⁾	0.03	0.11	
$I_{DD(SPI)}$	SPI supply current ⁽²⁾	0.01	0.04	
$I_{DD(I^2C)}$	I ² C supply current ⁽²⁾	0.02	0.06	
$I_{DD(AWU)}$	AWU supply current ⁽²⁾	0.003	0.02	
$I_{DD(TOT_DIG)}$	All digital peripherals on	0.22	1	
$I_{DD(ADC)}$	ADC supply current when converting ⁽³⁾	0.93	0.95	

1. Typical values not tested in production. Since the peripherals are powered by an internally regulated, constant digital supply voltage, the values are similar in the full supply voltage range.
2. Data based on a differential I_{DD} measurement between no peripheral clocked and a single active peripheral. This measurement does not include the pad toggling consumption.
3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

Current consumption curves

Figure 10 to Figure 15 show typical current consumption measured with code executing in RAM.

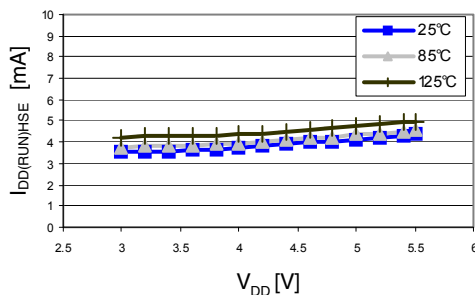
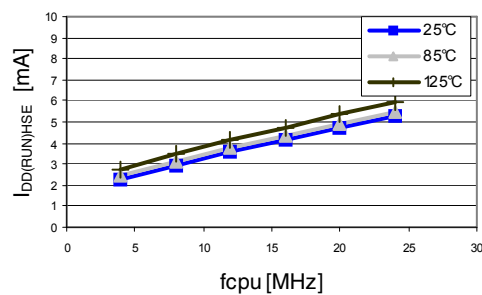
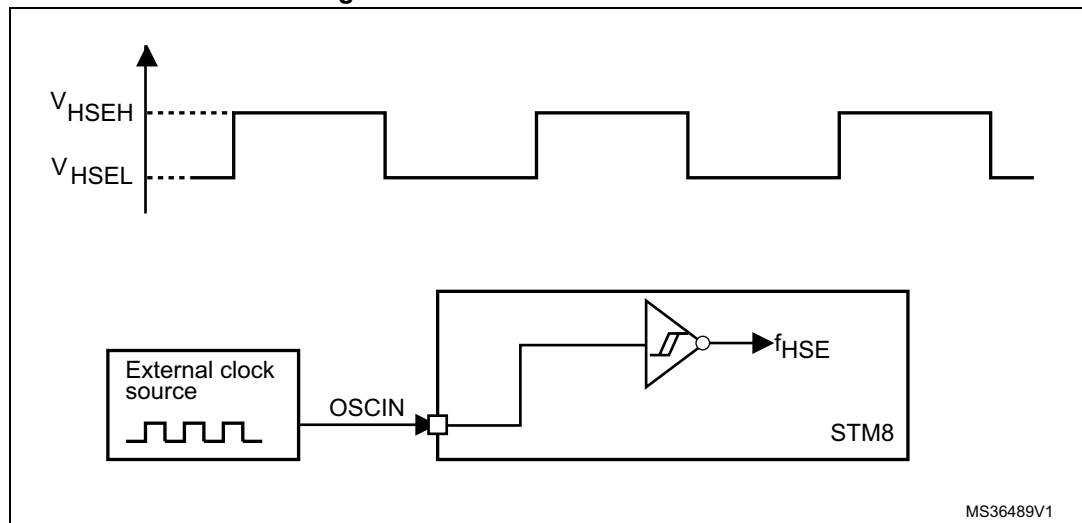
Figure 10. Typ. $I_{DD(RUN)HSE}$ vs. V_{DD}
@ $f_{CPU} = 16\text{ MHz}$, peripheral = onFigure 11. Typ. $I_{DD(RUN)HSE}$ vs. f_{CPU}
@ $V_{DD} = 5.0\text{ V}$, peripheral = on

Figure 16. HSE external clock source



MS36489V1

HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied using a crystal/ceramic resonator oscillator of up to 16 MHz. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 29. HSE oscillator characteristics

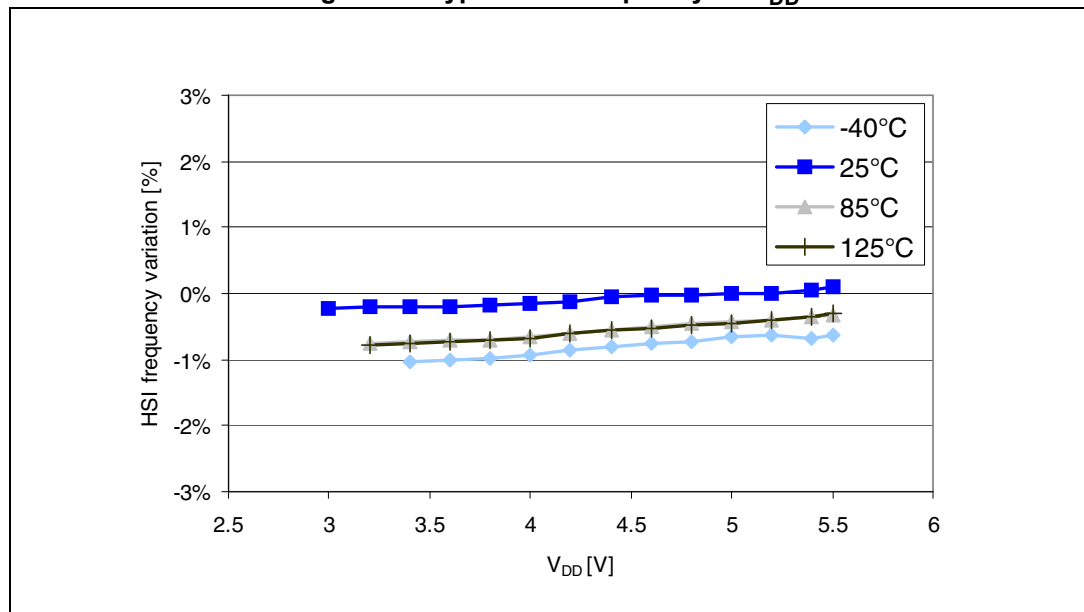
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	220	-	$k\Omega$
$C_{L1}/C_{L2}^{(1)}$	Recommended load capacitance	-	-	-	20	pF
g_m	Oscillator transconductance	-	5	-	-	mA/V
$t_{SU(HSE)}^{(2)}$	Startup time	V_{DD} is stabilized	-	2.8	-	ms

1. The oscillator needs two load capacitors, C_{L1} and C_{L2} , to act as load for the crystal. The total load capacitance (C_{load}) is $(C_{L1} * C_{L2}) / (C_{L1} + C_{L2})$. If $C_{L1} = C_{L2}$, $C_{load} = C_{L1} / 2$. Some oscillators have built-in load capacitors, C_{L1} and C_{L2} .
2. This value is the startup time, measured from the moment it is enabled (by software) until a stabilized 16 MHz oscillation is reached. It can vary with the crystal type that is used.

Table 30. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ACC _{HS}	HSI oscillator user trimming accuracy	Trimmed by the application for any V _{DD} and T _A conditions	-1 ⁽¹⁾	-	1 ⁽¹⁾	%
			-0.5 ⁽¹⁾	-	0.5 ⁽¹⁾	
	HSI oscillator accuracy (factory calibrated)	3.0 V ≤ V _{DD} ≤ 5.5 V, -40 °C ≤ T _A ≤ 150 °C	-5	-	5	
		3.0 V ≤ V _{DD} ≤ 5.5 V, -40 °C ≤ T _A ≤ 125 °C	-2.5 ⁽²⁾	-	2.5 ⁽²⁾	
t _{su} (HSI)	HSI oscillator wakeup time	-	-	-	2 ⁽³⁾	μs

1. Depending on option byte setting (OPT3 and NOPT3)
2. These values are guaranteed for STM8AF62x6ITx order codes only.
3. Guaranteed by characterization, not tested in production

Figure 18. Typical HSI frequency vs V_{DD}

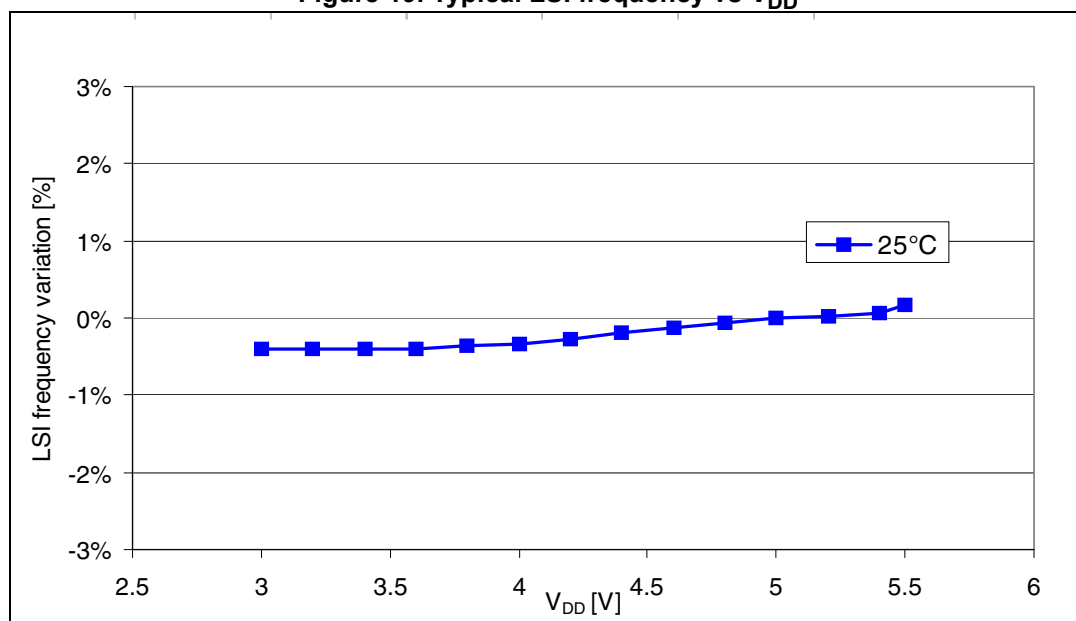
Low speed internal RC oscillator (LSI)

Subject to general operating conditions for V_{DD} and T_A.

Table 31. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{LSI}	Frequency	-	112	128	144	kHz
t _{su} (LSI)	LSI oscillator wakeup time	-	-	-	7 ⁽¹⁾	μs

1. Data based on characterization results, not tested in production.

Figure 19. Typical LSI frequency vs V_{DD} 

2. Guaranteed by design.
3. Data based on characterization results, not tested in production.

Figure 20. Typical V_{IL} and V_{IH} vs V_{DD} @ four temperatures

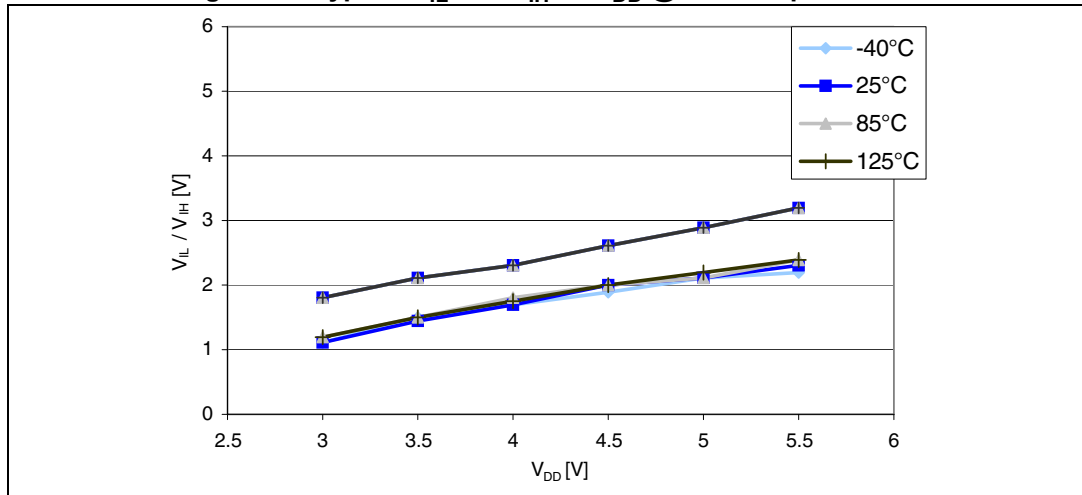


Figure 21. Typical pull-up resistance R_{PU} vs V_{DD} @ four temperatures

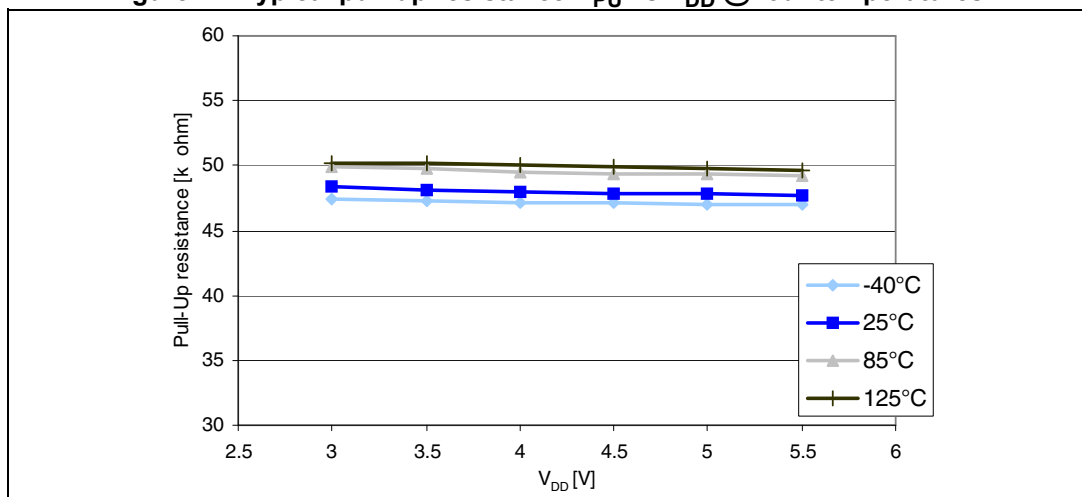
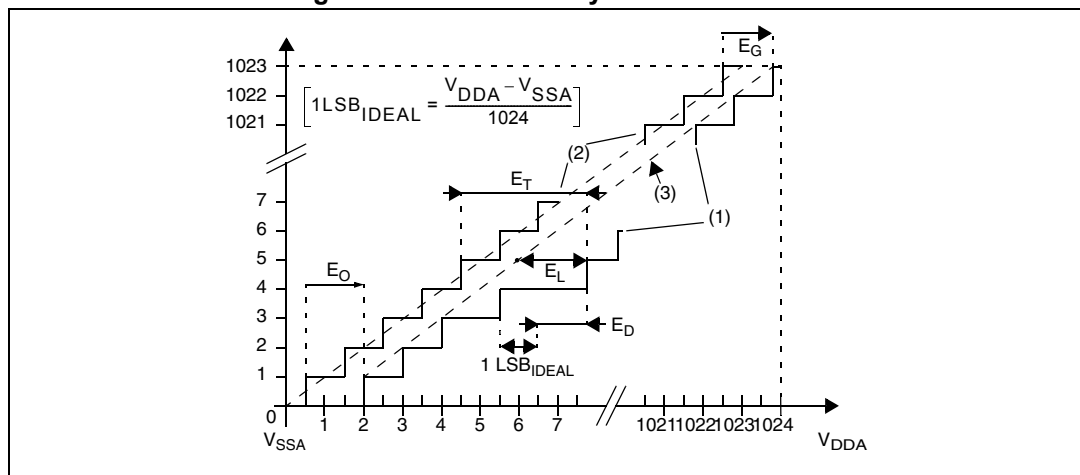


Table 41. ADC accuracy for $V_{DDA} = 5\text{ V}$

Symbol	Parameter	Conditions	Typ	Max ⁽¹⁾	Unit
$ E_T $	Total unadjusted error ⁽²⁾	$f_{\text{ADC}} = 2\text{ MHz}$	1.4	3 ⁽³⁾	LSB
$ E_O $	Offset error ⁽²⁾		0.8	3	
$ E_G $	Gain error ⁽²⁾		0.1	2	
$ E_D $	Differential linearity error ⁽²⁾		0.9	1	
$ E_L $	Integral linearity error ⁽²⁾		0.7	1.5	
$ E_T $	Total unadjusted error ⁽²⁾	$f_{\text{ADC}} = 4\text{ MHz}$	1.9 ⁽⁴⁾	4 ⁽⁴⁾	
$ E_O $	Offset error ⁽²⁾		1.3 ⁽⁴⁾	4 ⁽⁴⁾	
$ E_G $	Gain error ⁽²⁾		0.6 ⁽⁴⁾	3 ⁽⁴⁾	
$ E_D $	Differential linearity error ⁽²⁾		1.5 ⁽⁴⁾	2 ⁽⁴⁾	
$ E_L $	Integral linearity error ⁽²⁾		1.2 ⁽⁴⁾	1.5 ⁽⁴⁾	

1. Max value is based on characterization, not tested in production.
2. ADC accuracy vs. injection current: Any positive or negative injection current within the limits specified for $I_{\text{INJ(PIN)}}$ and $\Sigma I_{\text{INJ(PIN)}}$ in [Section 10.3.6](#) does not affect the ADC accuracy.
3. TUE 2LSB can be reached on specific sales types on the whole temperature range.
4. Target values.

Figure 41. ADC accuracy characteristics



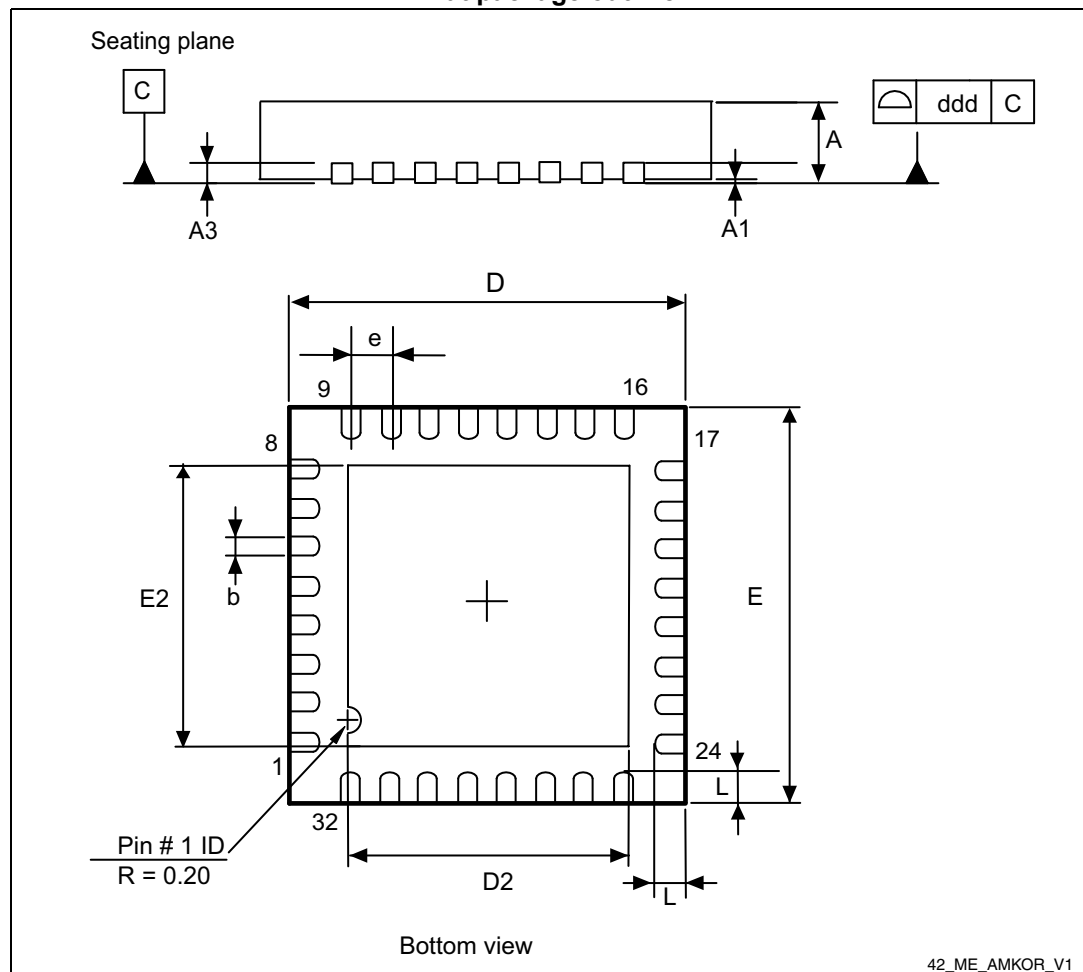
1. Example of an actual transfer curve
 2. The ideal transfer curve
 3. End point correlation line
- E_T = Total unadjusted error: Maximum deviation between the actual and the ideal transfer curves.
 E_O = Offset error: Deviation between the first actual transition and the first ideal one.
 E_G = Gain error: Deviation between the last ideal transition and the last actual one.
 E_D = Differential linearity error: Maximum deviation between actual steps and the ideal one.
 E_L = Integral linearity error: Maximum deviation between any actual transition and the end point correlation line.

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

11.1 VFQFPN32 package information

Figure 42. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline



1. Drawing is not to scale.

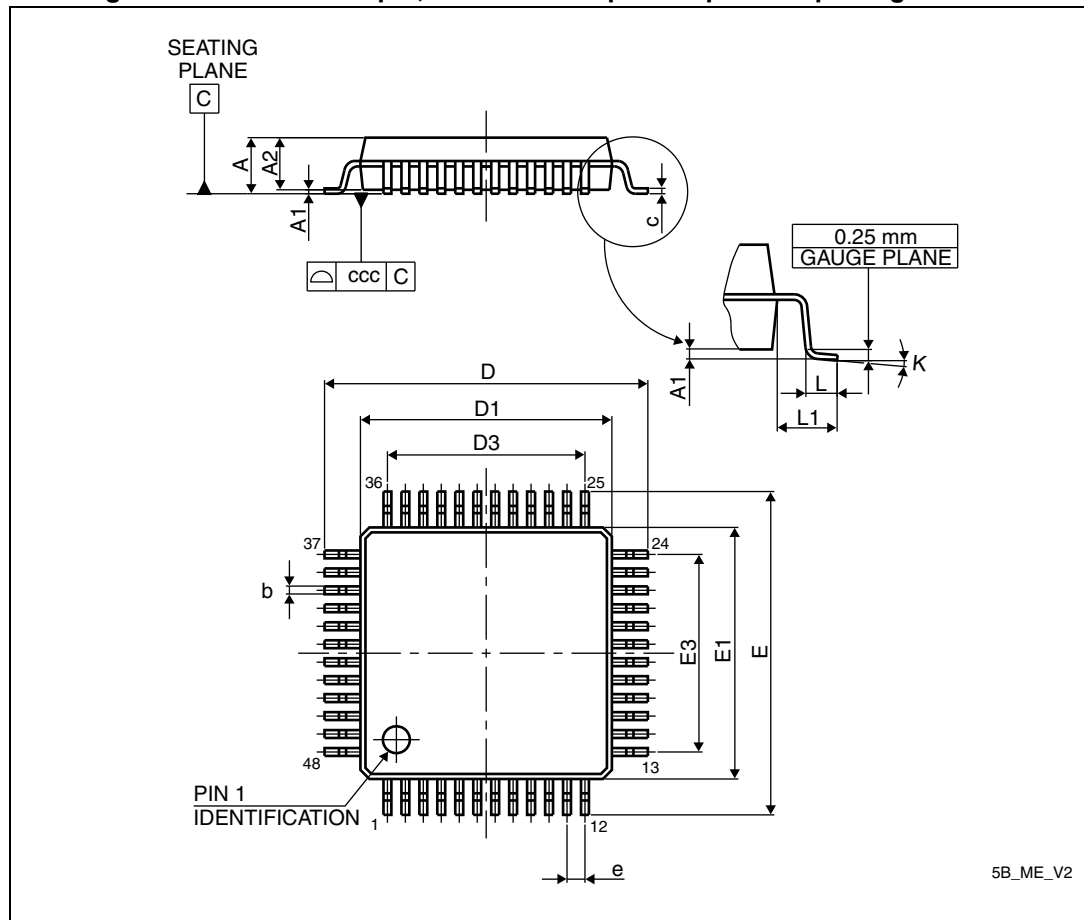
Table 46. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.200	-	-	0.0079	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D2	3.500	3.600	3.700	0.1378	0.1417	0.1457
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E2	3.500	3.600	3.700	0.1378	0.1417	0.1457
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

11.2 LQFP48 package information

Figure 45. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

13.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST visual develop (STVD) IDE and the ST visual programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8.

13.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at www.st.com. This package includes:

ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8A microcontroller Flash memory. STVP also offers project mode for saving programming configurations and automating programming sequences.

13.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of the application directly from an easy-to-use graphical interface.

Available toolchains include:

C compiler for STM8

All compilers are available in free version with a limited code size depending on the compiler. For more information, refer to www.cosmic-software.com, www.raisonance.com, and www.iar.com.

STM8 assembler linker

Free assembly toolchain included in the STM8 toolset, which allows users to assemble and link the application source code.