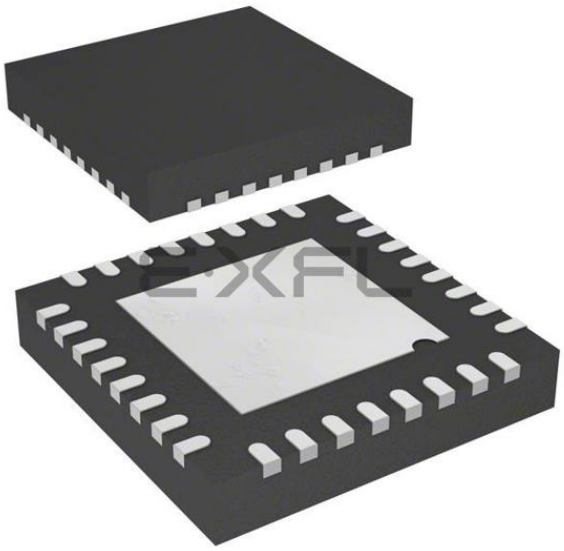

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6266ucy

List of tables

4 Block diagram

Figure 1. STM8AF6246/48/66/68 block diagram

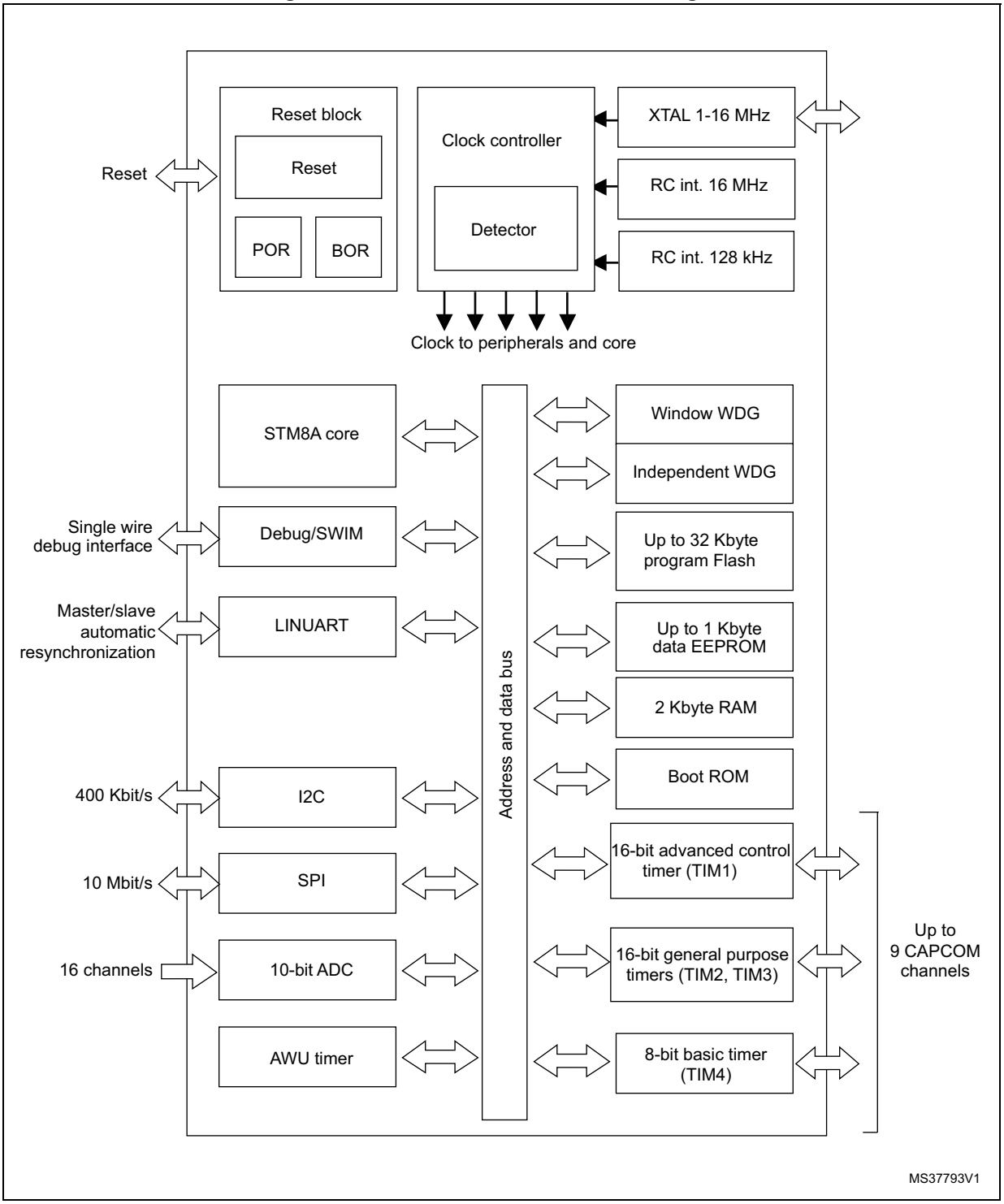


Table 8. STM8AF6246/48/66/68 (32 Kbyte) microcontroller pin description(1)(2) (continued)

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	VFQFPN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
24		PE6/AIN9	I/O	**X**	X	X	-	O1	X	X	**Port E7**	Analog input 9	-
25	17	PE5/SPI_NSS	I/O	**X**	X	X	-	O1	X	X	**Port E5**	SPI master/slave select	-
26	18	PC1/TIM1_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1	-
27	19	PC2/TIM1_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1- channel 2	-
28	20	PC3/TIM1_CH3	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	-
29	21	PC4/TIM1_CH4	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4	-
30	22	PC5/SPI_SCK	I/O	**X**	X	X		O3	X	X	**Port C5**	SPI clock	-
31	-	V_{SSIO_2}	S	-	-	-	-	-	-	-	I/O ground		-
32	-	V_{DDIO_2}	S	-	-	-	-	-	-	-	I/O power supply		-
33	23	PC6/SPI_MOSI	I/O	**X**	X	X	-	O3	X	X	**Port C6**	SPI master out/ slave in	-
34	24	PC7/SPI_MISO	I/O	**X**	X	X	-	O3	X	X	**Port C7**	SPI master in/ slave out	-
35	-	PG0	I/O	**X**	X	-	-	O1	X	X	**Port G0**	-	-
36	-	PG1	I/O	**X**	X	-	-	O1	X	X	**Port G1**	-	-
37	-	PE3/TIM1_BKIN	I/O	**X**	X	X	-	O1	X	X	**Port E3**	Timer 1 - break input	-
38	-	PE2/I^2C_SDA	I/O	**X**	-	X	-	O1	T(6)	-	**Port E2**	I^2C data	-
39	-	PE1/I^2C_SCL	I/O	**X**	-	X	-	O1	T(6)	-	**Port E1**	I^2C clock	-
40	-	PE0/CLK_CCO	I/O	**X**	X	X	-	O3	X	X	**Port E0**	Configurable clock output	-
41	25	PD0/TIM3_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 3 - channel 2	TIM1_BKIN [AFR3]/ CLK_CCO [AFR2]
42	26	PD1/SWIM(7)	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	-
43	27	PD2/TIM3_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	Timer 3 - channel 1	TIM2_CH3 [AFR1]
44	28	PD3/TIM2_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2	ADC_ETR [AFR0]
45	29	PD4/TIM2_CH1/ BEEP	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1	BEEP output [AFR7]
46	30	PD5/ LINUART_TX	I/O	**X**	X	X	-	O1	X	X	**Port D5**	LINUART data transmit	-

Table 8. STM8AF6246/48/66/68 (32 Kbyte) microcontroller pin description(1)(2) (continued)

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	VFQFPN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
47	31	PD6/ LINUART_RX	I/O	**X**	X	X	-	O1	X	X	**Port D6**	LINUART data receive	-
48	32	PD7/TLI(8)	I/O	**X**	X	X	-	O1	X	X	**Port D7**	Top level interrupt	-

1. Refer to *Table 7* for the definition of the abbreviations.
2. Reset state is shown in bold.
3. In Halt/Active-halt mode this pad behaves in the following way:
   - the input/output path is disabled
   - if the HSE clock is used for wakeup, the internal weak pull up is disabled
   - if the HSE clock is off, internal weak pull up setting from corresponding OR bit is used
   By managing the OR bit correctly, it must be ensured that the pad is not left floating during Halt/Active-halt.
4. On this pin, a pull-up resistor as specified in *Table 35*. I/O static characteristics is enabled during the reset phase of the product.
5. AIN12 is not selectable in ADC scan mode or with analog watchdog.
6. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, week pull-up, and protection diode to V_{DD} are not implemented)
7. The PD1 pin is in input pull-up during the reset phase and after reset release.
8. If this pin is configured as interrupt pin, it will trigger the TLI.

6.2 Alternate function remapping

As shown in the rightmost column of *Table 8*, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. Refer to *Section 9: Option bytes on page 44*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016).

7 Memory and register map

7.1 Memory map

Figure 5. Register and memory map of STM8A products

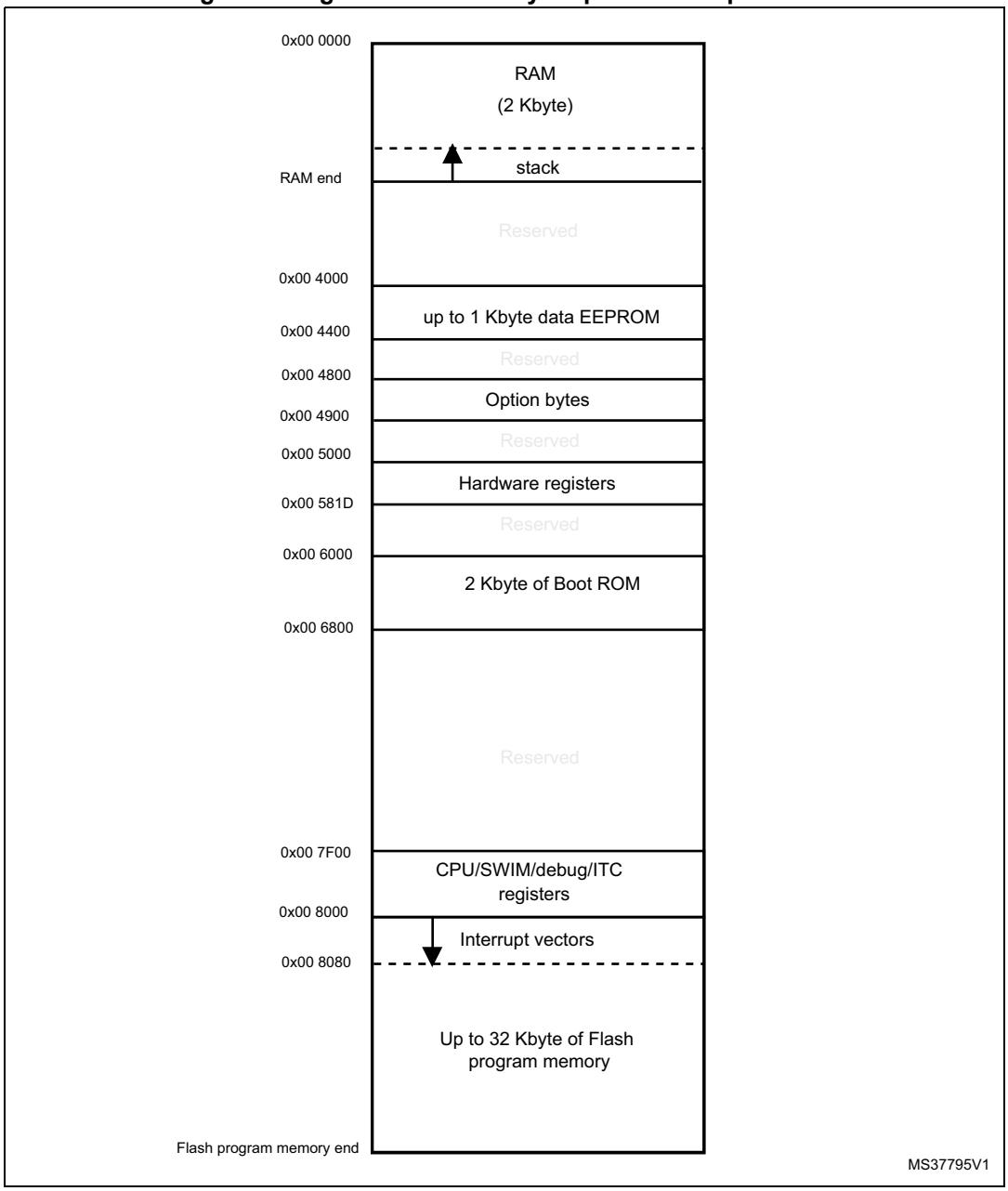


Table 10. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX(1)
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX(1)
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00
0x00 501E	Port G	PG_ODR	Port G data output latch register	0x00
0x00 501F		PG_IDR	Port G input pin value register	0xXX(1)
0x00 5020		PG_DDR	Port G data direction register	0x00
0x00 5021		PG_CR1	Port G control register 1	0x00
0x00 5022		PG_CR2	Port G control register 2	0x00

1. Depends on the external circuitry.

Table 11. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 505A	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 505B		FLASH_CR2	Flash control register 2	0x00
0x00 505C		FLASH_NCR2	Flash complementary control register 2	0xFF
0x00 505D		FLASH_FPR	Flash protection register	0x00
0x00 505E		FLASH_NFPR	Flash complementary protection register	0xFF
0x00 505F		FLASH_IAPSR	Flash in-application programming status register	0x40
0x00 5060 to 0x00 5061	Reserved area (2 bytes)			
0x00 5062	Flash	FLASH_PUKR	Flash Program memory unprotection register	0x00
0x00 5063	Reserved area (1 byte)			
0x00 5064	Flash	FLASH_DUKR	Data EEPROM unprotection register	0x00
0x00 5065 to 0x00 509F	Reserved area (59 bytes)			

Table 15. Option bytes (continued)

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 480B	TMU	OPT6	TMU[3:0]								0x00
0x00 480C		NOPT6	NTMU[3:0]								0xFF
0x00 480D	Flash wait states	OPT7	Reserved							WAIT STATE	0x00
0x00 480E		NOPT7	Reserved							NWAIT STATE	0xFF
0x00 480F	Reserved										
0x00 4810	TMU	OPT8	TMU_KEY 1 [7:0]								0x00
0x00 4811		OPT9	TMU_KEY 2 [7:0]								0x00
0x00 4812		OPT10	TMU_KEY 3 [7:0]								0x00
0x00 4813		OPT11	TMU_KEY 4 [7:0]								0x00
0x00 4814		OPT12	TMU_KEY 5 [7:0]								0x00
0x00 4815		OPT13	TMU_KEY 6 [7:0]								0x00
0x00 4816		OPT14	TMU_KEY 7 [7:0]								0x00
0x00 4817		OPT15	TMU_KEY 8 [7:0]								0x00
0x00 4818		OPT16	TMU_MAXATT [7:0]								0xC7
0x00 4819 to 487D	Reserved										
0x00 487E	Boot-loader(1)	OPT17	BL [7:0]								0x00
0x00 487F		NOPT17	NBL[7:0]								0xFF

1. This option consists of two bytes that must have a complementary value in order to be valid. If the option is invalid, it has no effect on EMC reset.

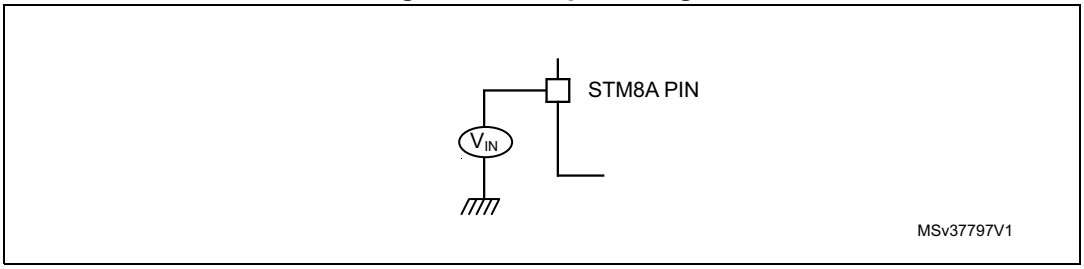
Table 16. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]: Memory readout protection (ROP)** 0xAA: Enable readout protection (write access via SWIM protocol) *Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[5:0]: User boot code area** 0x00: No UBC, no write-protection 0x01: Page 0 to 1 defined as UBC, memory write-protected 0x02: Page 0 to 3 defined as UBC, memory write-protected 0x03 to 0x3F: Pages 4 to 63 defined as UBC, memory write-protected *Note: Refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) section on Flash/EEPROM write protection for more details.*
OPT2	**AFR7: Alternate function remapping option 7** 0: Port D4 alternate function = TIM2_CH1 1: Port D4 alternate function = BEEP **AFR6: Alternate function remapping option 6** 0: Port B5 alternate function = AIN5, port B4 alternate function = AIN4 1: Port B5 alternate function = I^2C_SDA, port B4 alternate function = I^2C_SCL. **AFR5: Alternate function remapping option 5** 0: Port B3 alternate function = AIN3, port B2 alternate function = AIN2, port B1 alternate function = AIN1, port B0 alternate function = AIN0. 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_CH3N, port B1 alternate function = TIM1_CH2N, port B0 alternate function = TIM1_CH1N. **AFR4: Alternate function remapping option 4** Reserved, bit must be kept at “0” **AFR3: Alternate function remapping option 3** 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = TIM1_BKIN **AFR2: Alternate function remapping option 2** 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = CLK_CCO *Note: AFR2 option has priority over AFR3 if both are activated* **AFR1: Alternate function remapping option 1** 0: Port A3 alternate function = TIM2_CH3, port D2 alternate function TIM3_CH1. 1: Port A3 alternate function = TIM3_CH1, port D2 alternate function TIM2_CH3. **AFR0: Alternate function remapping option 0** 0: Port D3 alternate function = TIM2_CH2 1: Port D3 alternate function = ADC_ETR

10.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 7. Pin input voltage



10.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 17. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (PE1, PE2)(2)	V_{SS} - 0.3	6.5	V
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{DD} \rvert$	Variations between different power pins	-	50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins	-	50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 76*		

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

2. Guaranteed by design.
3. Data based on characterization results, not tested in production.

Figure 20. Typical V_{IL} and V_{IH} vs V_{DD} @ four temperatures

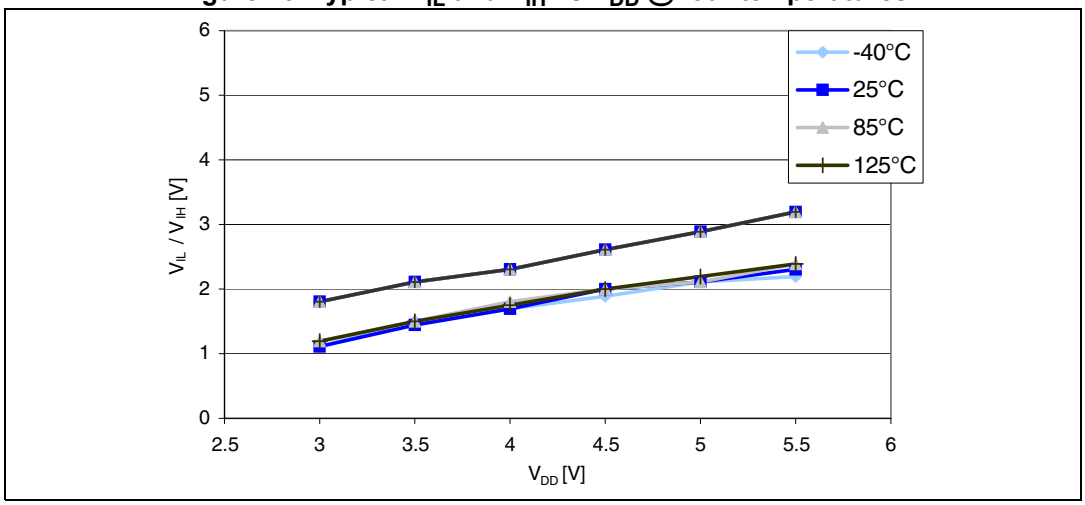
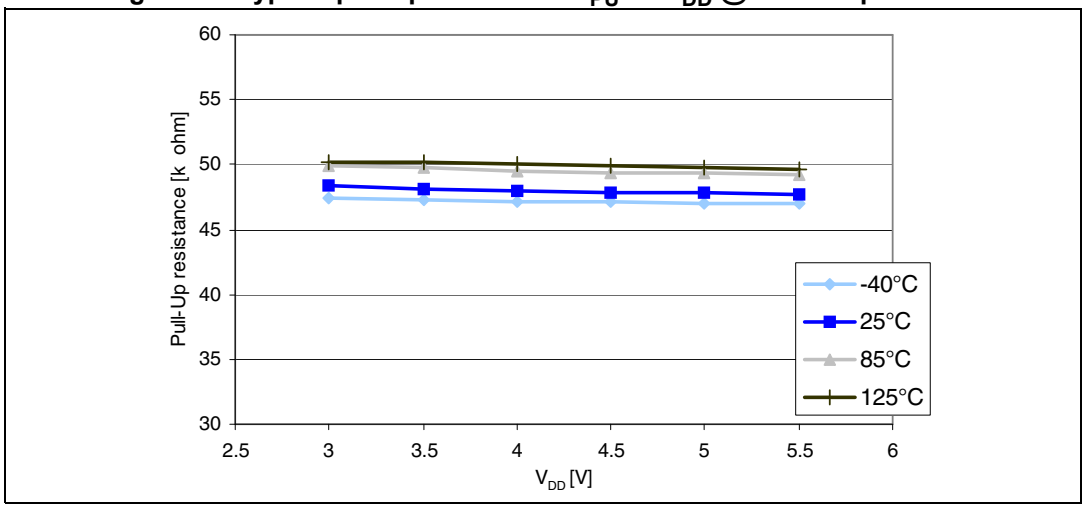


Figure 21. Typical pull-up resistance R_{PU} vs V_{DD} @ four temperatures



10.3.7 Reset pin characteristics

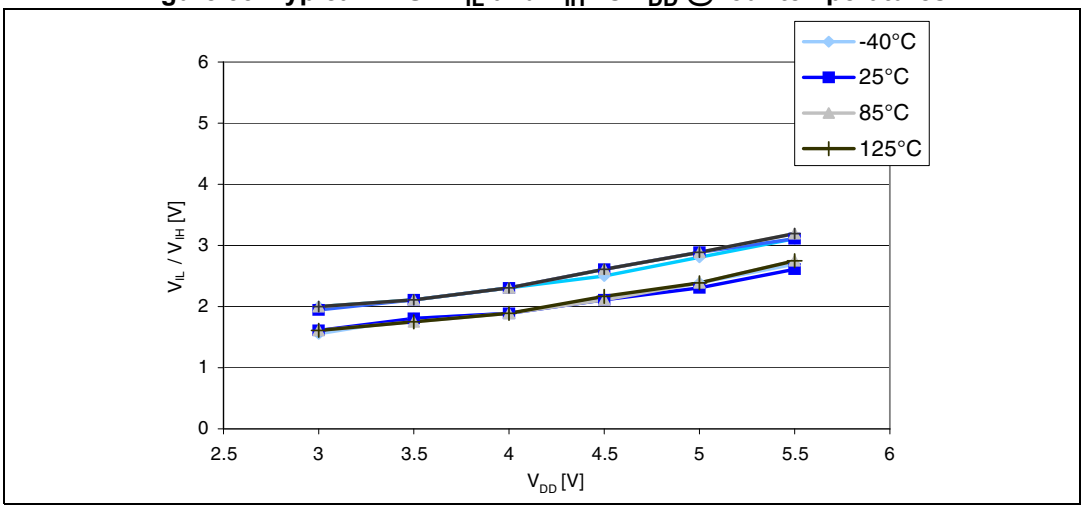
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 36. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)	-	V_{SS}	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage(1)	-	0.7 x V_{DD}	-	V_{DD}	
$V_{OL(NRST)}$	NRST output low level voltage(1)	I_{OL}= 3 mA	-	-	0.6	
$R_{PU(NRST)}$	NRST pull-up resistor	-	30	40	60	kΩ
t_{IFP}	NRST input filtered pulse(1)	-	85	-	315	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse duration(2)	-	500	-	-	

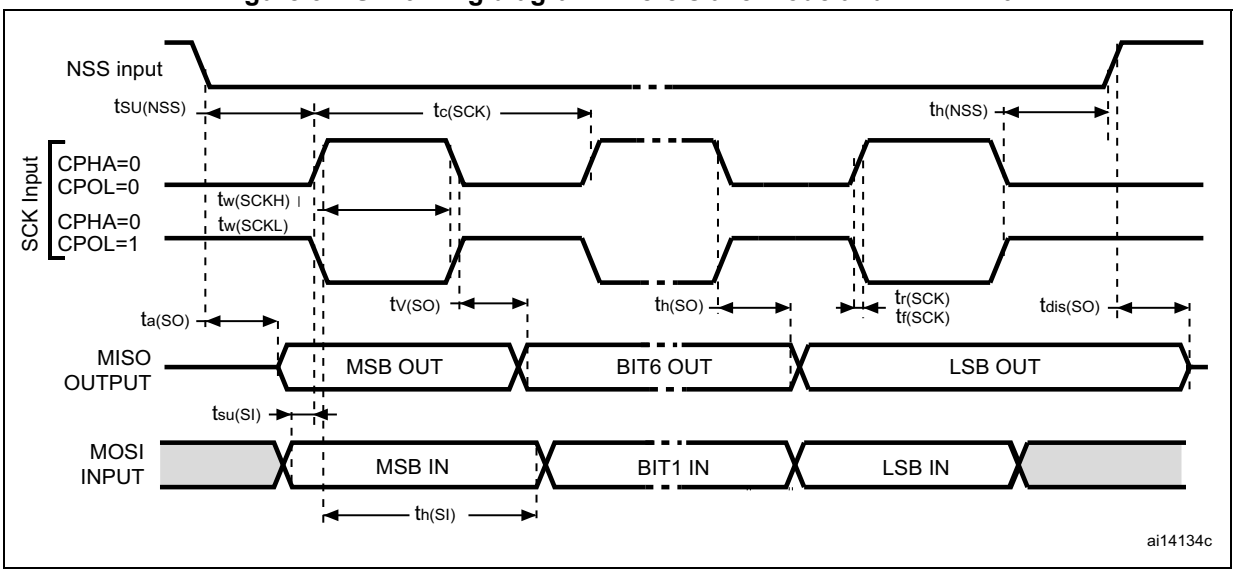
1. Data based on characterization results, not tested in production.
2. Data guaranteed by design, not tested in production.

Figure 33. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ four temperatures



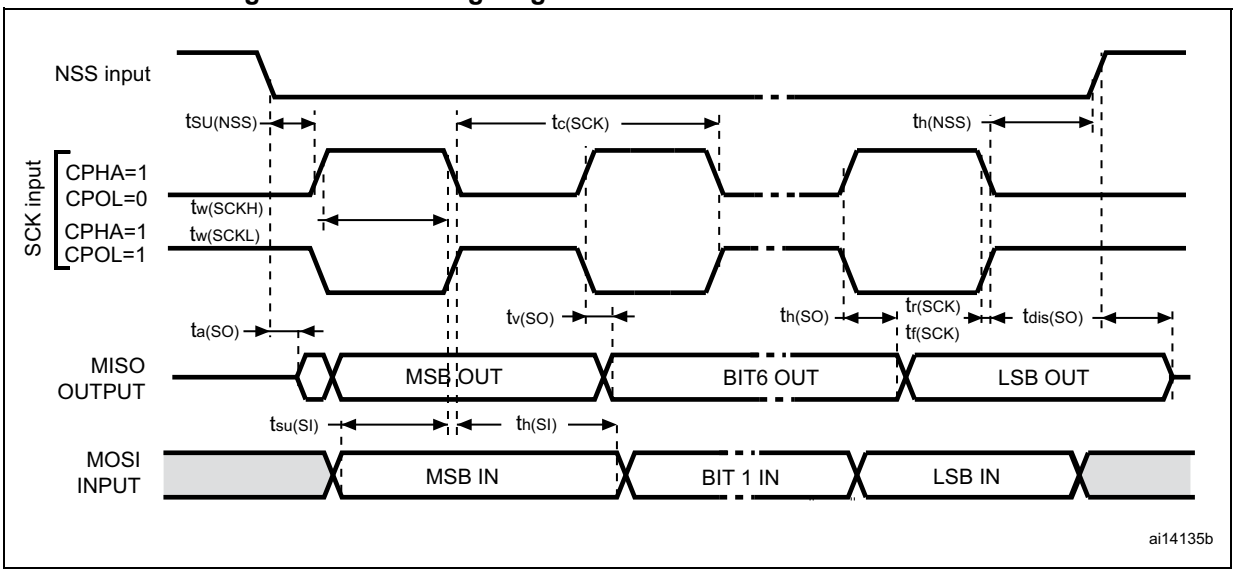
3. Values based on design simulation and/or characterization results, and not tested in production.
4. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
5. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 37. SPI timing diagram where slave mode and CPHA = 0



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 38. SPI timing diagram where slave mode and CPHA = 1



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

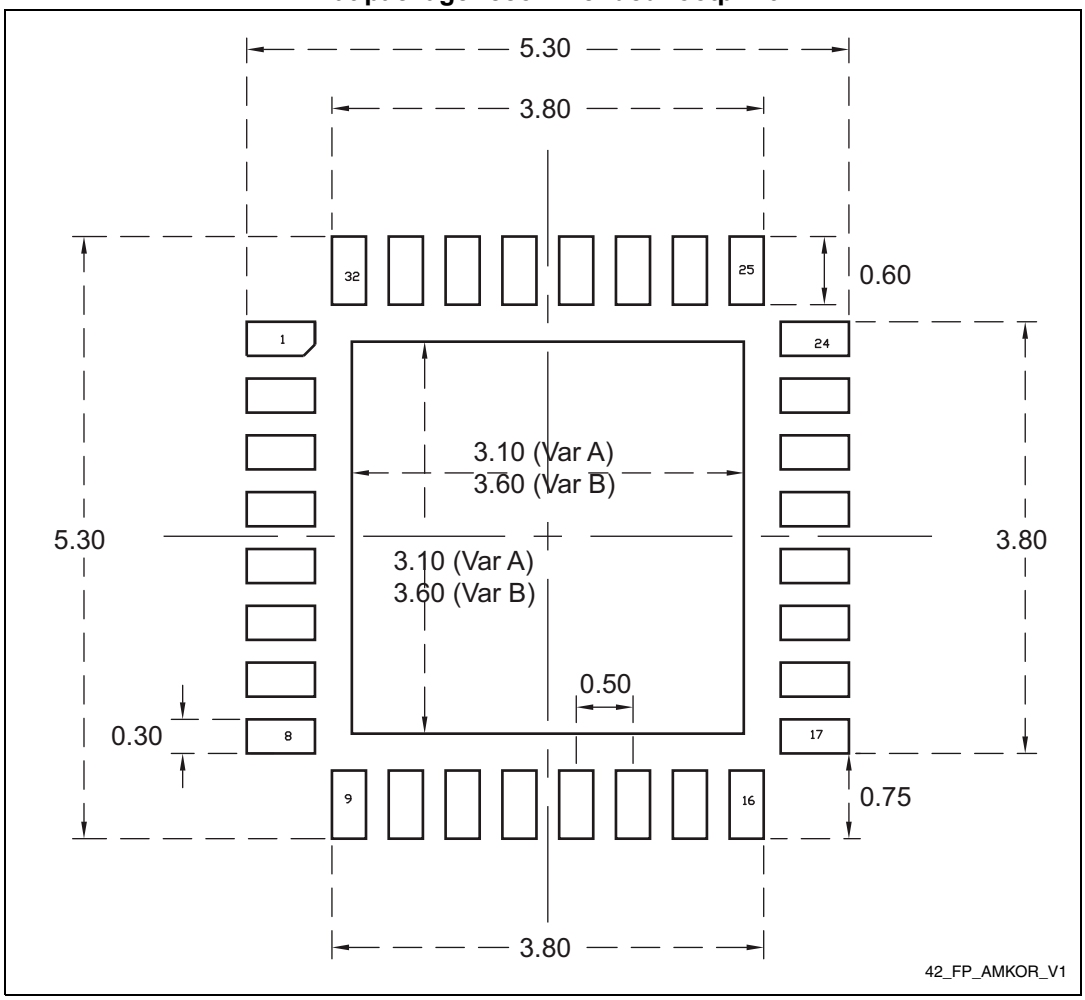
10.3.10 I²C interface characteristics

Table 39. I²C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	-	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time (V_{DD} = 3 to 5.5 V)	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time (V_{DD} = 3 to 5.5 V)	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

Figure 43. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint

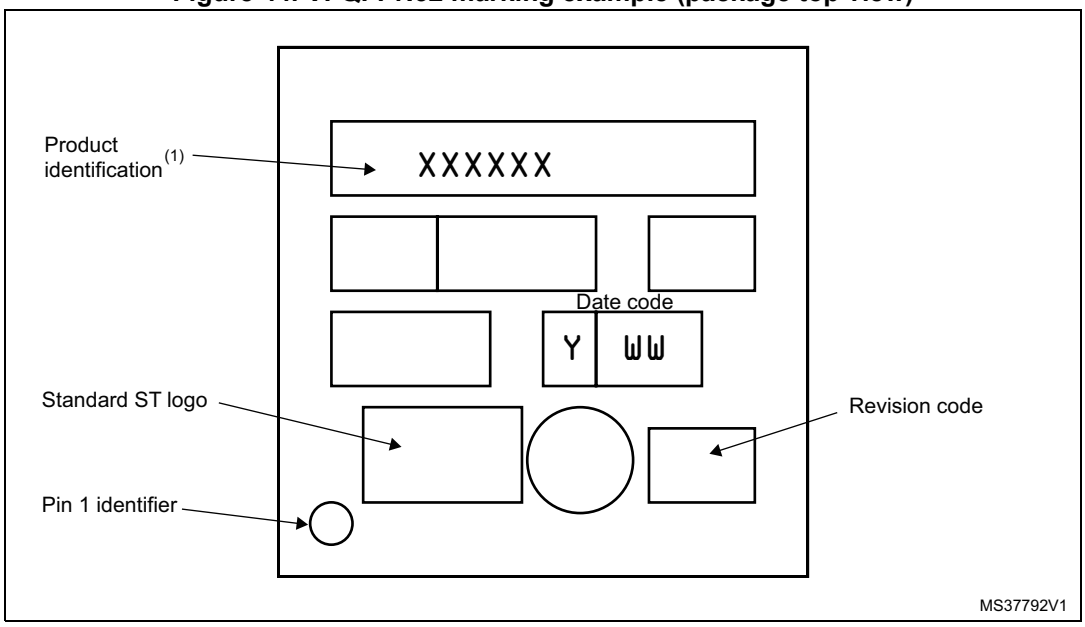


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 44. VFQFPN32 marking example (package top view)



Assuming the following application conditions:

Maximum ambient temperature T_{Amax}= 82 °C (measured according to JESD51-2), I_{DDmax} = 14 mA, V_{DD} = 5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 14 mA x 5 V= 70 mW

P_{IOmax} = 20 x 8 mA x 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} 64 mW:

P_{Dmax} = 70 mW + 64 mW

Thus: P_{Dmax} = 134 mW.

Using the values obtained in *Table 49: Thermal characteristics* T_{Jmax} is calculated as follows:

For LQFP64 46 °C/W

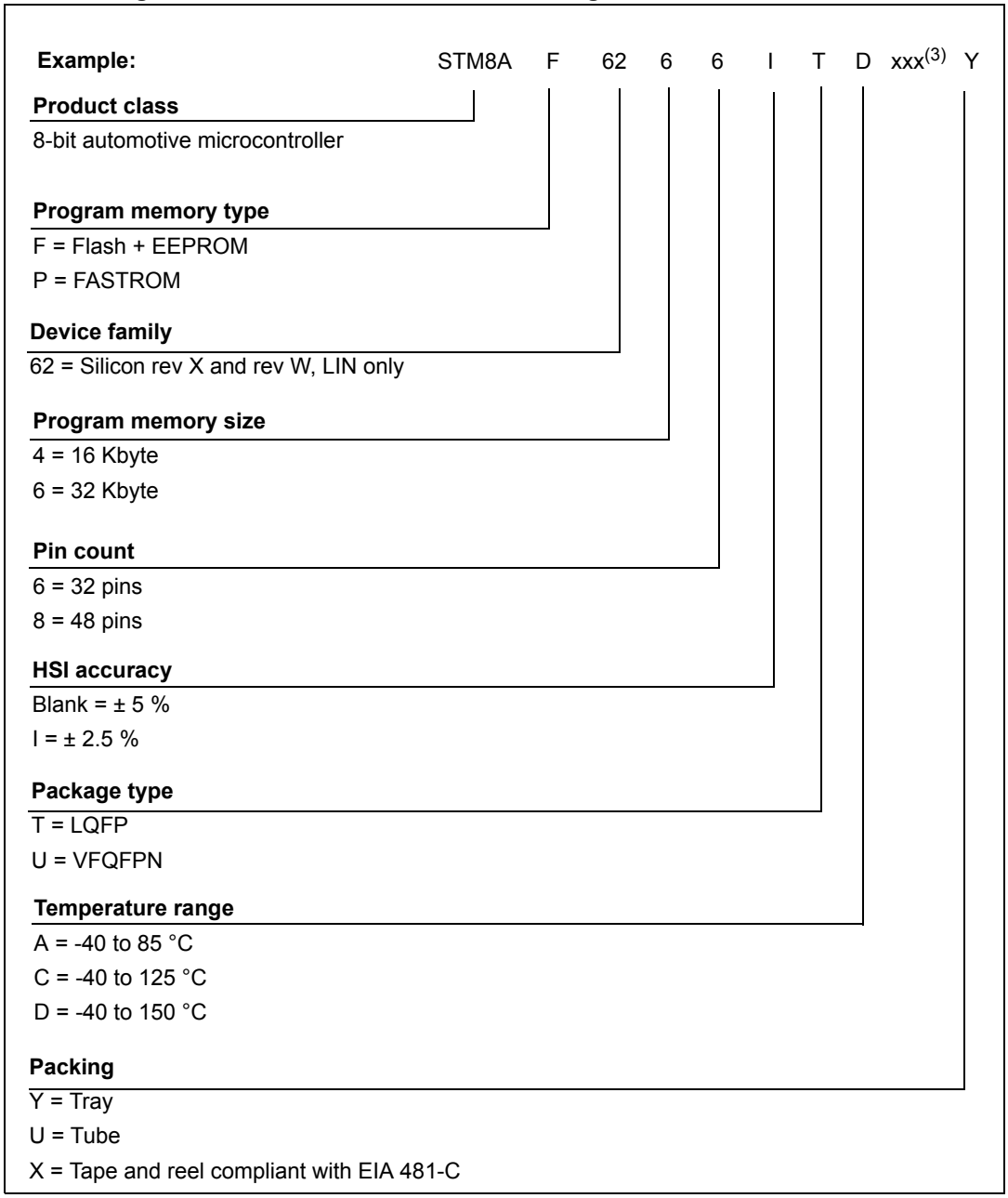
T_{Jmax} = 82 °C + (46 °C/W x 134 mW) = 82 °C + 6 °C = 88 °C

This is within the range of the suffix C version parts (-40 < T_J < 125 °C).

Parts must be ordered at least with the temperature range suffix C.

12 Ordering information

Figure 51. STM8AF6246/48/66/68 ordering information scheme(1) (2)



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the nearest ST Sales Office.
2. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.
3. Customer specific FASTROM code or custom device configuration. This field shows ‘SSS’ if the device contains a super set silicon, usually equipped with bigger memory and more I/Os. This silicon is supposed to be replaced later by the target silicon.

Table 50. Document revision history (continued)

Date	Revision	Changes
31-Jan-2011	5	Modified references to reference manual, and Flash programming manual in the whole document. Added reference to AEC Q100 standard on cover page. Renamed timer types as follows: – Auto-reload timer to general purpose timer – Multipurpose timer to advanced control timer – System timer to basic timer Introduced concept of medium density Flash program memory. Updated timer names in *Figure: STM8A block diagram.* Added TMU brief description in *Section: Flash program and data EEPROM*, and updated TMU_MAXATT description in *Table: Option byte description*. Updated clock sources in clock controller features. Changed 16MHZTRIM0 to HSITRIM bit in *Section: User trimming.* Added *Table: Peripheral clock gating bits.* Updated *Section: Low-power operating modes.* Added calibration using TIM3 in *Section: Auto-wakeup counter.* Added *Table: ADC naming* and *Table: Communication peripheral naming correspondence.* Added *Note 1* related AIN12 pin in *Section: Analog-to-digital converter (ADC)* and *Table: STM8AF61xx/62xx (32 Kbyte) microcontroller pin description.* Updated SPI data rate to 10 Mbit/s or $f_{MASTER}/2$ in *Section: Serial peripheral interface (SPI).* Added reset state in *Table: Legend/abbreviation.* *Table: STM8AF61xx/62xx (32 Kbyte) microcontroller pin description:* added *Note 7* related to PD1/SWIM, modified *Note 6,* corrected wpu input for PE1 and PE2, and renamed TIMn_CCx and TIMn_NCCx to TIMn_CHx and TIMn_CHxN, respectively. ***Section: Register map:*** Replaced tables describing register maps and reset values for non-volatile memory, global configuration, reset status, clock controller, interrupt controller, timers, communication interfaces, and ADC, by *Table: General hardware register map*. Added *Note 1* for Px_IDR registers in *Table: I/O port hardware register map.* Updated register reset values for Px_IDR registers. Added SWIM and debug module register map.