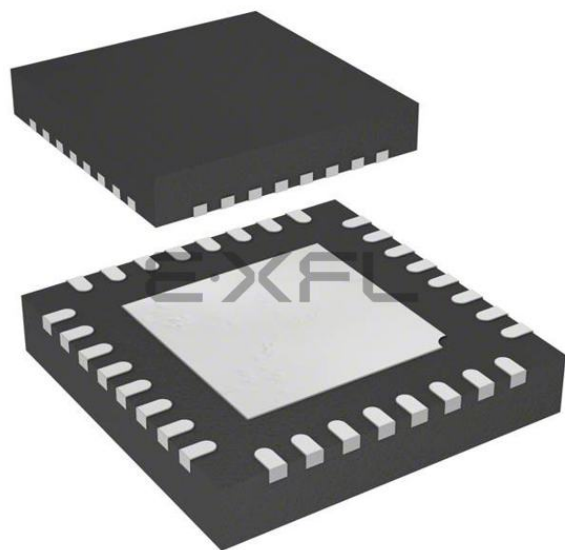




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6266udx

5.7.4	Advanced control and general purpose timers	21
5.7.5	Basic timer	22
5.8	Analog-to-digital converter (ADC)	23
5.9	Communication interfaces	23
5.9.1	Serial peripheral interface (SPI)	24
5.9.2	Inter integrated circuit (I ² C) interface	24
5.9.3	Universal asynchronous receiver/transmitter with LIN support (LINUART)	25
5.10	Input/output specifications	26
6	Pinouts and pin description	27
6.1	Package pinouts	27
6.2	Alternate function remapping	31
7	Memory and register map	32
7.1	Memory map	32
7.2	Register map	33
8	Interrupt table	43
9	Option bytes	44
10	Electrical characteristics	49
10.1	Parameter conditions	49
10.1.1	Minimum and maximum values	49
10.1.2	Typical values	49
10.1.3	Typical curves	49
10.1.4	Loading capacitor	49
10.1.5	Pin input voltage	50
10.2	Absolute maximum ratings	50
10.3	Operating conditions	52
10.3.1	VCAP external capacitor	54
10.3.2	Supply current characteristics	54
10.3.3	External clock sources and timing characteristics	57
10.3.4	Internal clock sources and timing characteristics	59
10.3.5	Memory characteristics	62
10.3.6	I/O port pin characteristics	63

List of figures

Figure 1.	STM8AF6246/48/66/68 block diagram	12
Figure 2.	Flash memory organization of STM8AF6246/48/66/68	16
Figure 3.	VFQFPN/LQFP 32-pin pinout	27
Figure 4.	LQFP 48-pin pinout	28
Figure 5.	Register and memory map of STM8A products	32
Figure 6.	Pin loading conditions	49
Figure 7.	Pin input voltage	50
Figure 8.	f_{CPUmax} versus V_{DD}	52
Figure 9.	External capacitor C_{EXT}	54
Figure 10.	Typ. $I_{DD(RUN)HSE}$ vs. V_{DD} @ $f_{CPU} = 16$ MHz, peripheral = on	56
Figure 11.	Typ. $I_{DD(RUN)HSE}$ vs. f_{CPU} @ $V_{DD} = 5.0$ V, peripheral = on	56
Figure 12.	Typ. $I_{DD(RUN)HSI}$ vs. V_{DD} @ $f_{CPU} = 16$ MHz, peripheral = off	57
Figure 13.	Typ. $I_{DD(WFI)HSE}$ vs. V_{DD} @ $f_{CPU} = 16$ MHz, peripheral = on	57
Figure 14.	Typ. $I_{DD(WFI)HSE}$ vs. f_{CPU} @ $V_{DD} = 5.0$ V, peripheral = on	57
Figure 15.	Typ. $I_{DD(WFI)HSI}$ vs. V_{DD} @ $f_{CPU} = 16$ MHz, peripheral = off	57
Figure 16.	HSE external clock source	58
Figure 17.	HSE oscillator circuit diagram	59
Figure 18.	Typical HSI frequency vs V_{DD}	60
Figure 19.	Typical LSI frequency vs V_{DD}	61
Figure 20.	Typical V_{IL} and V_{IH} vs V_{DD} @ four temperatures	64
Figure 21.	Typical pull-up resistance R_{PU} vs V_{DD} @ four temperatures	64
Figure 22.	Typical pull-up current I_{pu} vs V_{DD} @ four temperatures	65
Figure 23.	Typ. V_{OL} @ $V_{DD} = 3.3$ V (standard ports)	65
Figure 24.	Typ. V_{OL} @ $V_{DD} = 5.0$ V (standard ports)	65
Figure 25.	Typ. V_{OL} @ $V_{DD} = 3.3$ V (true open drain ports)	65
Figure 26.	Typ. V_{OL} @ $V_{DD} = 5.0$ V (true open drain ports)	65
Figure 27.	Typ. V_{OL} @ $V_{DD} = 3.3$ V (high sink ports)	66
Figure 28.	Typ. V_{OL} @ $V_{DD} = 5.0$ V (high sink ports)	66
Figure 29.	Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 3.3$ V (standard ports)	66
Figure 30.	Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 5.0$ V (standard ports)	66
Figure 31.	Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 3.3$ V (high sink ports)	66
Figure 32.	Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 5.0$ V (high sink ports)	66
Figure 33.	Typical NRST V_{IL} and V_{IH} vs V_{DD} @ four temperatures	67
Figure 34.	Typical NRST pull-up resistance R_{PU} vs V_{DD}	68
Figure 35.	Typical NRST pull-up current I_{pu} vs V_{DD}	68
Figure 36.	Recommended reset pin protection	68
Figure 37.	SPI timing diagram where slave mode and CPHA = 0	70
Figure 38.	SPI timing diagram where slave mode and CPHA = 1	70
Figure 39.	SPI timing diagram - master mode	71
Figure 40.	Typical application with ADC	73
Figure 41.	ADC accuracy characteristics	74
Figure 42.	VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline	78
Figure 43.	VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint	80
Figure 44.	VFQFPN32 marking example (package top view)	81
Figure 45.	LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline	82
Figure 46.	LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package	

1. Legend:
 - ADC: Analog-to-digital converter
 - beCAN: Controller area network
 - BOR: Brownout reset
 - I²C: Inter-integrated circuit multimaster interface
 - IWDG: Independent window watchdog
 - LINUART: Local interconnect network universal asynchronous receiver transmitter
 - POR: Power on reset
 - SPI: Serial peripheral interface
 - SWIM: Single wire interface module
 - USART: Universal synchronous asynchronous receiver transmitter
 - Window WDG: Window watchdog

5 Product overview

This section describes the family features that are implemented in the products covered by this datasheet.

For more detailed information on each feature please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).

5.1 STM8A central processing unit (CPU)

The 8-bit STM8A core is a modern CISC core and has been designed for code efficiency and performance. It contains 21 internal registers (six directly addressable in each execution context), 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

5.1.1 Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus with single cycle fetching for most instructions
- X and Y 16-bit index registers, enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter with 16-Mbyte linear memory space
- 16-bit stack pointer with access to a 64 Kbyte stack
- 8-bit condition code register with seven condition flags for the result of the last instruction.

5.1.2 Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for efficient implementation of local variables and parameter passing

5.1.3 Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

5.9.1 Serial peripheral interface (SPI)

The devices covered by this datasheet contain one SPI. The SPI is available on all the supported packages.

- Maximum speed: 10 Mbit/s or $f_{\text{MASTER}}/2$ both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave mode/master mode management by hardware or software for both master and slave
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Dedicated transmission and reception flags with interrupt capability
- SPI bus busy status flag
- Hardware CRC feature for reliable communication:
 - CRC value can be transmitted as last byte in Tx mode
 - CRC error checking for last received byte

5.9.2 Inter integrated circuit (I²C) interface

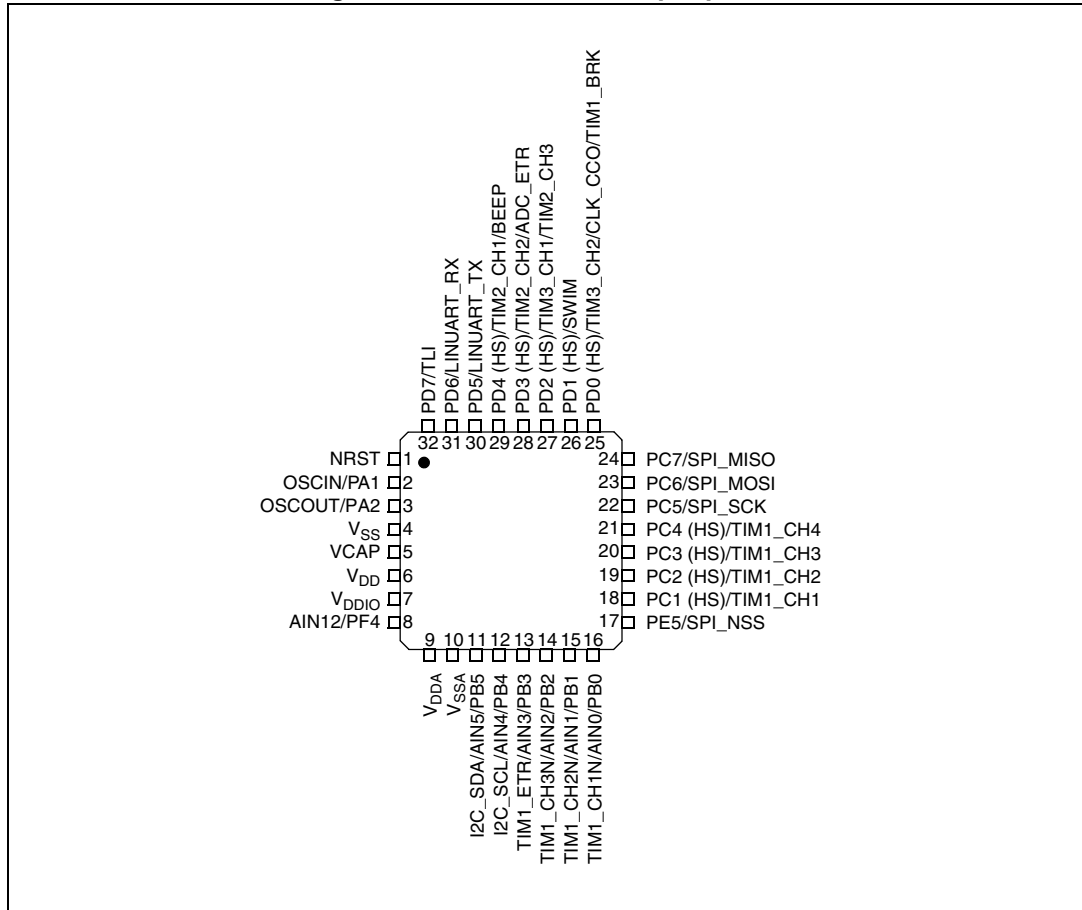
The devices covered by this datasheet contain one I²C interface. The interface is available on all the supported packages.

- I²C master features:
 - Clock generation
 - Start and stop generation
- I²C slave features:
 - Programmable I²C address detection
 - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
 - Standard speed (up to 100 kHz),
 - Fast speed (up to 400 kHz)
- Status flags:
 - Transmitter/receiver mode flag
 - End-of-byte transmission flag
 - I²C busy flag
- Error flags:
 - Arbitration lost condition for master mode
 - Acknowledgment failure after address/data transmission
 - Detection of misplaced start or stop condition
 - Overrun/underrun if clock stretching is disabled

6 Pinouts and pin description

6.1 Package pinouts

Figure 3. VFQFPN/LQFP 32-pin pinout



1. (HS) high sink capability.

Table 8. STM8AF6246/48/66/68 (32 Kbyte) microcontroller pin description⁽¹⁾⁽²⁾ (continued)

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	VFQFPN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
47	31	PD6/ LINUART_RX	I/O	X	X	X	-	O1	X	X	Port D6	LINUART data receive	-
48	32	PD7/TLI ⁽⁸⁾	I/O	X	X	X	-	O1	X	X	Port D7	Top level interrupt	-

1. Refer to [Table 7](#) for the definition of the abbreviations.
2. Reset state is shown in bold.
3. In Halt/Active-halt mode this pad behaves in the following way:
 - the input/output path is disabled
 - if the HSE clock is used for wakeup, the internal weak pull up is disabled
 - if the HSE clock is off, internal weak pull up setting from corresponding OR bit is used
 By managing the OR bit correctly, it must be ensured that the pad is not left floating during Halt/Active-halt.
4. On this pin, a pull-up resistor as specified in [Table 35](#). I/O static characteristics is enabled during the reset phase of the product.
5. AIN12 is not selectable in ADC scan mode or with analog watchdog.
6. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to V_{DD} are not implemented)
7. The PD1 pin is in input pull-up during the reset phase and after reset release.
8. If this pin is configured as interrupt pin, it will trigger the TLI.

6.2 Alternate function remapping

As shown in the rightmost column of [Table 8](#), some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. Refer to [Section 9: Option bytes on page 44](#). When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016).

Table 9. Memory model for the devices covered in this datasheet

Flash program memory size	Flash program memory end address	RAM size	RAM end address	Stack roll-over address
32K	0x00 0FFFF	2K	0x00 07FF	0x00 0600
16K	0x00 0BFFF			

7.2 Register map

In this section the memory and register map of the devices covered by this datasheet is described. For a detailed description of the functionality of the registers, refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016.

Table 10. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX ⁽¹⁾
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX ⁽¹⁾
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PC_IDR	Port C input pin value register	0xXX ⁽¹⁾
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX ⁽¹⁾
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00

Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5240	LINUART	UART2_SR	LINUART status register	0xC0
0x00 5241		UART2_DR	LINUART data register	0xFF
0x00 5242		UART2_BRR1	LINUART baud rate register 1	0x00
0x00 5243		UART2_BRR2	LINUART baud rate register 2	0x00
0x00 5244		UART2_CR1	LINUART control register 1	0x00
0x00 5245		UART2_CR2	LINUART control register 2	0x00
0x00 5246		UART2_CR3	LINUART control register 3	0x00
0x00 5247		UART2_CR4	LINUART control register 4	0x00
0x00 5248		Reserved		
0x00 5249		UART2_CR6	LINUART control register 6	0x00
0x00 524A to 0x00 524F	Reserved area (6 bytes)			
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00

Table 12. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F81 to 0x00 7F8F	Reserved area (15 bytes)			
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM debug module control register 1	0x00
0x00 7F97		DM_CR2	DM debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 bytes)			

1. Accessible by debug module only

2. Product dependent value, see [Figure 5: Register and memory map of STM8A products](#).

Table 13. Temporary memory unprotection registers

Address	Block	Register label	Register name	Reset status
0x00 5800	TMU	TMU_K1	Temporary memory unprotection key register 1	0x00
0x00 5801		TMU_K2	Temporary memory unprotection key register 2	0x00
0x00 5802		TMU_K3	Temporary memory unprotection key register 3	0x00
0x00 5803		TMU_K4	Temporary memory unprotection key register 4	0x00
0x00 5804		TMU_K5	Temporary memory unprotection key register 5	0x00
0x00 5805		TMU_K6	Temporary memory unprotection key register 6	0x00
0x00 5806		TMU_K7	Temporary memory unprotection key register 7	0x00
0x00 5807		TMU_K8	Temporary memory unprotection key register 8	0x00
0x00 5808		TMU_CSR	Temporary memory unprotection control and status register	0x00

Table 16. Option byte description (continued)

Option byte no.	Description
OPT12	TMU_KEY 5 [7:0]: Temporary unprotection key 4 Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT13	TMU_KEY 6 [7:0]: Temporary unprotection key 5 Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT14	TMU_KEY 7 [7:0]: Temporary unprotection key 6 Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT15	TMU_KEY 8 [7:0]: Temporary unprotection key 7 Temporary unprotection key: Must be different from 0x00 or 0xFF
OPT16	TMU_MAXATT [7:0]: TMU access failure counter TMU_MAXATT can be initialized with the desired value only if TMU is disabled (TMU[3:0]=0101 in OPT6 option byte). When TMU is enabled, any attempt to temporarily remove the readout protection by using wrong key values increments the counter. When the option byte value reaches 0x08, the Flash memory and data EEPROM are erased.
OPT17	BL [7:0]: Bootloader enable If this option byte is set to 0x55 (complementary value 0xAA) the bootloader program is activated also in case of a programmed code memory (for more details, see the bootloader user manual, UM0560).

10 Electrical characteristics

10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS} .

10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = -40\text{ }^{\circ}\text{C}$, $T_A = 25\text{ }^{\circ}\text{C}$, and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

10.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

10.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 6](#).

Figure 6. Pin loading conditions

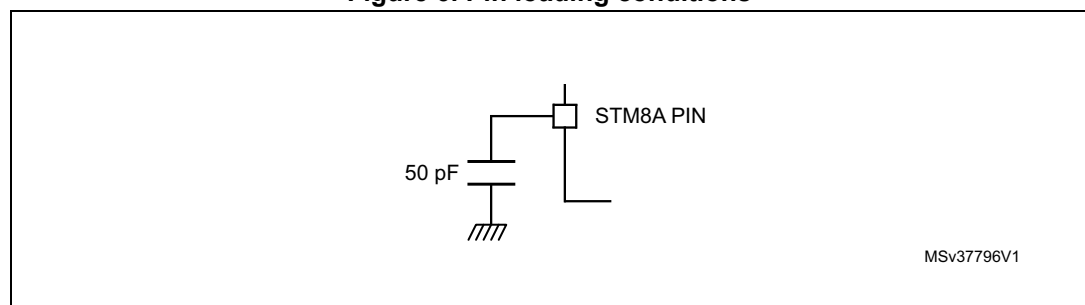


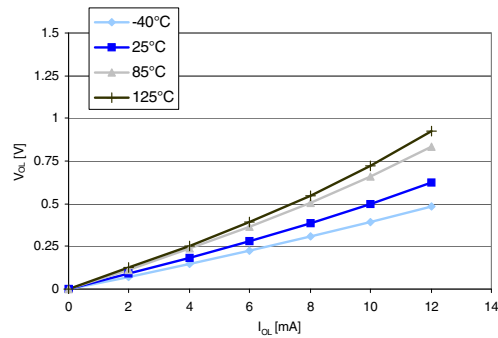
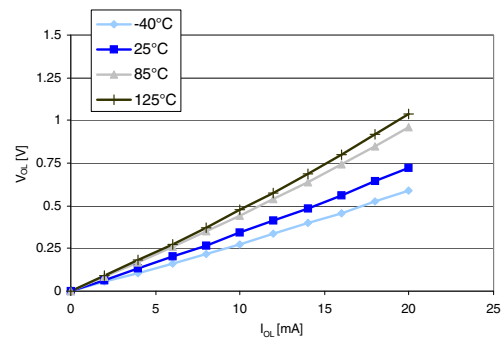
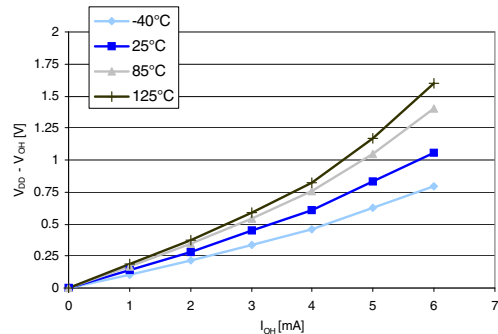
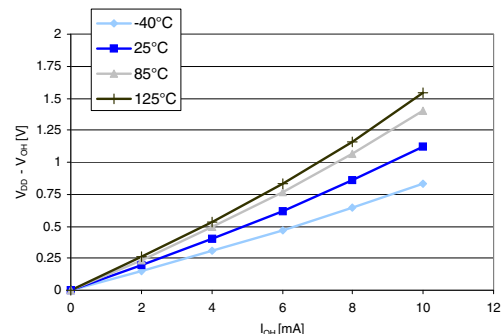
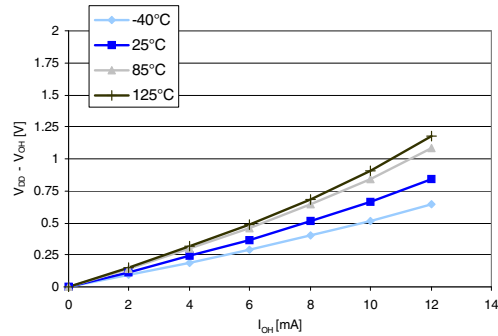
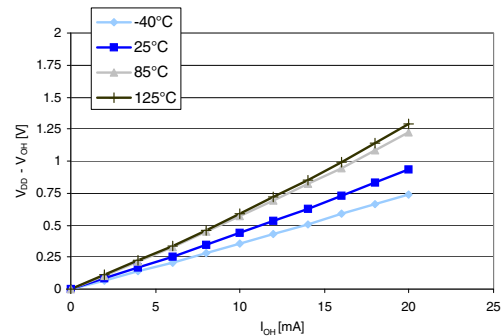
Figure 27. Typ. V_{OL} @ $V_{DD} = 3.3$ V (high sink ports)**Figure 28. Typ. V_{OL} @ $V_{DD} = 5.0$ V (high sink ports)****Figure 29. Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 3.3$ V (standard ports)****Figure 30. Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 5.0$ V (standard ports)****Figure 31. Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 3.3$ V (high sink ports)****Figure 32. Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 5.0$ V (high sink ports)**

Figure 34. Typical NRST pull-up resistance R_{PU} vs V_{DD}

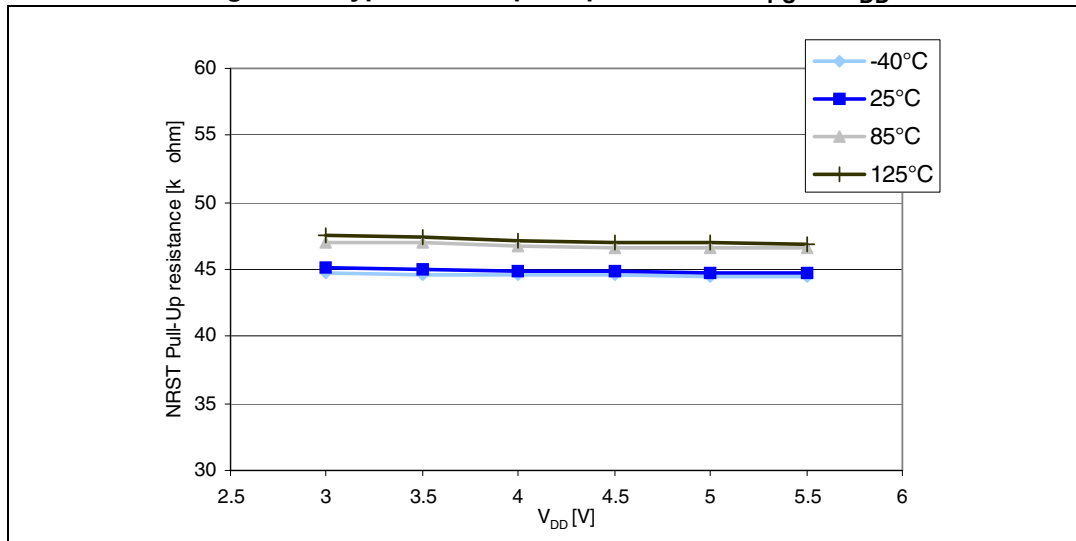
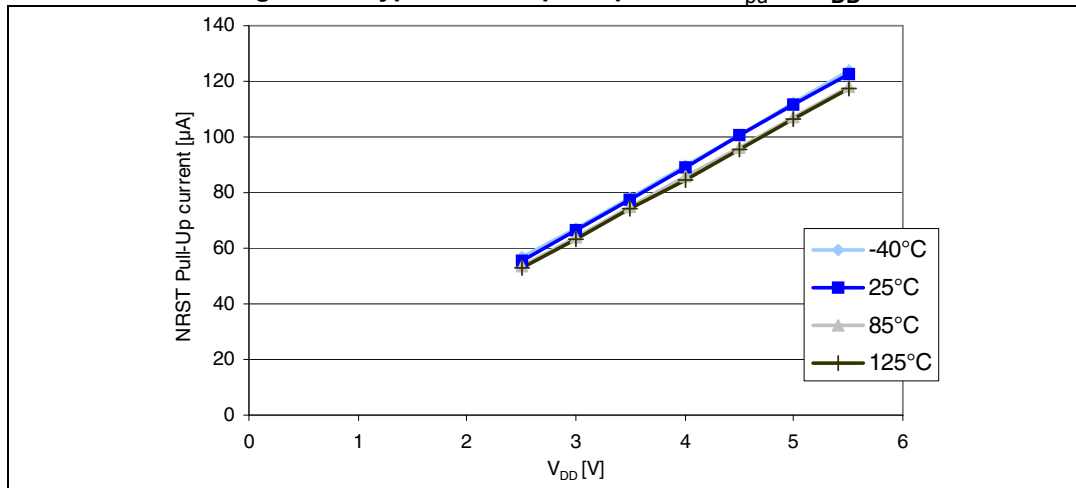
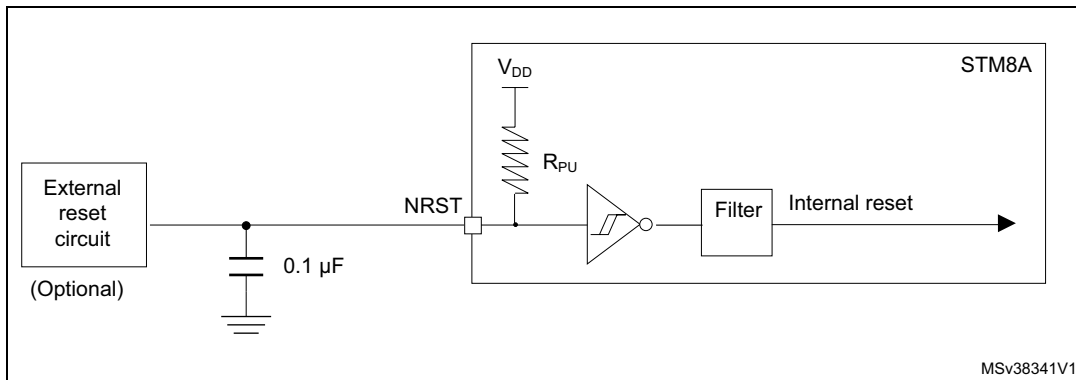


Figure 35. Typical NRST pull-up current I_{PU} vs V_{DD}



The reset network shown in [Figure 36](#) protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below $V_{IL(NRST)}$ max (see [Table 36: NRST pin characteristics](#)), otherwise the reset is not taken into account internally.

Figure 36. Recommended reset pin protection



10.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD:** Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB:** A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 42. EMS data

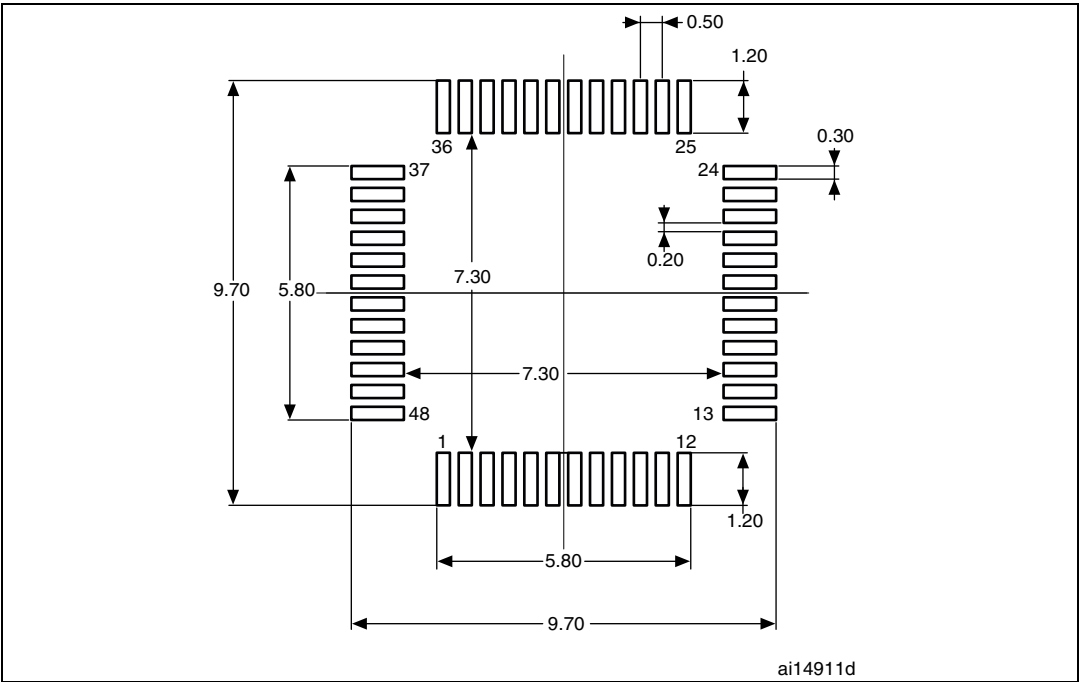
Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, $f_{MASTER} = 16\text{ MHz}$ (HSI clock), Conforms to IEC 1000-4-2	3/B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, $f_{MASTER} = 16\text{ MHz}$ (HSI clock), Conforms to IEC 1000-4-4	4/A

Table 46. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.200	-	-	0.0079	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D2	3.500	3.600	3.700	0.1378	0.1417	0.1457
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E2	3.500	3.600	3.700	0.1378	0.1417	0.1457
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 46. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 47. LQFP48 marking example (package top view)

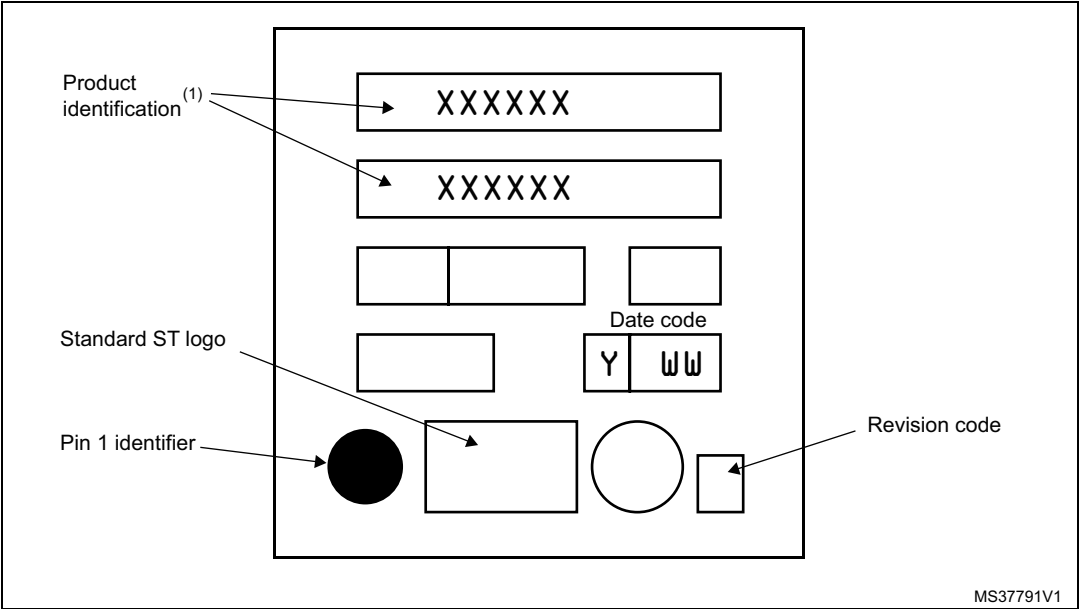
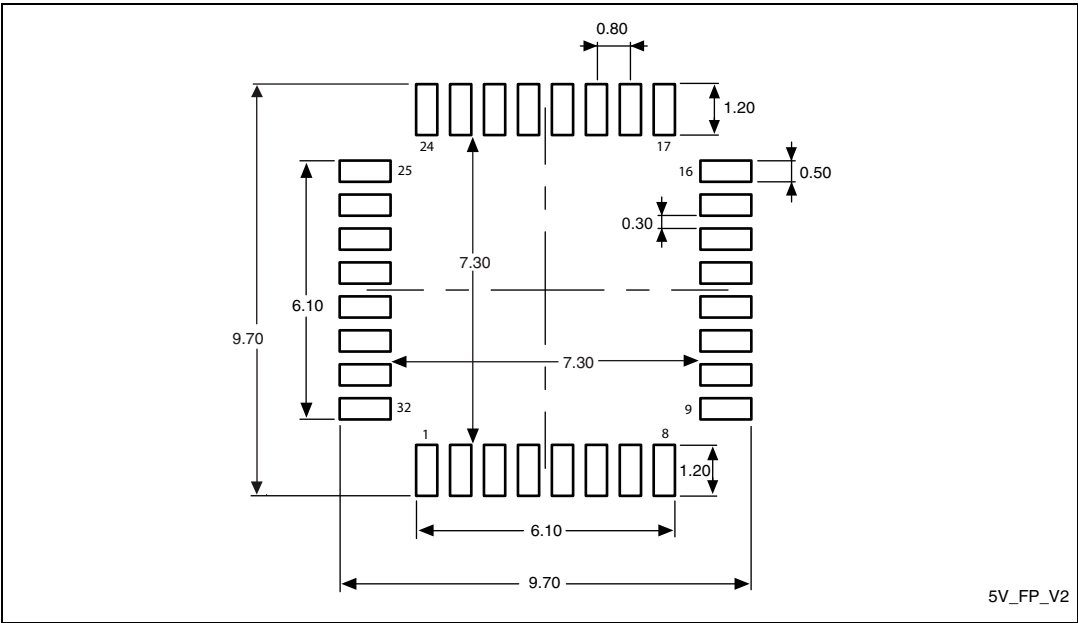


Figure 49. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint

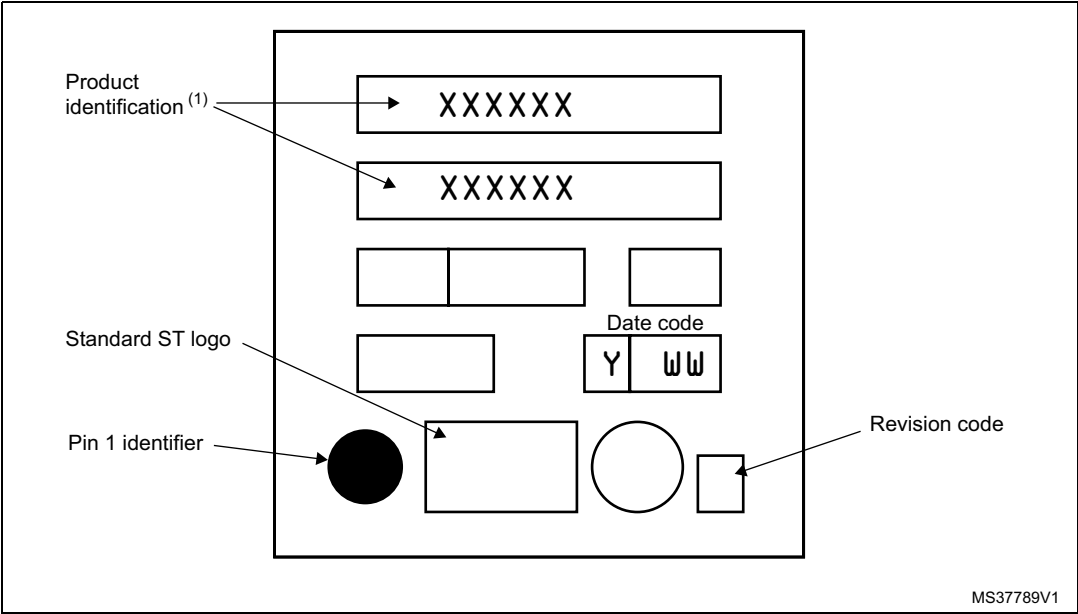


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 50. LQFP32 marking example (package top view)



Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 82\text{ }^{\circ}\text{C}$ (measured according to JESD51-2),
 $I_{DDmax} = 14\text{ mA}$, $V_{DD} = 5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 14\text{ mA} \times 5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

This gives: $P_{INTmax} = 70\text{ mW}$ and $P_{IOmax} = 64\text{ mW}$:

$$P_{Dmax} = 70\text{ mW} + 64\text{ mW}$$

Thus: $P_{Dmax} = 134\text{ mW}$.

Using the values obtained in [Table 49: Thermal characteristics](#) T_{Jmax} is calculated as follows:

For LQFP64 $46\text{ }^{\circ}\text{C/W}$

$$T_{Jmax} = 82\text{ }^{\circ}\text{C} + (46\text{ }^{\circ}\text{C/W} \times 134\text{ mW}) = 82\text{ }^{\circ}\text{C} + 6\text{ }^{\circ}\text{C} = 88\text{ }^{\circ}\text{C}$$

This is within the range of the suffix C version parts ($-40 < T_J < 125\text{ }^{\circ}\text{C}$).

Parts must be ordered at least with the temperature range suffix C.

Table 50. Document revision history (continued)

Date	Revision	Changes
31-Jan-2011	5 (continued)	Renamed Fast Active Halt mode to Active-halt mode with regulator on, and Slow Active Halt mode to Active-halt mode with regulator off. Updated <i>Table: Total current consumption in Halt and Active-halt modes</i>. General conditions for VDD apply, TA = -40 to 55 °C, in particular I_{DD}(FAH) and I_{DD}(SAH) renamed I_{DD}(AH); t_{WU}(FAH) and t_{WU}(SAH) renamed t_{WU}(AH), and temperature condition added. Removed I_{DD}(USART) from <i>Table: Typical peripheral current consumption VDD = 5.0 V</i>. Updated general conditions in <i>Section: Memory characteristics</i>. Modified T_{WE} maximum value in <i>Table: Flash program memory</i> and <i>Table: Data memory</i>. Update I_{lkg ana} maximum value for T_A ranging from -40 to 150 °C in <i>Table: I/O static characteristics</i>. Added t_{IFP}(NRST) and renamed V_F(NRST) t_{IFP} in <i>Table: NRST pin characteristics</i>. Added recommendations concerning NRST pin level above <i>Figure: Recommended reset pin protection</i>, and updated external capacitor value. Added Raisonance compiler in <i>Section: Software tools</i>. Moved know limitations to separate errata sheet.
18-Jul-2012	6	Updated wildcards of document part numbers. <i>Table: Device summary</i>: updated the footnotes to all STM8AF61xx part numbers. <i>Section: Introduction</i>: small text change in first paragraph. <i>Table: STM8AF62xx product line-up</i>: added "P" version for all order codes; updated RAM. <i>Table: STM8AF/H61xx product line-up</i>: added "P" version for all order codes. <i>Figure: STM8A block diagram</i>: updated POR, BOR and WDG; updated LINUART input; added legend. <i>Section: Flash program and data EEPROM</i>: removed non relevant bullet points and added a sentence about the factory programmer. <i>Table: Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers</i>: updated <i>ADC features</i>: updated ADC input range. <i>Table: Memory model for the devices covered in this datasheet</i>: updated 16 Kbyte and 8 Kbyte information. <i>Table: Option bytes</i>: updated factory default setting for NOPT17; added footnote 1. <i>Section: Minimum and maximum values</i>: T_A = -40 °C (not 40 °C). <i>Table: General operating conditions</i>: updated V_{CAP}. <i>Table: Total current consumption in Run, Wait and Slow mode</i> General conditions for VDD apply, TA = -40 to 150 °C: updated conditions for I_{DD}(RUN). <i>Table: I/O static characteristics</i>: added new condition and new max values for rise and fall time; updated the footnote.