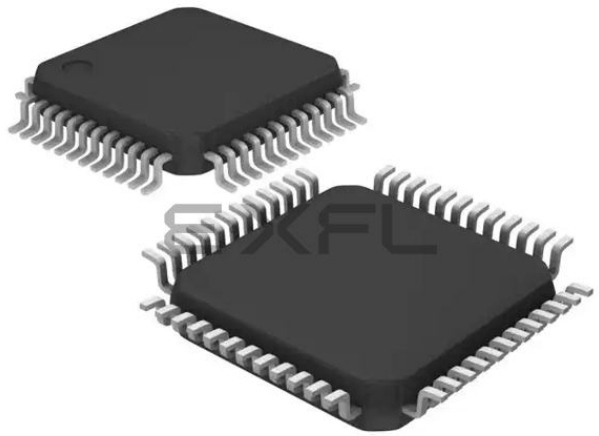

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6268tcy

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1 Introduction

This datasheet refers to the STM8AF6246, STM8AF6248, STM8AF6266 and STM8AF6268 products with 16 to 32 Kbyte of Flash program memory.

In the order code, the letter ‘F’ refers to product versions with data EEPROM and ‘H’ refers to product versions without data EEPROM. The identifiers ‘F’ and ‘H’ do not coexist in a given order code.

The datasheet contains the description of family features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8A microcontroller memory, registers and peripherals, please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8 Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

2 Description

The STM8AF6246, STM8AF6248, STM8AF6266 and STM8AF6268 automotive 8-bit microcontrollers offer from 16 to 32 Kbyte of Flash program memory and integrated true data EEPROM. They are referred to as medium density STM8A devices in STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).

All devices of the STM8A product line provide the following benefits: reduced system cost, performance and robustness, short development cycles, and product longevity.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 k write/erase cycles and a high system integration level with internal clock oscillators, watchdog, and brown-out reset.

Device performance is ensured by a clock frequency of up to 16 MHz CPU and enhanced characteristics which include robust I/O, independent watchdogs (with a separate clock source), and a clock security system.

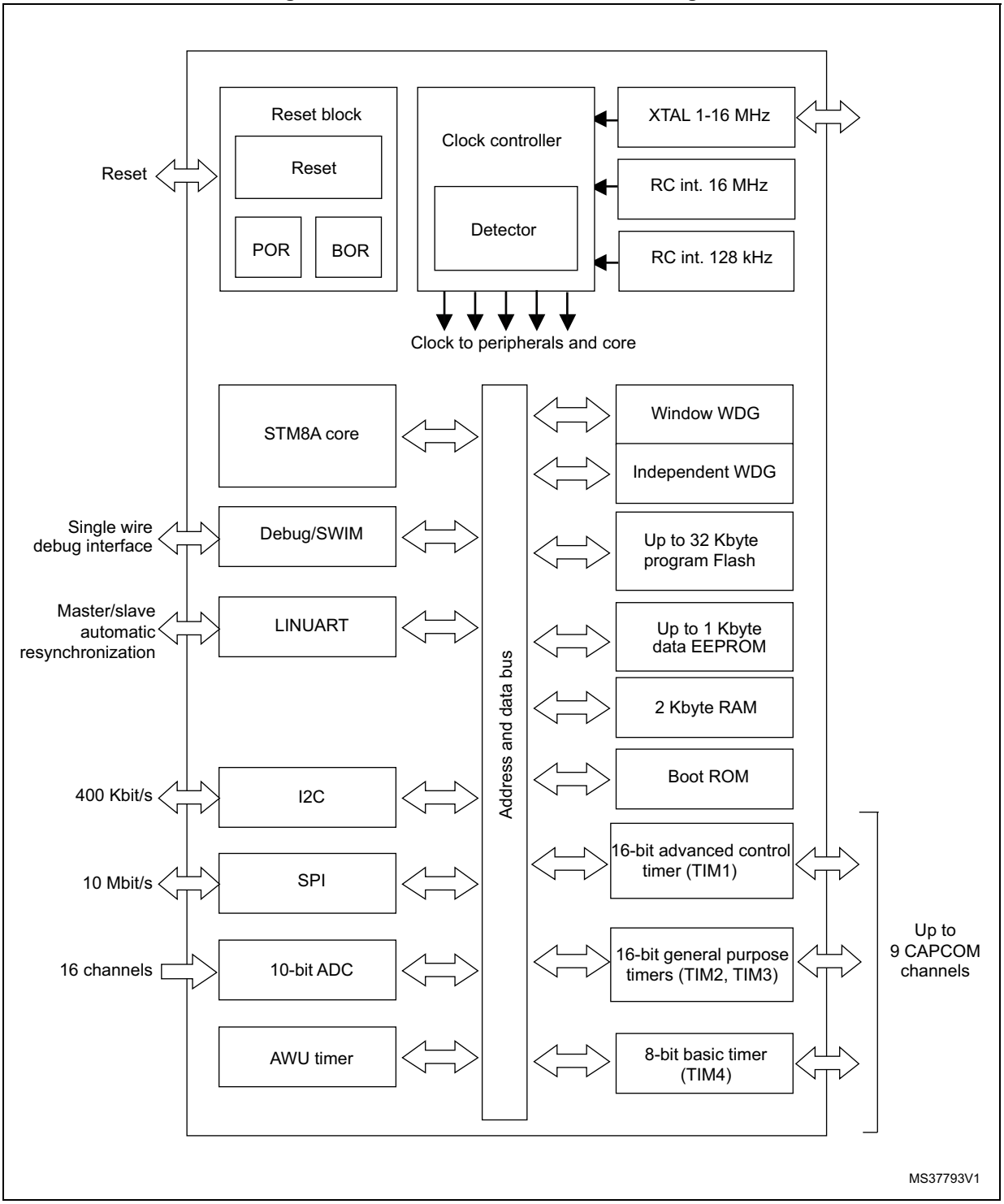
Short development cycles are guaranteed due to application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals. Full documentation is offered with a wide choice of development tools.

Product longevity is ensured in the STM8A family thanks to their advanced core which is made in a state-of-the art technology for automotive applications with 3.3 V to 5 V operating supply.

All STM8A and ST7 microcontrollers are supported by the same tools including STVD/STVP development environment, the STice emulator and a low-cost, third party in-circuit debugging tool.

4 Block diagram

Figure 1. STM8AF6246/48/66/68 block diagram



5 Product overview

This section describes the family features that are implemented in the products covered by this datasheet.

For more detailed information on each feature please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).

5.1 STM8A central processing unit (CPU)

The 8-bit STM8A core is a modern CISC core and has been designed for code efficiency and performance. It contains 21 internal registers (six directly addressable in each execution context), 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

5.1.1 Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus with single cycle fetching for most instructions
- X and Y 16-bit index registers, enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter with 16-Mbyte linear memory space
- 16-bit stack pointer with access to a 64 Kbyte stack
- 8-bit condition code register with seven condition flags for the result of the last instruction.

5.1.2 Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for efficient implementation of local variables and parameter passing

5.1.3 Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

5.4.2 Write protection (WP)

Write protection in application mode is intended to avoid unintentional overwriting of the memory. The write protection can be removed temporarily by executing a specific sequence in the user software.

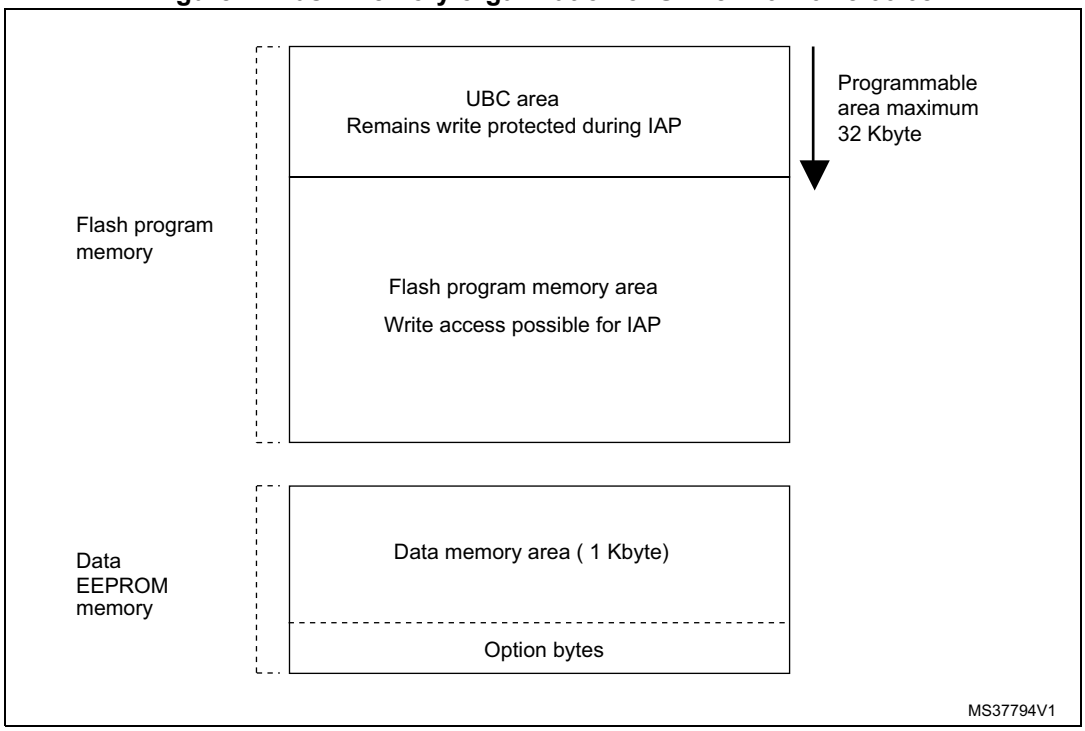
5.4.3 Protection of user boot code (UBC)

If the user chooses to update the Flash program memory using a specific boot code to perform in application programming (IAP), this boot code needs to be protected against unwanted modification.

In the STM8A a memory area of up to 32 Kbyte can be protected from overwriting at user option level. Other than the standard write protection, the UBC protection can exclusively be modified via the debug interface, the user software cannot modify the UBC protection status.

The UBC memory area contains the reset and interrupt vectors and its size can be adjusted in increments of 512 bytes by programming the UBC and NUBC option bytes (see *Section 9: Option bytes on page 44*).

Figure 2. Flash memory organization of STM8AF6246/48/66/68



Independent watchdog timer

The independent watchdog peripheral can be used to resolve malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure. If the hardware watchdog feature is enabled through the device option bits, the watchdog is automatically enabled at power-on, and generates a reset unless the key register is written by software before the counter reaches the end of count.

5.7.2 Auto-wakeup counter

This counter is used to cyclically wakeup the device in Active-halt mode. It can be clocked by the internal 128 kHz internal low-frequency RC oscillator or external clock.

LSI clock can be internally connected to TIM3 input capture channel 1 for calibration.

5.7.3 Beeper

This function generates a rectangular signal in the range of 1, 2 or 4 kHz which can be output on a pin. This is useful when audible sounds without interference need to be generated for use in the application.

5.7.4 Advanced control and general purpose timers

STM8A devices described in this datasheet, contain up to three 16-bit advanced control and general purpose timers providing nine CAPCOM channels in total. A CAPCOM channel can be used either as input compare, output compare or PWM channel. These timers are named TIM1, TIM2 and TIM3.

Table 3. Advanced control and general purpose timers

Timer	Counter width	Counter type	Prescaler factor	Channels	Inverted outputs	Repetition counter	trigger unit	External trigger	Break input
TIM1	16-bit	Up/down	1 to 65536	4	3	Yes	Yes	Yes	Yes
TIM2	16-bit	Up	2^n n = 0 to 15	3	None	No	No	No	No
TIM3	16-bit	Up	2^n n = 0 to 15	2	None	No	No	No	No

TIM1: Advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and bridge driver.

- 16-bit up, down and up/down AR (auto-reload) counter with 16-bit fractional prescaler.
- Four independent CAPCOM channels configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Trigger module which allows the interaction of TIM1 with other on-chip peripherals. In the present implementation it is possible to trigger the ADC upon a timer event.
- External trigger to change the timer behavior depending on external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Interrupt sources: 4 x input capture/output compare, 1 x overflow/update, 1 x break

TIM2 and TIM3: 16-bit general purpose timers

- 16-bit auto-reload up-counter
- 15-bit prescaler adjustable to fixed power of two ratios 1…32768
- Timers with three or two individually configurable CAPCOM channels
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

5.7.5 Basic timer

The typical usage of this timer (TIM4) is the generation of a clock tick.

Table 4. TIM4

Timer	Counter width	Counter type	Prescaler factor	Channels	Inverted outputs	Repetition counter	trigger unit	External trigger	Break input
TIM4	8-bit	Up	2^n n = 0 to 7	0	None	No	No	No	No

- 8-bit auto-reload, adjustable prescaler ratio to any power of two from 1 to 128
- Clock source: master clock
- Interrupt source: 1 x overflow/update

UART mode

- Full duplex, asynchronous communications - NRZ standard format (mark/space)
- High-precision baud rate generator
  - A common programmable transmit and receive baud rates up to $f_{MASTER}/16$
- Programmable data word length (8 or 9 bits) – 1 or 2 stop bits – parity control
- Separate enable bits for transmitter and receiver
- Error detection flags
- Reduced power consumption mode
- Multi-processor communication - enter mute mode if address match does not occur
- Wakeup from mute mode (by idle line detection or address mark detection)
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line

5.10 Input/output specifications

The product features four different I/O types:

- Standard I/O 2 MHz
- Fast I/O up to 10 MHz
- High sink 8 mA, 2 MHz
- True open drain (I^2C interface)

To decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os.

The analog inputs are equipped with a low leakage analog switch. Additionally, the schmitt-trigger input stage on the analog I/Os can be disabled in order to reduce the device standby consumption.

STM8A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA. Thanks to this feature, external protection diodes against current injection are no longer required.

Table 8. STM8AF6246/48/66/68 (32 Kbyte) microcontroller pin description(1)(2) (continued)

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	VFQFPN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
47	31	PD6/ LINUART_RX	I/O	**X**	X	X	-	O1	X	X	**Port D6**	LINUART data receive	-
48	32	PD7/TLI(8)	I/O	**X**	X	X	-	O1	X	X	**Port D7**	Top level interrupt	-

1. Refer to *Table 7* for the definition of the abbreviations.
2. Reset state is shown in bold.
3. In Halt/Active-halt mode this pad behaves in the following way:
   - the input/output path is disabled
   - if the HSE clock is used for wakeup, the internal weak pull up is disabled
   - if the HSE clock is off, internal weak pull up setting from corresponding OR bit is used
   By managing the OR bit correctly, it must be ensured that the pad is not left floating during Halt/Active-halt.
4. On this pin, a pull-up resistor as specified in *Table 35*. I/O static characteristics is enabled during the reset phase of the product.
5. AIN12 is not selectable in ADC scan mode or with analog watchdog.
6. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, week pull-up, and protection diode to V_{DD} are not implemented)
7. The PD1 pin is in input pull-up during the reset phase and after reset release.
8. If this pin is configured as interrupt pin, it will trigger the TLI.

6.2 Alternate function remapping

As shown in the rightmost column of *Table 8*, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. Refer to *Section 9: Option bytes on page 44*. When the remapping option is active, the default alternate function is no longer available.

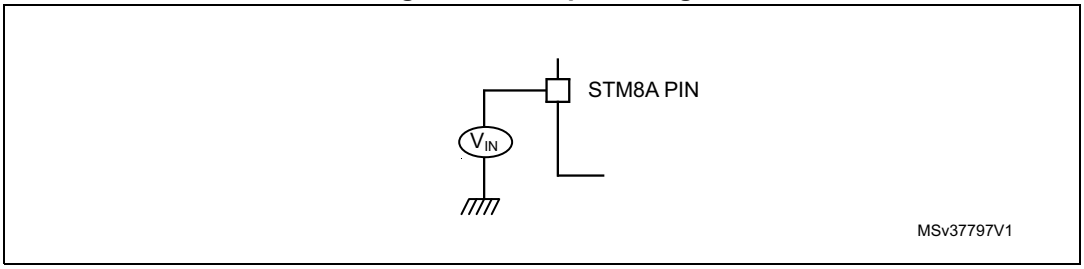
To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of STM8S series and STM8AF series 8-bit microcontrollers reference manual, RM0016).

10.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 7. Pin input voltage



10.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 17. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (PE1, PE2)(2)	V_{SS} - 0.3	6.5	V
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{DD} \rvert$	Variations between different power pins	-	50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins	-	50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 76*		

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

10.3.8 TIM 1, 2, 3, and 4 timer specifications

Subject to general operating conditions for V_{DD}, f_{MASTER}, and T_A unless otherwise specified.

Table 37. TIM 1, 2, 3, and 4 electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{EXT}	Timer external clock frequency(1)	-	-	-	16	MHz

1. Not tested in production. On 64 Kbyte devices, the frequency is limited to 16 MHz.

10.3.9 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 38* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 38. SPI characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode		0	10	MHz
		Slave mode	V_{DD} < 4.5 V	0	6(1)	
			V_{DD} = 4.5 V to 5.5 V	0	8(1)	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		-	25(2)	ns
$t_{su(NSS)}$(3)	NSS setup time	Slave mode		4 * t_{MASTER}	-	
$t_{h(NSS)}$(3)	NSS hold time	Slave mode		70	-	
$t_{w(SCKH)}$(3) $t_{w(SCKL)}$(3)	SCK high and low time	Master mode		$t_{SCK}/2$ - 15	$t_{SCK}/2$ + 15	
$t_{su(MI)}$(3) $t_{su(SI)}$(3)	Data input setup time	Master mode		5	-	
		Slave mode		5	-	
$t_{h(MI)}$(3) $t_{h(SI)}$(3)	Data input hold time	Master mode		7	-	
		Slave mode		10	-	
$t_{a(SO)}$(3)(4)	Data output access time	Slave mode		-	3* t_{MASTER}	
$t_{dis(SO)}$(3)(5)	Data output disable time	Slave mode		25		
$t_{v(SO)}$(3)	Data output valid time	Slave mode (after enable edge)	V_{DD} < 4.5 V	-	75	
			V_{DD} = 4.5 V to 5.5 V	-	53	
$t_{v(MO)}$(3)	Data output valid time	Master mode (after enable edge)		-	30	
$t_{h(SO)}$(3)	Data output hold time	Slave mode (after enable edge)		31	-	
$t_{h(MO)}$(3)		Master mode (after enable edge)		12	-	

1. $f_{SCK} < f_{MASTER}/2$.
2. The pad has to be configured accordingly (fast mode).

10.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

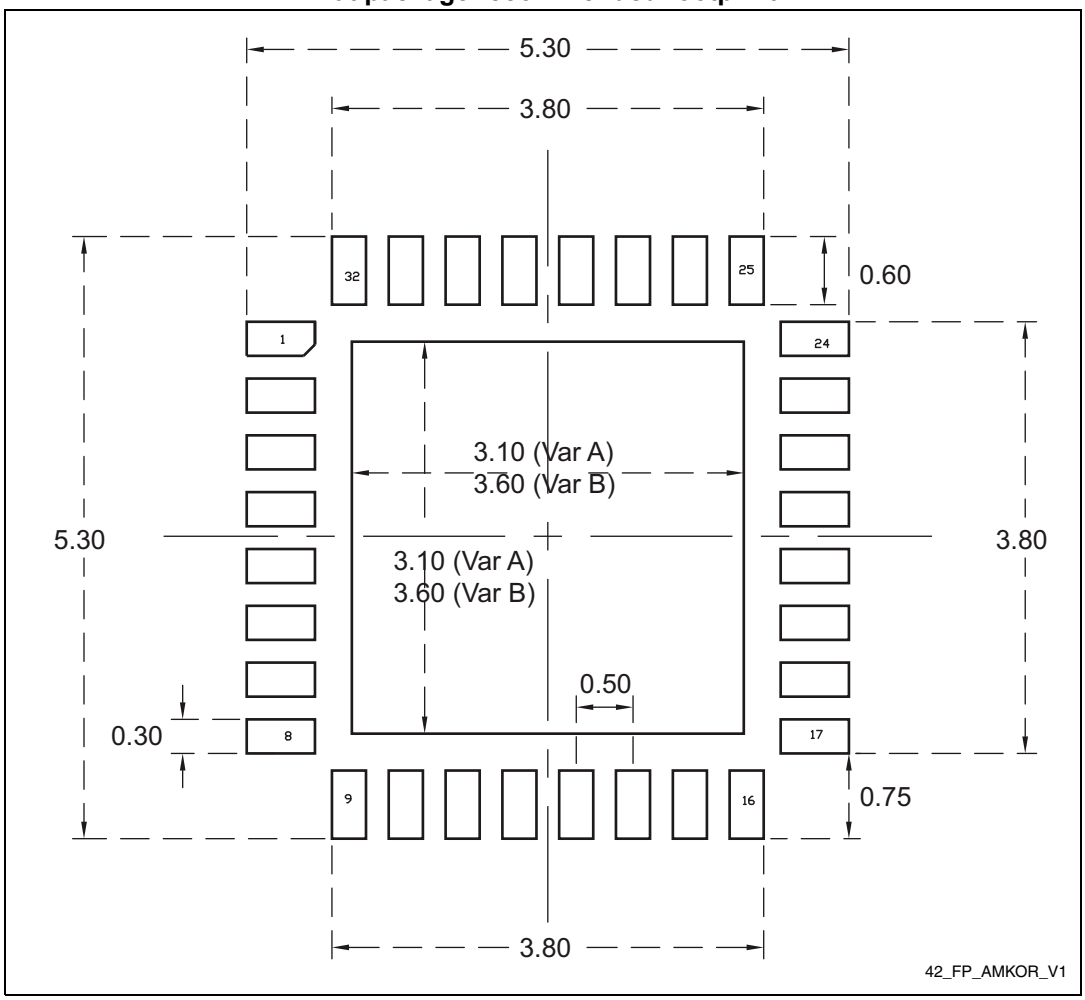
Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 42. EMS data

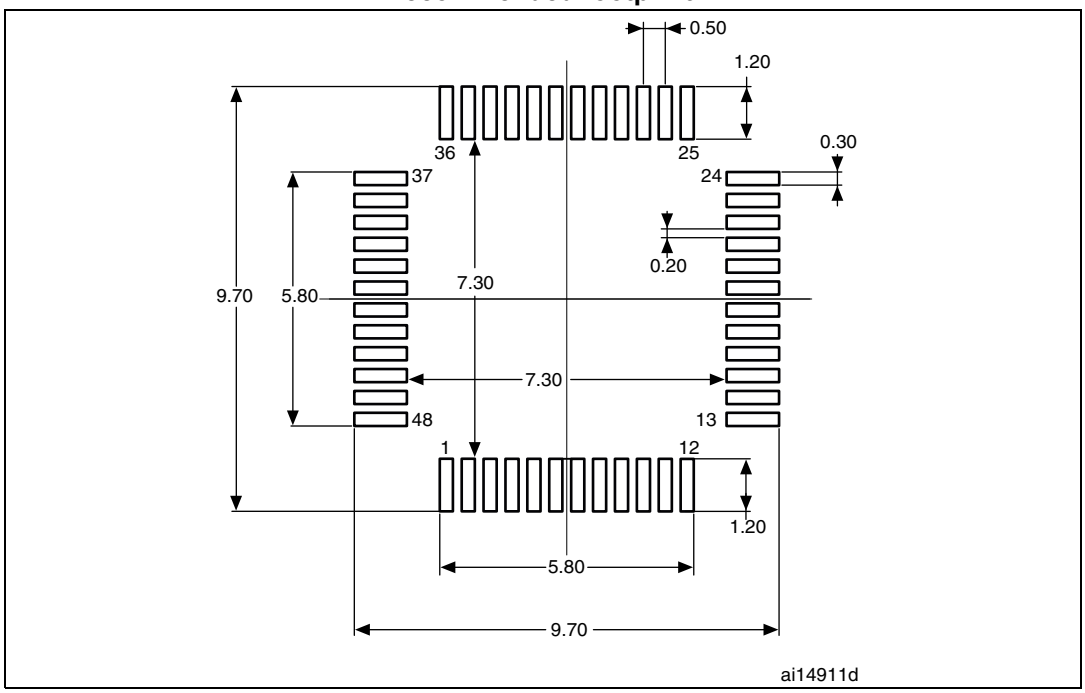
Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-2	3/B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD}= 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-4	4/A

Figure 43. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Figure 46. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint

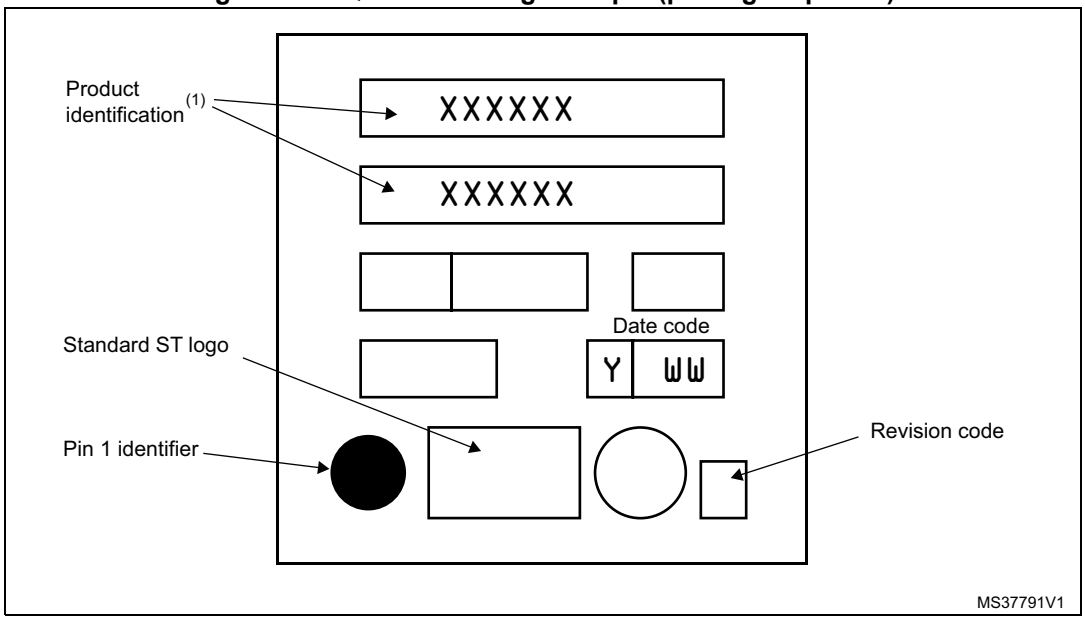


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 47. LQFP48 marking example (package top view)



13.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8A Flash microcontroller on the user application board via the SWIM protocol. Additional tools are used to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the user STM8A.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

14 Revision history

Table 50. Document revision history

Date	Revision	Changes
22-Aug-2008	1	Initial release
10-Aug-2009	2	Document revised as the following: Updated *Features*; Updated *Table: Device summary;* Updated *Section: Product line-up;* Changed *Section: Product overview*; Updated *Section: Pinouts and pin description;* Changed *Section: Register map;* Updated *Section: Interrupt table;* Updated *Section: Option bytes;* Updated *Section: Electrical characteristics;* Updated *Section: Package information;* Updated *Section: Ordering information;* Added *Section: STM8 development tools.*
22-Oct-2009	3	Adapted *Table: STM8AF61xx/62xx (32 Kbyte) microcontroller pin description.* Added *Section: LIN header error when automatic resynchronization is enabled.*
08-Jul-2010	4	Updated title on cover page. Added VFQFPN32 5x 5 mm package. Added STM8AF62xx devices, and modified cover page header to clarify the part numbers covered by the datasheets. Updated *Note 1* below *Table: Device summary.* Updated D temperature range to -40 to 150°C. Content of *Section: Product overview* reorganized. Renamed *Section: Memory and register map*, and content merged with Register map section. Renamed BL_EN and NBL_EN, BL and NBL, respectively, in *Table: Option bytes.* Added *Table: Operating lifetime.* Added CEXT and P_D (power dissipation) in *Table: General operating conditions*, and *Section: VCAP external capacitor.* Suffix D maximum junction temperature (T_J) updated in *Table: General operating conditions.* Update t_{VDD} in *Table: Operating conditions at power-up/power-down*. Moved *Table: Typical peripheral current consumption VDD = 5.0 V* to *Section: Current consumption for on-chip peripherals* and removed $I_{DD(CAN)}$. Updated *Section: Ordering information* for the devices supported by the datasheet. Updated *Section: STM8 development tools.*

Table 50. Document revision history (continued)

Date	Revision	Changes
18-Jul-2012	6 (continued)	*Section: Reset pin characteristics:* updated text below *Figure: Typical NRST pull-up current Ipu vs VDD*. *Figure: Recommended reset pin protection*: updated unit of capacitor. *Table: SPI characteristics:* updated SCK high and low time conditions and values. *Figure: SPI timing diagram - master mode*: replaced 'SCK input' signals with 'SCK output' signals. Updated *Table: VFQFPN 32-lead very thin fine pitch quad flat no-lead package mechanical data, Table: LQFP 48-pin low profile quad flat package mechanical data*, and *Table: LQFP 32-pin low profile quad flat package mechanical data.* Replaced *Figure: LQFP 48-pin low profile quad flat package (7 x 7)* and *Figure: LQFP 32-pin low profile quad flat package (7 x 7)*. Added *Figure: LQFP 48-pin recommended footprint* and *Figure: LQFP 32-pin recommended footprint.* *Figure: Ordering information scheme(1):* added footnote *1*, added "xxx" and footnote *2*, updated example and device family; added FASTROM. *Section: C and assembly toolchains:* added www.iar.com
04-Apr-2014	7	Updated: – *Table: Device summary,* – *Table: STM8AF62xx product line-up,* – *Table: STM8AF/H61xx product line-up.* – SPI description in *Features.* – The typical and maximum values for t_{TEMP} reset release delay in *Table: Operating conditions at power-up/power-down.* – The symbol for NRST Input not filtered pulse duration in *Table: NRST pin characteristics* – The address and comment of Reset interrupt in *Table: STM8A interrupt table.* Added the three footnotes to *Figure VFQFPN 32-lead very thin fine pitch quad flat no-lead package (5 x 5)*.
24-Jun-2014	8	Updated *Table: HSI oscillator characteristics.* Added HSI accuracy and removed temperature range B in *Figure: Ordering information scheme(1).*
12-Nov-2014	9	Updates in *Table: HSI oscillator characteristics* (HSI oscillator accuracy (factory calibrated) values) and *Figure: Ordering information scheme(1)* (changed the value for I).