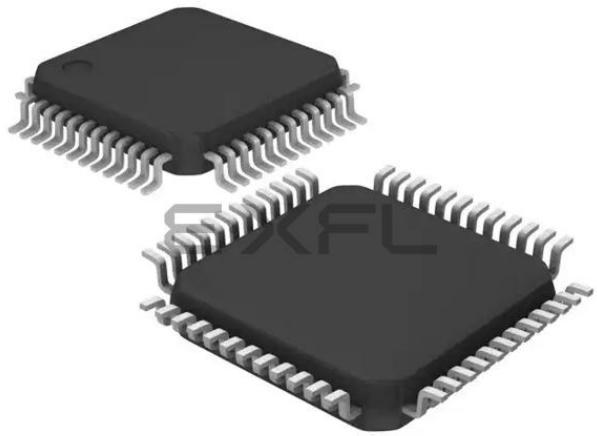

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8af6268tdy

5.4.2 Write protection (WP)

Write protection in application mode is intended to avoid unintentional overwriting of the memory. The write protection can be removed temporarily by executing a specific sequence in the user software.

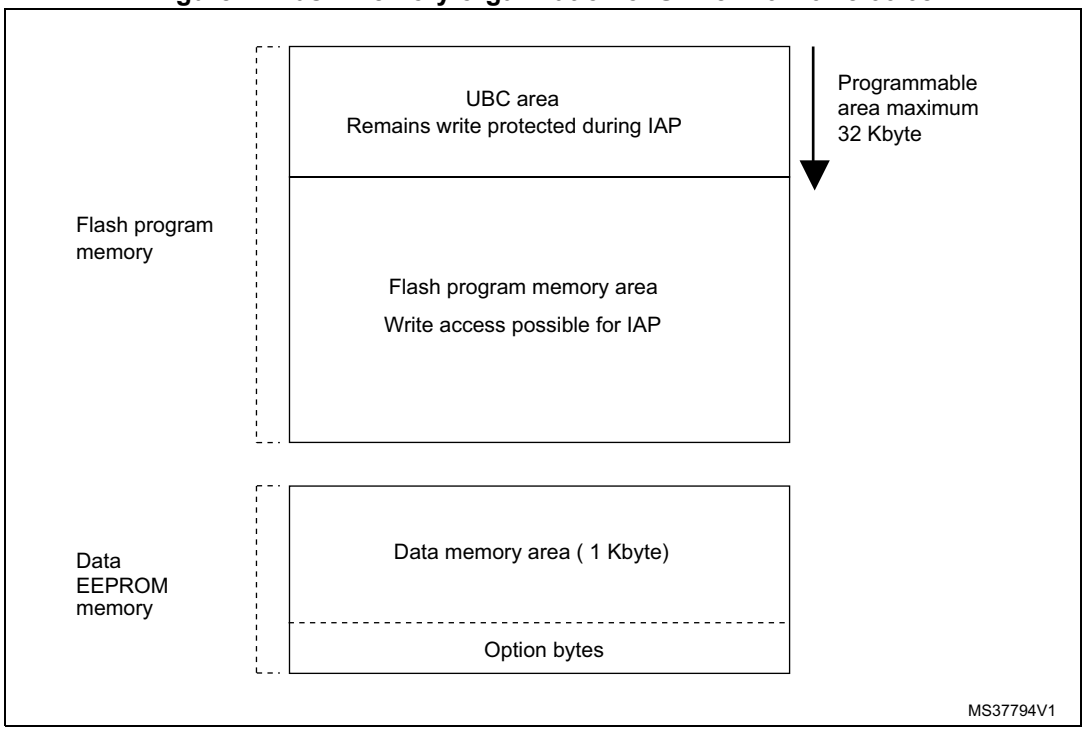
5.4.3 Protection of user boot code (UBC)

If the user chooses to update the Flash program memory using a specific boot code to perform in application programming (IAP), this boot code needs to be protected against unwanted modification.

In the STM8A a memory area of up to 32 Kbyte can be protected from overwriting at user option level. Other than the standard write protection, the UBC protection can exclusively be modified via the debug interface, the user software cannot modify the UBC protection status.

The UBC memory area contains the reset and interrupt vectors and its size can be adjusted in increments of 512 bytes by programming the UBC and NUBC option bytes (see *Section 9: Option bytes on page 44*).

Figure 2. Flash memory organization of STM8AF6246/48/66/68



5.4.4 Read-out protection (ROP)

The STM8A provides a read-out protection of the code and data memory which can be activated by an option byte setting (see the ROP option byte in section 10).

The read-out protection prevents reading and writing Flash program memory, data memory and option bytes via the debug module and SWIM interface. This protection is active in all device operation modes. Any attempt to remove the protection by overwriting the ROP option byte triggers a global erase of the program and data memory.

The ROP circuit may provide a temporary access for debugging or failure analysis. The temporary read access is protected by a user defined, 8-byte keyword stored in the option bytes area. This keyword must be entered via the SWIM interface to temporarily unlock the device.

If desired, the temporary unlock mechanism can be permanently disabled by the user through OPT6/NOPT6 option bytes.

5.5 Clock controller

The clock controller distributes the system clock coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

5.5.1 Features

- **Clock sources**
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
  - 1-16 MHz high-speed external crystal (HSE)
  - Up to 16 MHz high-speed user-external clock (HSE user-ext)
- **Reset**: After reset the microcontroller restarts by default with an internal 2-MHz clock (16 MHz/8). The clock source and speed can be changed by the application program as soon as the code execution starts.
- **Safe clock switching**: Clock sources can be changed safely on the fly in Run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management**: To reduce power consumption, the clock controller can stop the clock to the core or individual peripherals.
- **Wakeup**: In case the device wakes up from low-power modes, the internal RC oscillator (16 MHz/8) is used for quick startup. After a stabilization time, the device switches to the clock source that was selected before Halt mode was entered.
- **Clock security system (CSS)**: The CSS permits monitoring of external clock sources and automatic switching to the internal RC (16 MHz/8) in case of a clock failure.
- **Configurable main clock output (CCO)**: This feature permits to output a clock signal for use by the application.

5.8 Analog-to-digital converter (ADC)

The STM8A products described in this datasheet contain a 10-bit successive approximation ADC with up to 16 multiplexed input channels, depending on the package.

The ADC name differs between the datasheet and STM8S series and STM8AF series 8-bit microcontrollers reference manual (see *Table 5*).

Table 5. ADC naming

Peripheral name in datasheet	Peripheral name in reference manual (RM0016)
ADC	ADC1

ADC features

- 10-bit resolution
- Single and continuous conversion modes
- Programmable prescaler: f_{MASTER} divided by 2 to 18
- Conversion trigger on timer events and external events
- Interrupt generation at end of conversion
- Selectable alignment of 10-bit data in 2 x 8 bit result register
- Shadow registers for data consistency
- ADC input range: $V_{SSA} \leq V_{IN} \leq V_{DDA}$
- Analog watchdog
- Schmitt-trigger on analog inputs can be disabled to reduce power consumption
- Scan mode (single and continuous)
- Dedicated result register for each conversion channel
- Buffer mode for continuous conversion

Note: An additional AIN12 analog input is not selectable in ADC scan mode or with analog watchdog. Values converted from AIN12 are stored only into the ADC_DRH/ADC_DRL registers.

5.9 Communication interfaces

The following sections give a brief overview of the communication peripheral. Some peripheral names differ between the datasheet and STM8S series and STM8AF series 8-bit microcontrollers reference manual (see *Table 6*).

Table 6. Communication peripheral naming correspondence

Peripheral name in datasheet	Peripheral name in reference manual (RM0016)
LINUART	UART2

- Interrupt:
  - Successful address/data communication
  - Error condition
  - Wakeup from Halt
- Wakeup from Halt on address detection in slave mode

5.9.3 Universal asynchronous receiver/transmitter with LIN support (LINUART)

The devices covered by this datasheet contain one LINUART interface. The interface is available on all the supported packages. The LINUART is an asynchronous serial communication interface which supports extensive LIN functions tailored for LIN slave applications. In LIN mode it is compliant to the LIN standards rev 1.2 to rev 2.2.

Detailed feature list:

LIN mode

Master mode:

- LIN break and delimiter generation
- LIN break and delimiter detection with separate flag and interrupt source for read back checking.

Slave mode:

- Autonomous header handling – one single interrupt per valid header
- Mute mode to filter responses
- Identifier parity error checking
- LIN automatic resynchronization, allowing operation with internal RC oscillator (HSI) clock source
- Break detection at any time, even during a byte reception
- Header errors detection:
  - Delimiter too short
  - Synch field error
  - Deviation error (if automatic resynchronization is enabled)
  - Framing error in synch field or identifier field
  - Header time-out

7 Memory and register map

7.1 Memory map

Figure 5. Register and memory map of STM8A products

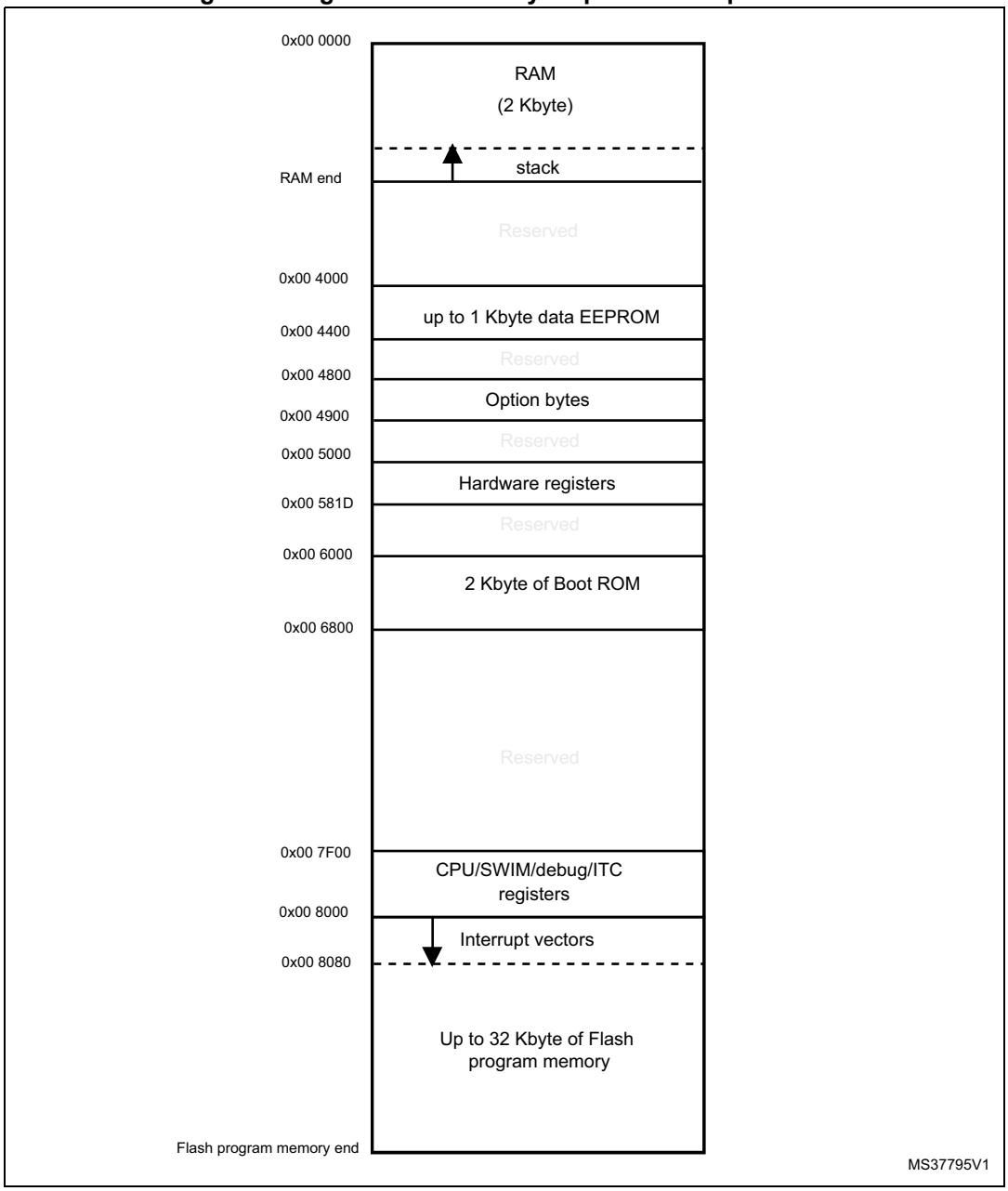


Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5314	TIM2	TIM2_CCR3L	TIM2 capture/compare register 3 low	0x00
0x00 5315 to 0x00 531F	Reserved area (11 bytes)			
0x00 5320	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5321		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5322		TIM3_SR1	TIM3 status register 1	0x00
0x00 5323		TIM3_SR2	TIM3 status register 2	0x00
0x00 5324		TIM3_EGR	TIM3 event generation register	0x00
0x00 5325		TIM3_CCMR1	TIM3 capture/compare mode register 1	0x00
0x00 5326		TIM3_CCMR2	TIM3 capture/compare mode register 2	0x00
0x00 5327		TIM3_CCER1	TIM3 capture/compare enable register 1	0x00
0x00 5328		TIM3_CNTRH	TIM3 counter high	0x00
0x00 5329		TIM3_CNTRL	TIM3 counter low	0x00
0x00 532A		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 532B		TIM3_ARRH	TIM3 auto-reload register high	0xFF
0x00 532C		TIM3_ARRL	TIM3 auto-reload register low	0xFF
0x00 532D		TIM3_CCR1H	TIM3 capture/compare register 1 high	0x00
0x00 532E		TIM3_CCR1L	TIM3 capture/compare register 1 low	0x00
0x00 532F		TIM3_CCR2H	TIM3 capture/compare register 2 high	0x00
0x00 5330		TIM3_CCR2L	TIM3 capture/compare register 2 low	0x00
0x00 5331 to 0x00 533F	Reserved area (15 bytes)			
0x00 5340	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 5341		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 5342		TIM4_SR	TIM4 status register	0x00
0x00 5343		TIM4_EGR	TIM4 event generation register	0x00
0x00 5344		TIM4_CNTR	TIM4 counter	0x00
0x00 5345		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 5346		TIM4_ARR	TIM4 auto-reload register	0xFF
0x00 5347 to 0x00 53DF	Reserved area (185 bytes)			

Table 11. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 540B	ADC	ADC_LTRL	ADC low threshold register low	0x00
0x00 540C		ADC _AWSRH	ADC watchdog status register high	0x00
0x00 540D		ADC_AWSRL	ADC watchdog status register low	0x00
0x00 540E		ADC _AWCRH	ADC watchdog control register high	0x00
0x00 540F		ADC _AWCRL	ADC watchdog control register low	0x00
0x00 5410 to 0x00 541F	Reserved area (16 bytes)			

1. Depends on the previous reset source.
2. Write only register.

Table 12. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x80
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x17(2)
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CC	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 bytes)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF
0x00 7F76 to 0x00 7F79	Reserved area (4 bytes)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00

8 Interrupt table

Table 14. STM8A interrupt table

Priority	Source block	Description	Interrupt vector address	Wakeup from Halt	Comments
-	Reset	Reset	0x00 8000	Yes	User RESET vector
-	TRAP	SW interrupt	0x00 8004	-	-
0	TLI	External top level interrupt	0x00 8008	-	-
1	AWU	Auto-wakeup from Halt	0x00 800C	Yes	-
2	Clock controller	Main clock controller	0x00 8010	-	-
3	MISC	Ext interrupt E0	0x00 8014	Yes	Port A interrupts
4	MISC	Ext interrupt E1	0x00 8018	Yes	Port B interrupts
5	MISC	Ext interrupt E2	0x00 801C	Yes	Port C interrupts
6	MISC	Ext interrupt E3	0x00 8020	Yes	Port D interrupts
7	MISC	Ext interrupt E4	0x00 8024	Yes	Port E interrupts
8	Reserved(1)	-	-	-	-
9	Reserved(1)	-	-	-	-
10	SPI	End of transfer	0x00 8030	Yes	-
11	Timer 1	Update/overflow/ trigger/break	0x00 8034	-	-
12	Timer 1	Capture/compare	0x00 8038	-	-
13	Timer 2	Update/overflow	0x00 803C	-	-
14	Timer 2	Capture/compare	0x00 8040	-	-
15	Timer 3	Update/overflow	0x00 8044	-	-
16	Timer 3	Capture/compare	0x00 8048	-	-
17	Reserved(1)	-	-	-	-
18	Reserved(1)	-	-	-	-
19	I^2C	I^2C interrupts	0x00 8054	Yes	-
20	LINUART	Tx complete/error	0x00 8058	-	-
21	LINUART	Receive data full reg.	0x00 805C	-	-
22	ADC	End of conversion	0x00 8060	-	-
23	Timer 4	Update/overflow	0x00 8064	-	-
24	EEPROM	End of Programming/ Write in not allowed area	0x00 8068	-	-

1. All reserved and unused interrupts must be initialized with ‘IRET’ for robust programming.

10 Electrical characteristics

10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = -40 °C, T_A = 25 °C, and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

10.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

10.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

Figure 6. Pin loading conditions

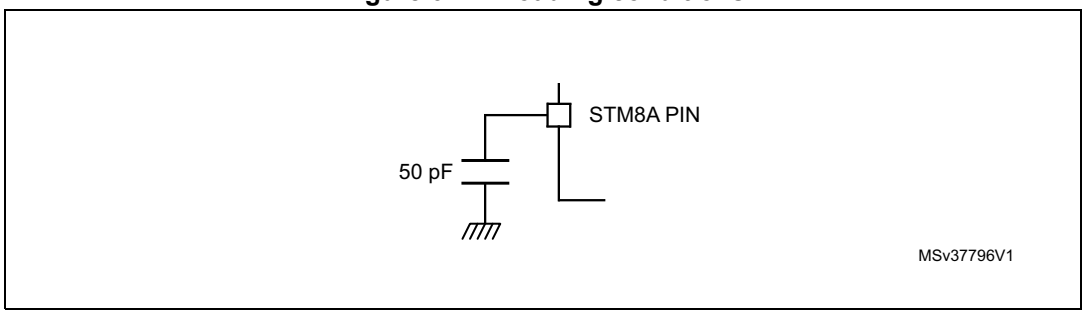
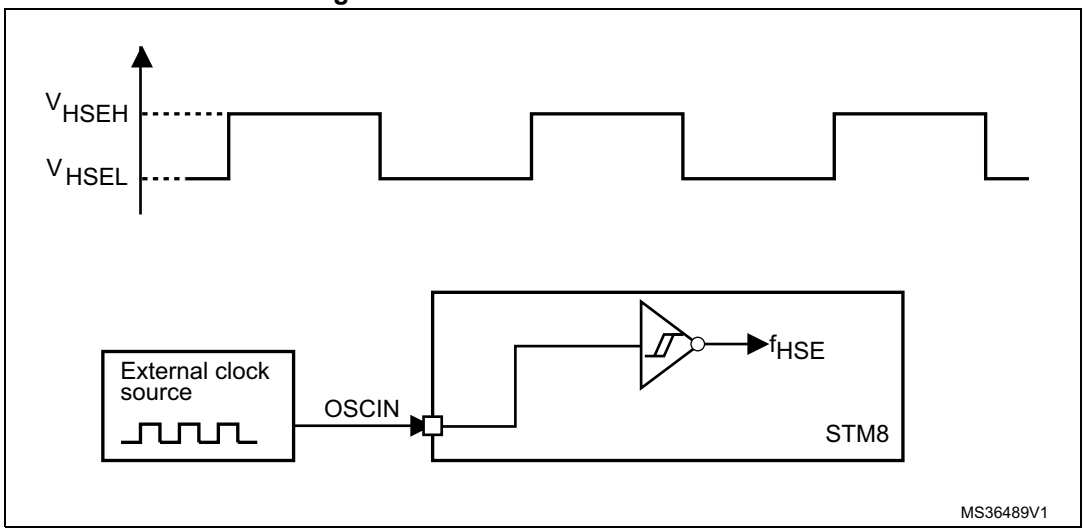


Figure 16. HSE external clock source



HSE crystal/ceramic resonator oscillator

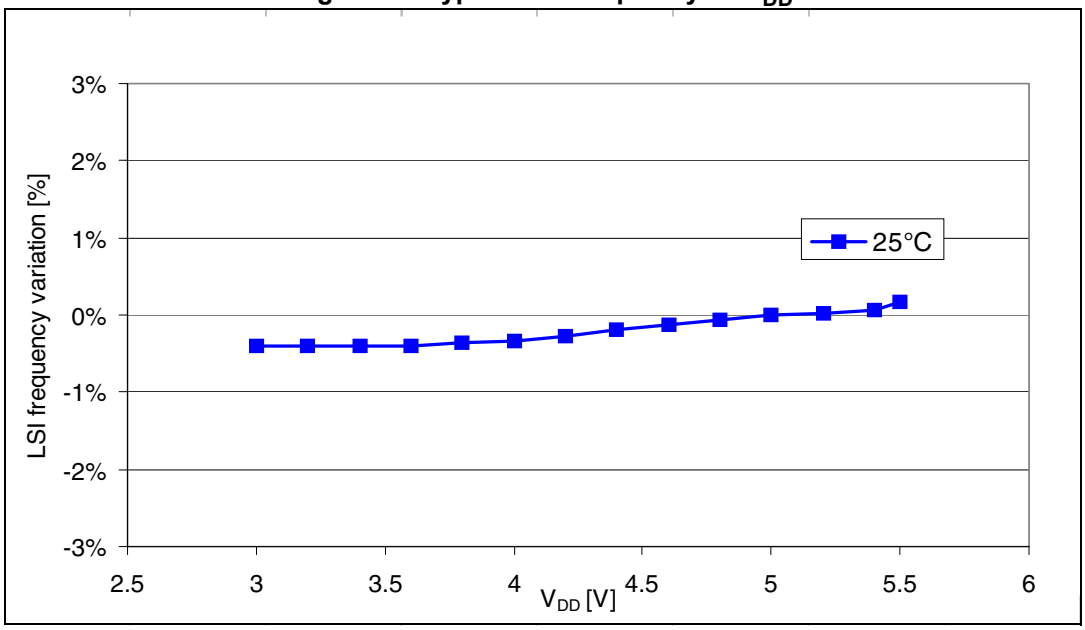
The HSE clock can be supplied using a crystal/ceramic resonator oscillator of up to 16 MHz. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 29. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	220	-	kΩ
C_{L1}/C_{L2}(1)	Recommended load capacitance	-	-	-	20	pF
g_m	Oscillator transconductance	-	5	-	-	mA/V
$t_{SU(HSE)}$(2)	Startup time	V_{DD} is stabilized	-	2.8	-	ms

1. The oscillator needs two load capacitors, C_{L1} and C_{L2}, to act as load for the crystal. The total load capacitance (C_{load}) is $(C_{L1} * C_{L2})/(C_{L1} + C_{L2})$. If $C_{L1} = C_{L2}$, $C_{load} = C_{L1} / 2$. Some oscillators have built-in load capacitors, C_{L1} and C_{L2}.
2. This value is the startup time, measured from the moment it is enabled (by software) until a stabilized 16 MHz oscillation is reached. It can vary with the crystal type that is used.

Figure 19. Typical LSI frequency vs V_{DD}



10.3.5 Memory characteristics

Flash program memory/data EEPROM memory

General conditions: T_A = -40 to 150 °C.

Table 32. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	f_{CPU} is 0 to 16 MHz with 0 ws	3.0	-	5.5	V
V_{DD}	Operating voltage (code execution)	f_{CPU} is 0 to 16 MHz with 0 ws	2.6	-	5.5	
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/128 bytes)	-	-	6	6.6	ms
	Fast programming time for 1 block (128 bytes)	-	-	3	3.3	
t_{erase}	Erase time for 1 block (128 bytes)	-	-	3	3.3	

Table 33. Flash program memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Flash program memory endurance (erase/write cycles)(1)	T_A = 25 °C	1000	-	cycles
t_{RET}	Data retention time	T_A = 25 °C	40	-	years
		T_A = 55 °C	20	-	

1. The physical granularity of the memory is four bytes, so cycling is performed on four bytes even when a write/erase operation addresses a single byte.

Table 34. Data memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	150	°C
N_{WE}	Data memory endurance(1) (erase/write cycles)	T_A = 25 °C	300 k	-	cycles
		T_A = -40°C to 125 °C	100 k(2)	-	
t_{RET}	Data retention time	T_A = 25 °C	40(2)(3)	-	years
		T_A = 55 °C	20(2)(3)	-	

1. The physical granularity of the memory is four bytes, so cycling is performed on four bytes even when a write/erase operation addresses a single byte.
2. More information on the relationship between data retention time and number of write/erase cycles is available in a separate technical document.
3. Retention time for 256B of data memory after up to 1000 cycles at 125 °C.

2. Guaranteed by design.
3. Data based on characterization results, not tested in production.

Figure 20. Typical V_{IL} and V_{IH} vs V_{DD} @ four temperatures

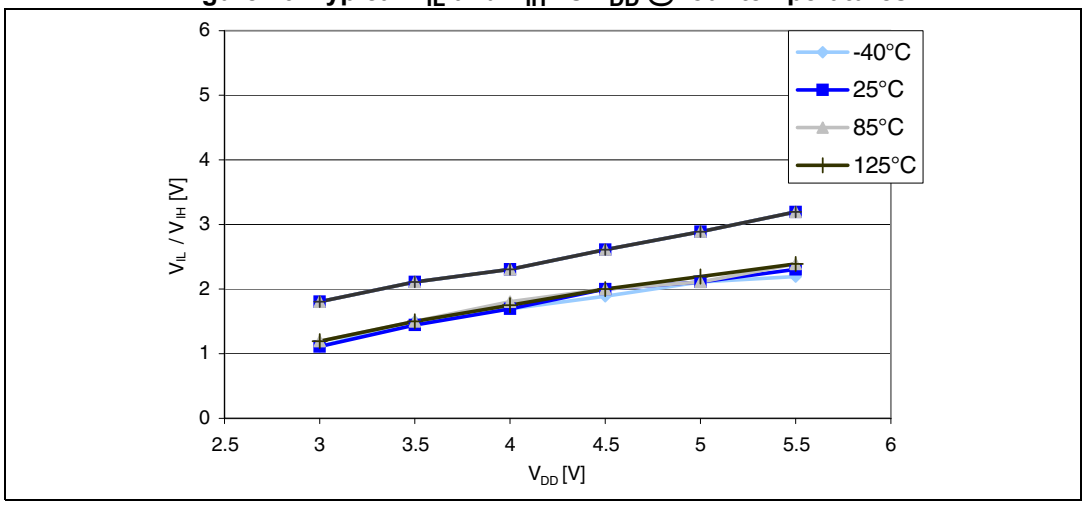
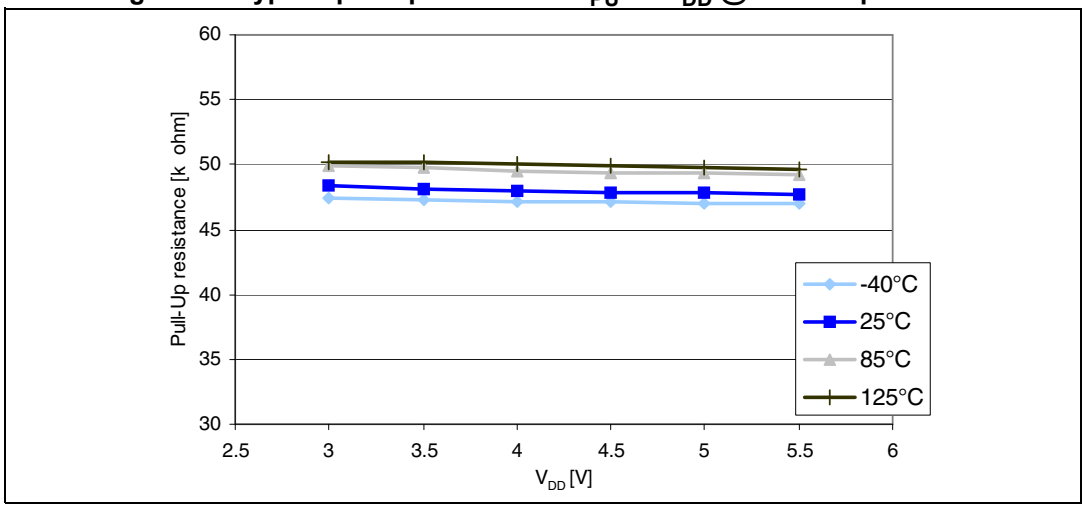


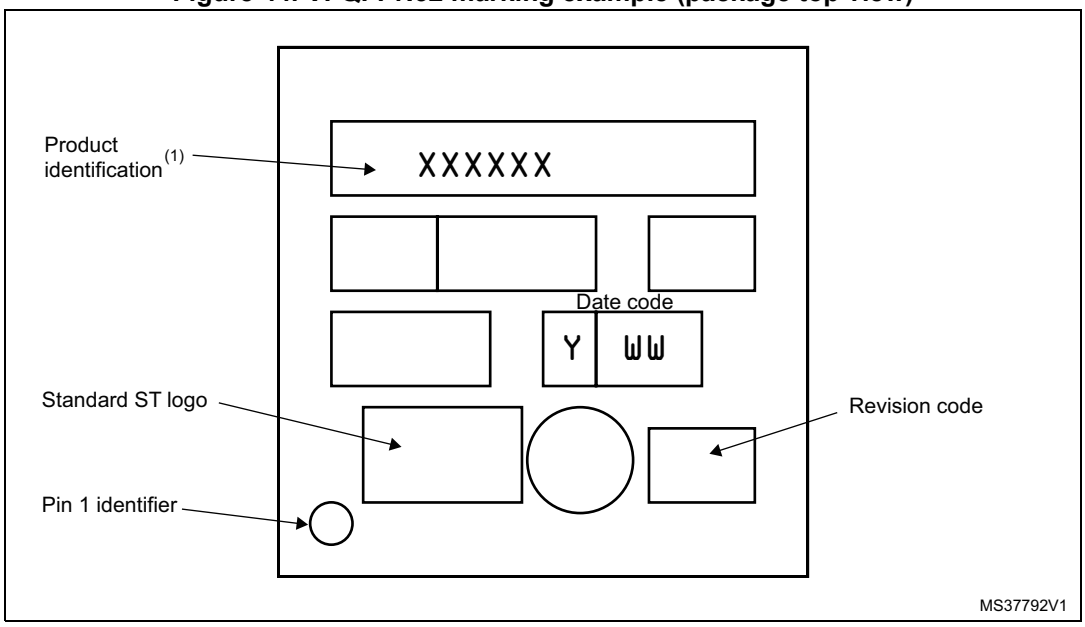
Figure 21. Typical pull-up resistance R_{PU} vs V_{DD} @ four temperatures



Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 44. VFQFPN32 marking example (package top view)



14 Revision history

Table 50. Document revision history

Date	Revision	Changes
22-Aug-2008	1	Initial release
10-Aug-2009	2	Document revised as the following: Updated *Features*; Updated *Table: Device summary;* Updated *Section: Product line-up;* Changed *Section: Product overview*; Updated *Section: Pinouts and pin description;* Changed *Section: Register map;* Updated *Section: Interrupt table;* Updated *Section: Option bytes;* Updated *Section: Electrical characteristics;* Updated *Section: Package information;* Updated *Section: Ordering information;* Added *Section: STM8 development tools.*
22-Oct-2009	3	Adapted *Table: STM8AF61xx/62xx (32 Kbyte) microcontroller pin description.* Added *Section: LIN header error when automatic resynchronization is enabled.*
08-Jul-2010	4	Updated title on cover page. Added VFQFPN32 5x 5 mm package. Added STM8AF62xx devices, and modified cover page header to clarify the part numbers covered by the datasheets. Updated *Note 1* below *Table: Device summary.* Updated D temperature range to -40 to 150°C. Content of *Section: Product overview* reorganized. Renamed *Section: Memory and register map*, and content merged with Register map section. Renamed BL_EN and NBL_EN, BL and NBL, respectively, in *Table: Option bytes.* Added *Table: Operating lifetime.* Added CEXT and P_D (power dissipation) in *Table: General operating conditions*, and *Section: VCAP external capacitor.* Suffix D maximum junction temperature (T_J) updated in *Table: General operating conditions.* Update t_{VDD} in *Table: Operating conditions at power-up/power-down*. Moved *Table: Typical peripheral current consumption VDD = 5.0 V* to *Section: Current consumption for on-chip peripherals* and removed $I_{DD(CAN)}$. Updated *Section: Ordering information* for the devices supported by the datasheet. Updated *Section: STM8 development tools.*

Table 50. Document revision history (continued)

Date	Revision	Changes
31-Jan-2011	5	Modified references to reference manual, and Flash programming manual in the whole document. Added reference to AEC Q100 standard on cover page. Renamed timer types as follows: – Auto-reload timer to general purpose timer – Multipurpose timer to advanced control timer – System timer to basic timer Introduced concept of medium density Flash program memory. Updated timer names in *Figure: STM8A block diagram.* Added TMU brief description in *Section: Flash program and data EEPROM*, and updated TMU_MAXATT description in *Table: Option byte description*. Updated clock sources in clock controller features. Changed 16MHZTRIM0 to HSITRIM bit in *Section: User trimming.* Added *Table: Peripheral clock gating bits.* Updated *Section: Low-power operating modes.* Added calibration using TIM3 in *Section: Auto-wakeup counter.* Added *Table: ADC naming* and *Table: Communication peripheral naming correspondence.* Added *Note 1* related AIN12 pin in *Section: Analog-to-digital converter (ADC)* and *Table: STM8AF61xx/62xx (32 Kbyte) microcontroller pin description.* Updated SPI data rate to 10 Mbit/s or $f_{MASTER}/2$ in *Section: Serial peripheral interface (SPI).* Added reset state in *Table: Legend/abbreviation.* *Table: STM8AF61xx/62xx (32 Kbyte) microcontroller pin description:* added *Note 7* related to PD1/SWIM, modified *Note 6,* corrected wpu input for PE1 and PE2, and renamed TIMn_CCx and TIMn_NCCx to TIMn_CHx and TIMn_CHxN, respectively. ***Section: Register map:*** Replaced tables describing register maps and reset values for non-volatile memory, global configuration, reset status, clock controller, interrupt controller, timers, communication interfaces, and ADC, by *Table: General hardware register map*. Added *Note 1* for Px_IDR registers in *Table: I/O port hardware register map.* Updated register reset values for Px_IDR registers. Added SWIM and debug module register map.

Table 50. Document revision history (continued)

Date	Revision	Changes
31-Jan-2011	5 (continued)	Renamed Fast Active Halt mode to Active-halt mode with regulator on, and Slow Active Halt mode to Active-halt mode with regulator off. Updated *Table: Total current consumption in Halt and Active-halt modes. General conditions for VDD apply, TA = -40 to 55 °C*, in particular $I_{DD(FAH)}$ and $I_{DD(SAH)}$ renamed $I_{DD(AH)}$; $t_{WU(FAH)}$ and $t_{WU(SAH)}$ renamed $t_{WU(AH)}$, and temperature condition added. Removed $I_{DD(USART)}$ from *Table: Typical peripheral current consumption VDD = 5.0 V.* Updated general conditions in *Section: Memory characteristics.* Modified T_{WE} maximum value in *Table: Flash program memory* and *Table: Data memory.* Update $I_{lkg\ ana}$ maximum value for T_A ranging from -40 to 150 °C in *Table: I/O static characteristics*. Added $t_{IFP(NRST)}$ and renamed $V_{F(NRST)}$ t_{IFP} in *Table: NRST pin characteristics.* Added recommendations concerning NRST pin level above *Figure: Recommended reset pin protection,* and updated external capacitor value. Added Raisonance compiler in *Section: Software tools.* Moved know limitations to separate errata sheet.
18-Jul-2012	6	Updated wildcards of document part numbers. *Table: Device summary: u*pdated the footnotes to all STM8AF61xx part numbers. *Section: Introduction:* small text change in first paragraph. *Table: STM8AF62xx product line-up*: added “P” version for all order codes; updated RAM. *Table: STM8AF/H61xx product line-up*: added “P” version for all order codes. *Figure: STM8A block diagram*: updated POR, BOR and WDG; updated LINUART input; added legend. *Section: Flash program and data EEPROM:* removed non relevant bullet points and added a sentence about the factory programmer. *Table: Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers:* updated *ADC features:* updated ADC input range. *Table: Memory model for the devices covered in this datasheet:* updated 16 Kbyte and 8 Kbyte information. *Table: Option bytes*: updated factory default setting for NOPT17; added footnote *1*. *Section: Minimum and maximum values:* T_A = -40 °C (not 40 °C). *Table: General operating conditions:* updated V_{CAP}. *Table: Total current consumption in Run, Wait and Slow mode General conditions for VDD apply, TA = -40 to 150 °C*: updated conditions for $I_{DD(RUN)}$. *Table: I/O static characteristics*: added new condition and new max values for rise and fall time; updated the footnote.