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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	4MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	37
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.29x29.29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc11k0cfne4

MC68HC11K Family

Technical Data

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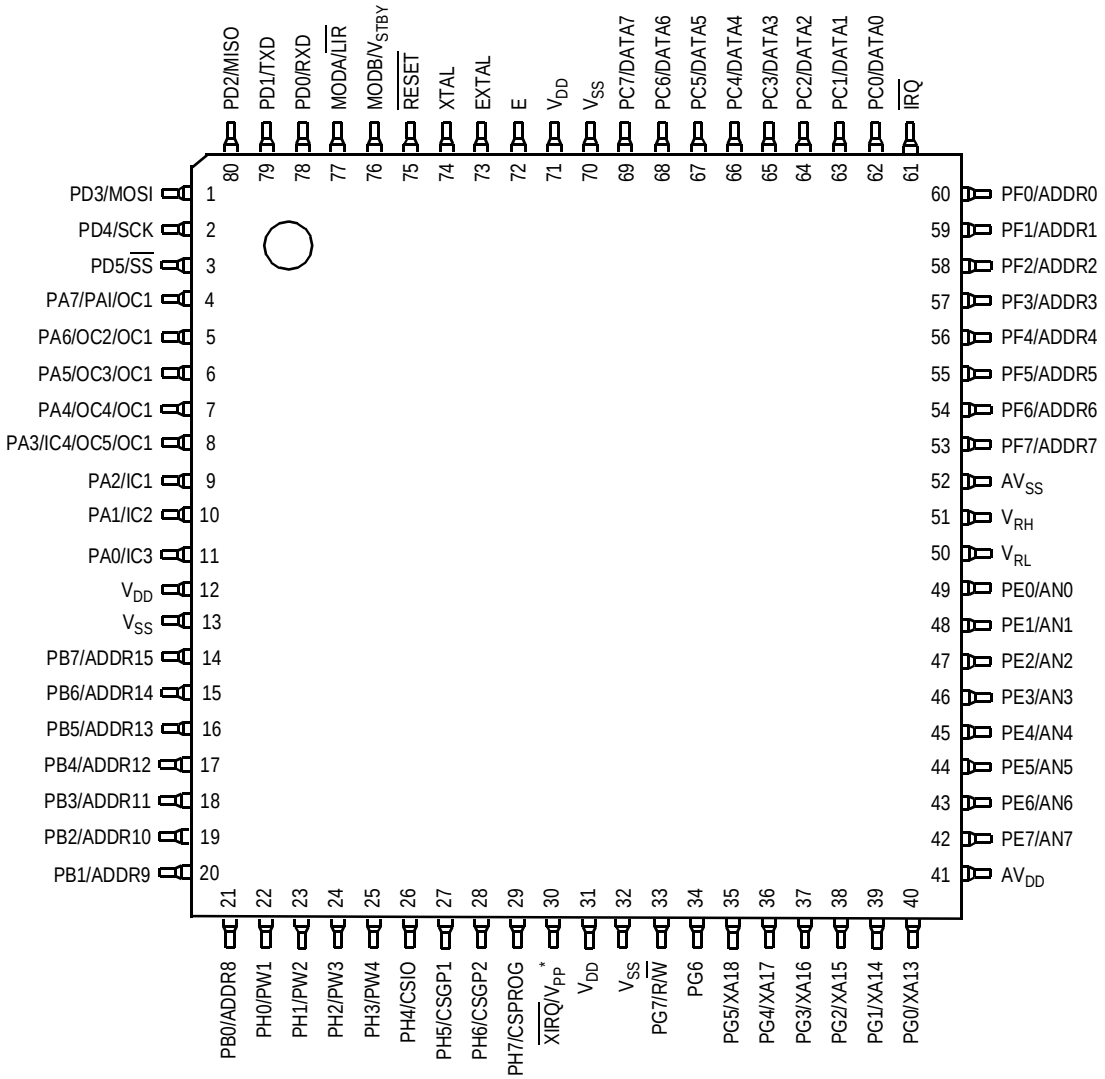


* V_{PP} applies only to EPROM devices.

Figure 2-2. Pin Assignments for M6811K 80-Pin QFP

4.8.2.2 EEPROM Bulk Erase

```
BULKE   LDAB    #$06
        STAB    $003B   Set EELAT and ERASE.
        STAA    $0,X    Store any data to any EEPROM address
        LDAB    #$07
        STAB    $002B   Set EEPGM bit as well
                        to enable EEPROM programming voltage
        JSR     DLY10   Delay 10 ms
        CLR     $003B   Turn off programming voltage and set
                        to READ mode
```

4.8.2.3 EEPROM Row Erase

```
ROWE    LDAB    #$07
        STAB    $003B   Set EELAT, ERASE and ROW.
        STAA    $0,X    Store any data to any EEPROM address
                        in row
        LDAB    #$07
        STAB    $002B   Set EEPGM bit as well
                        to enable EEPROM programming voltage
        JSR     DLY10   Delay 10 ms
        CLR     $003B   Turn off programming voltage and set
                        to READ mode
```

4.8.2.4 EEPROM Byte Erase

```
BYTEE   LDAB    #$16
        STAB    $003B   Set EELAT, ERASE and BYTE.
        STAA    $0,X    Store any data to targeted EEPROM
                        address
        LDAB    #$17
        STAB    $002B   Set EEPGM bit as well
                        to enable EEPROM programming voltage
        JSR     DLY10   Delay 10 ms
        CLR     $003B   Turn off programming voltage and set
                        to READ mode
```

  - All nine timer interrupts are disabled because their mask bits have been cleared.
  - The I4/O5 bit in the PACTL register is cleared to configure the I4/O5 function as OC5; however, the OM5:OL5 control bits in the TCTL1 register are clear so OC5 does not control the PA3 pin.

- Real-time interrupt (RTI)
  - The RTI enable bit in TMSK2 is cleared, masking automatic hardware interrupts.
  - The rate control bits are cleared after reset and can be initialized by software before the RTI system is enabled.
- Pulse accumulator
  - The pulse accumulator system is disabled at reset.
  - The PAI input pin defaults to a general-purpose input pin (PA7).
- Computer operating properly (COP) watchdog system
  - The COP watchdog system is enabled if the NOCOP control bit in the CONFIG register is clear and disabled if NOCOP is set.
  - The OPTION register's CR[1:0] bits are cleared, setting the COP rate for the shortest duration timeout.
- Serial communications interface (SCI)
  - At reset, the SCI baud rate control register (**7.9.1 SCI Baud Rate Control Register**) is initialized to $0004.
  - All transmit and receive interrupts are masked and both the transmitter and receiver are disabled so the port pins default to being general-purpose I/O lines.
  - The SCI frame format is initialized to an 8-bit character size.
  - The send break and receiver wake-up functions are disabled.
  - The TDRE and TC status bits in the SCI status register are both set, indicating that there is no transmit data in either the transmit data register or the transmit serial shift register.

extra hardware. The SPI system can send data at up to one half of the E-clock rate when configured as master and the full E-clock rate when configured as a slave.

8.3 SPI Functional Description

The SPI is a 4-wire, full-duplex communication system. Characters are eight bits, transmitted most significant bit (MSB) first. One master device exchanges data with one or more slave devices. Each device selects its mode by writing either a 1 (master) or 0 (slave) to the MSTR bit in the serial peripheral control register (SPCR). As a master device transmits data to a slave device via the MOSI (master out slave in) line, the slave transmits data to the master via the MISO (master in slave out) line. The master produces a common synchronization clock signal and drives it on its SCK (serial clock) pin, which is configured as an output. The slave SCK pin is configured as an input to receive the clock. An external logic low signal is applied to the slave select pin ($\overline{SS}$) of each slave device for which a particular message is intended. Devices not selected ($\overline{SS}$ high) ignore the transmission.

Received characters are double-buffered. Serial input bits are fed into a shift register; when the last bit is received, the completed character is parallel-loaded to a read data buffer. This allows the next message to be received while the current message is being read. As long as the buffer is read before the next received character is ready to be transferred to the buffer, no overrun condition occurs.

Transmitted characters are not double-buffered, they are written directly to the output shift register. This means that new data for transmission cannot be written to the shift register until the previous transmission is complete. An attempt to write during data transmission will not go through; the transmission in progress will proceed undisturbed, and the MCU will set the write collision (WCOL) status bit in the serial peripheral status register (SPSR). After the last bit of a character is shifted out, the SPI transfer complete flag (SPIF) of the SPSR is set. This will also generate an interrupt if the SPIE (SPI interrupt enable) bit in the SPCR is set.

8.4.4 Slave Select ($\overline{SS}$)

The slave select ($\overline{SS}$) input is used to target specific devices in the SPI system. It must be pulled low on a targeted slave device prior to any communication with a master and must remain low for the duration of the transaction. $\overline{SS}$ must always be high on any device in master mode. Pulling $\overline{SS}$ low on a master mode device generates a mode fault error (see **8.5.1 Mode Fault Error**).

8.4.5 SPI Timing

Four possible timing relationships are available through control bits CPOL (clock polarity) and CPHA (clock phase) in the SPCR. These bits must be the same in both master and slave devices. The master device always places data on the MOSI line approximately a half-cycle before the SCK clock edge. This enables the slave device to latch the data. See **Figure 8-2**.

A write collision is normally a slave error because a slave has no control over when a master initiates a transfer. A master knows when a transfer is in progress, so there is no reason for a master to generate a write-collision error, although the SPI logic can detect write collisions in both master and slave devices.

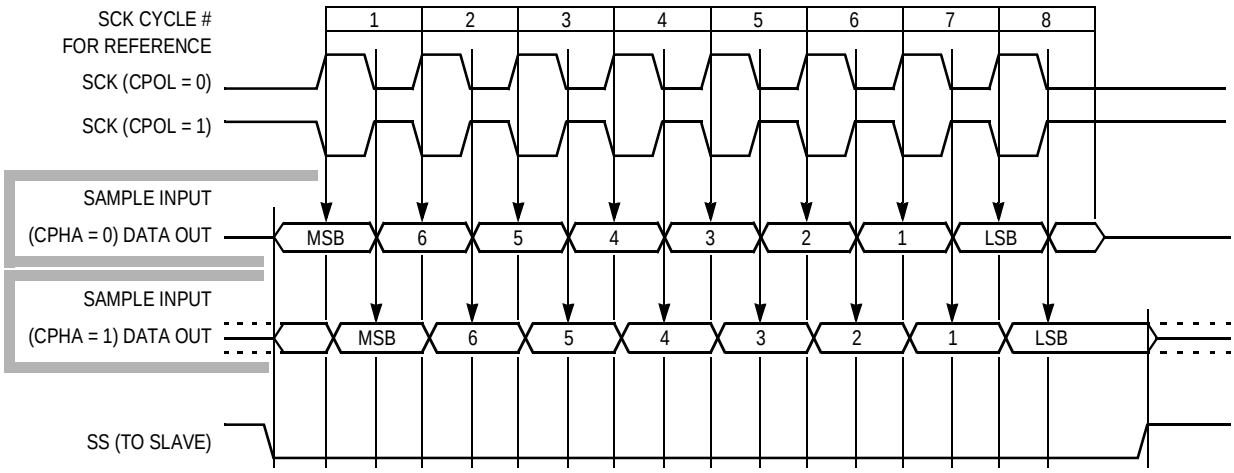


Figure 8-2. Data Clock Timing Diagram

- After a match occurs, change the appropriate OC1D bit to the opposite polarity, then add a value representing the width of the pulse to the original value and write it to the output compare register.

Because the pin state changes occur at specific values of the free-running counter, the pulse width can be controlled accurately to the resolution of the free-running counter, independent of software latencies. To generate an output signal of a specific frequency and duty cycle, repeat this pulse-generating procedure.

9.6.1 Timer Output Compare Registers

	Bit 7	6	5	4	3	2	1	Bit 0
Address:	$0016 — TOC1 (High)							
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1
Address:	$0017 — TOC1 (Low)							
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1
Address:	$0018 — TOC2 (High)							
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1
Address:	$0019 — TOC2 (Low)							
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1

Figure 9-13. Timer Output Compare Registers (TOC1–TOC4)

The three clocks are derived from the E clock by writing to registers which determine their scaling factors. The clock A frequency is equal to E divided by 1, 2, 4, or 8, depending on which bits (PCKA[2:1]) in the PWCLK register are set. The clock B frequency is equal to the E clock divided by a power of two determined by bits PCKB[3:1] in the PWCLK register. Clock S is derived by dividing clock A by the integer (1 to 256) stored in the PWSCAL register, then by two.

Two channels can be concatenated by setting the appropriate bit (CON34 or CON12) in the PWCLK register. In this mode, the clock source is determined by the low-order channel, which is channel two in CON12 and channel four in CON34. The output is also placed on the pin associated with the low-order channels, so when two channels are concatenated the pin associated with the high-order channel (PH0 and/or PH2) can be used for GPIO. A read of the high-order byte causes the low-order byte to be latched for one cycle to guarantee that double-byte reads are accurate. A write to the low-order byte of the counter causes reset of the entire counter. A write to the high-order byte of the counter has no effect.

9.9.2 Pulse-Width Modulation Control Registers

The PWM control registers are described here.

9.9.2.1 Pulse-Width Modulation Timer Clock Select Register

Address: $0060

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	CON34	CON12	PCKA2	PCKA1	0	PCKB3	PCKB2	PCKB1
Reset:	0	0	0	0	0	0	0	0

Figure 9-31. Pulse-Width Modulation Timer Clock Select (PWCLK)

9.9.2.4 Pulse-Width Modulation Timer Enable Register

Address: $0063

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TPWSL	DISCP	0	0	PWEN4	PWEN3	PWEN2	PWEN1
Reset:	0	0	0	0	0	0	0	0

Figure 9-34. Pulse-Width Modulation Timer Enable Register (PWEN)

TPWSL — PWM Scaled Clock Test Bit — factory use only; only accessible in special test mode

0 = Normal operation

1 = Clock S is output to PWSCAL register (test only)

DISCP — Disable Compare Scaled E-Clock Bit — factory use only; only accessible in special test mode

0 = Normal operation

1 = Match of period does not reset associated count register (test only)

PWEN[4:1] — Pulse-Width Enable for Channels [4:1] Bits

0 = Channel disabled

1 = Channel enabled at port H bits [3:0]

Table 11-1. CPU Address and Address Expansion Signals

Number of Banks	Window Size			
	8 Kbytes	16 Kbytes	32 Kbytes	32 Kbytes (Window Based at $4000)
2	ADDR[12:0] XA13	ADDR[13:0] XA14	ADDR[14:0] XA15	ADDR[13:0] XA[15:14]
4	ADDR[12:0] XA[14:13]	ADDR[13:0] XA[15:14]	ADDR[14:0] XA[16:15]	ADDR[13:0] XA[16:14]
8	ADDR[12:0] XA[15:13]	ADDR[13:0] XA[16:14]	ADDR[14:0] XA[17:15]	ADDR[13:0] XA[17:14]
16	ADDR[12:0] XA[16:13]	ADDR[13:0] XA[17:14]	ADDR[14:0] XA[18:15]	ADDR[13:0] XA[18:14]
32	ADDR[12:0] XA[17:13]	ADDR[13:0] XA[18:14]	— —	— —
64	ADDR[12:0] XA[18:13]	— —	— —	— —

The base address for each window must be an integer multiple of the window size, with one exception. When the window size is 32 Kbytes, the base address can be at $4000 as well as the 32-Kbyte multiples $0000 and $8000.

This special case requires a modification in address line deployment. Normally, when the bank size is 32 Kbytes and the bank address is $0000 or $8000, CPU address lines ADDR[14:0] select individual bytes within the 32-Kbyte space and the ADDR[14:0] pins are connected to address lines A[14:0] of the memory device. When the base address is $4000, the CPU address signal ADDR14 must be inverted to allow 32 Kbytes of contiguous memory. To do this, the CPU drives the inverted ADDR14 signal onto the XA14 pin when the window is active, and the non-inverted CPU ADDR14 signal onto the XA14 pin when the window is not active. Therefore, address 14 of the memory device must be connected to expansion line XA14 rather than normal address line ADDR14.

If the two memory windows overlap, window 1 has priority, and only the portion of window 2 that does not overlap window 1 remains active. If a

11.3.2.4 Memory Mapping Window Control Registers

Each of the memory mapping window control registers (MM1CR and MM2CR) determine the active memory bank for the corresponding window, containing the value to be output on the expansion address lines when the CPU selects addresses within its extended memory window. To change banks, write the address of the new bank into the appropriate window register.

Address: $0058 Memory Mapping Window 1 Control Register (MM1CR)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	X1A18	X1A17	X1A16	X1A15	X1A14	X1A13	0
Reset:	0	0	0	0	0	0	0	0

Address: $0059 Memory Mapping Window 2 Control Register (MM1CR)

Read: Write:	0	X2A18	X2A17	X2A16	X2A15	X2A14	X2A13	0
Reset:	0	0	0	0	0	0	0	0

Figure 11-4. Memory Mapping Window Control Registers (MM1CR and MM2CR)

X1A[18:13] — Memory Mapping Window 1 Expansion Address Line Select Bits

X2A[18:13] — Memory Mapping Window 2 Expansion Address Line Select Bits

Each bit value written to the MMxCR registers is driven on the corresponding port G expansion address line (if enabled by PGAR) to enable the specified bank in the window.

11.4.2 Input/Output Chip Select

The I/O chip select (CSIO) is programmable for a 4-Kbyte size located at addresses $1000–$1FFF or 8-Kbyte size located at addresses $0000–$1FFF. The default active-low polarity can be changed to active high by setting the IOPL bit in CSCTL. Default validity during high E clock can be changed to address valid time by setting the IOCSA bit in CSCTL. Clock stretching can be set from zero to three cycles (See **11.4.5 Clock Stretching**). CSIO is disabled out of reset.

Address: $005B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	IOEN	IOPL	IOCSA	IOSZ	GCSPR	PCSEN	PCSZA	PCSZB
Reset:	0	0	0	0	0	1	0	0

Figure 11-6. Chip-Select Control Register (CSCTL)

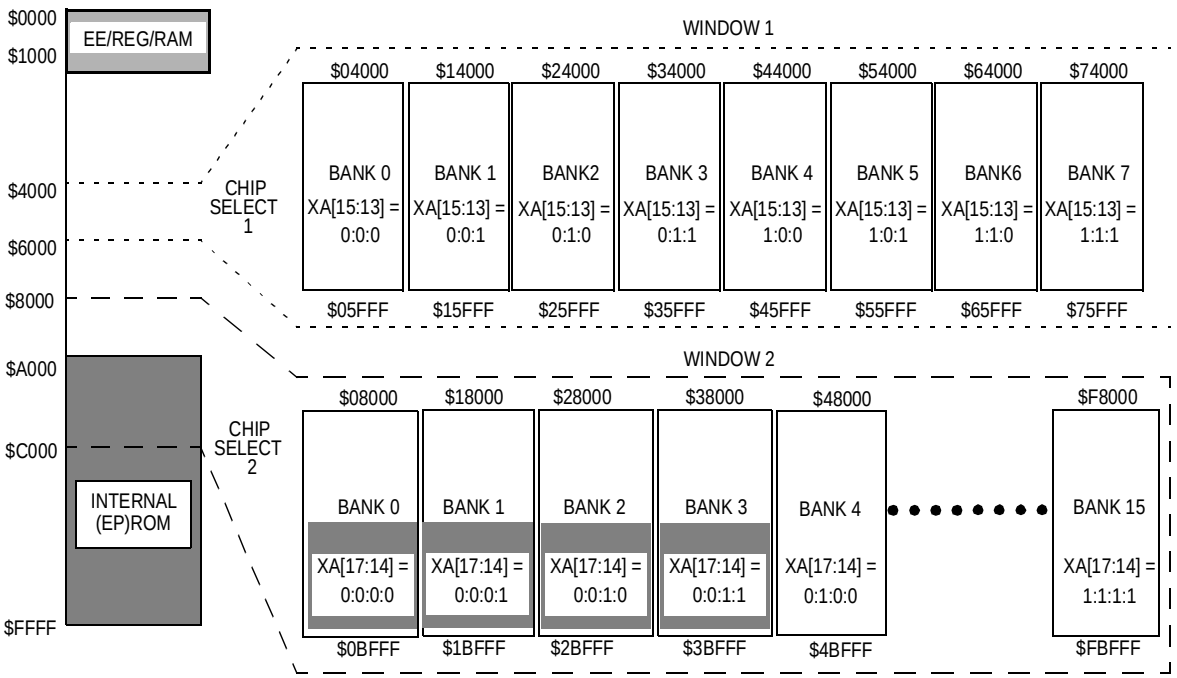
IOEN — I/O Chip-Select Enable Bit
0 = CSIO is disabled and port H bit 4 is GPIO.
1 = CSIO is enabled and uses port H bit 4.

IOPL — I/O Chip-Select Polarity Select Bit
0 = CSIO active low
1 = CSIO active high

IOCSA — I/O Chip-Select Address Valid Bit
0 = CSIO is valid during E-clock high time.
1 = CSIO is valid during address valid time.

IOSZ — I/O Chip-Select Size Select Bit
0 = CSIO size is four Kbytes at $1000–$1FFF.
1 = CSIO size is eight Kbytes at $0000–$1FFF.

The second example system shown in **Figure 11-16** contains two memory windows. The first window is organized as in the previous example, 8 banks of 8 Kbytes each. The second window accesses 256 Kbytes of memory in 16 banks of 16 Kbyte each. To access 16 Kbytes, or 2^{14} address locations, the CPU will need 14 address lines, ADDR[13:0]. Since ADDR13 is driven on XA13 in this example, XA13 replaces ADDR13 to drive the A13 line in the 6226 devices, but ADDR13 could be used as well. 16 (2^4) memory banks require four expansion address lines, A[17:14]. Refer to **Figure 11-16** for a memory map and schematic drawing of this system.



PGAR	= $1F	XA[17:13]	CSCTL	= $00	No I/O or program chip selects
MMWBR	= $84	Window 1 @ $4000 Window 2 @ $8000	GPCS1A	= $00	General-purpose chip select 1 from $00000
			GPCS1C	= $06	64 KByte range (8 x 8 K)
MMSIZ	= $E1	Window 1 = 8 Kbytes Window 2 = 16 Kbytes GPCS1, GPCS2 based on expansion address	GPCS2A	= $00	General-purpose chip select 2 from $00000
			GPCS2C	= $08	256 KByte range (16 x 16 K)

Figure 11-16. Memory Expansion Example 2 (Sheet 1 of 2)
Memory Map for One 8-Kbyte Window with Eight Banks and One 16-Kbyte Window with 16 Banks of External Memory

12.4 Functional Operating Range

Rating	Symbol	Value	Unit
Operating temperature range MC68HC(7)11KC MC68HC(7)11KV MC68HC(7)11KM	T_A	T_L to T_H –40 to +85 –40 to +105 –40 to +125	°C
Operating voltage range	V_{DD}	5.0 ± 10%	V

12.5 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Average junction temperature	T_J	$T_A + (P_D \times \Theta_{JA})$	°C
Ambient temperature	T_A	User-determined	°C
Package thermal resistance (junction-to-ambient) 80-pin low-profile quad flat pack 68-pin plastic leaded chip carrier 68-pin windowed ceramic cerquad (EPROM) 84-pin plastic leaded chip carrier 80-pin quad flat pack 84-pin J-cerquad	Θ_{JA}	 80 50 60 50 85 50	°C/W
Total power dissipation(1)	P_D	$P_{INT} + P_{I/O}$ $K / T_J + 273$ °C	W
Device internal power dissipation	P_{INT}	$I_{DD} \times V_{DD}$	W
I/O pin power dissipation(2)	$P_{I/O}$	User-determined	W
A constant(3)	K	$P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2$	W/°C

1. This is an approximate value, neglecting $P_{I/O}$.
2. For most applications, $P_{I/O} \leq P_{INT}$ and can be neglected.
3. K is a constant pertaining to the device. Solve for K with a known T_A and a measured P_D (at equilibrium). Use this value of K to solve for P_D and T_J iteratively for any value of T_A.

12.6 Electrical Characteristics

Characteristic[1]	Symbol	Min	Max	Unit
Output voltage, I_{Load} = ± 10.0 µA[2]) All outputs except XTAL All outputs except XTAL, RESET, and MODA	V_{OL} V_{OH}	— V_{DD} – 0.1	0.1 —	V
Output high voltage, I_{Load} = – 0.8 mA, V_{DD} = 4.5 V[2] All outputs except XTAL, RESET, and MODA	V_{OH}	V_{DD} – 0.8	—	V
Output low voltage, I_{Load} = 1.6 mA All outputs except XTAL	V_{OL}	—	0.4	V
Input high voltage All inputs except RESET RESET	V_{IH}	0.7 x V_{DD} 0.8 x V_{DD}	V_{DD} + 0.3 V_{DD} + 0.3	V
Input low voltage All Inputs	V_{IL}	V_{SS} – 0.3	0.2 x V_{DD}	V
I/O ports, three-state leakage, V_{In} = V_{IH} or V_{IL} Ports A, B, C, D, F, G, H, MODA/LIR, RESET	I_{OZ}	—	±10	µA
Input leakage current, V_{In} = V_{DD} or V_{SS}[3] IRQ, XIRQ on standard devices MODB/V_{STBY}, XIRQ on EPROM devices	I_{In}	— —	±1 ±10	µA
Input current with pullup resistors, V_{In} = V_{IL} Ports B, F, G, and H	I_{IPR}	100	500	µA
RAM standby voltage, power down	V_{SB}	2.0	V_{DD}	V
RAM standby current, power down	I_{SB}	—	10	µA
Input capacitance PE[7:0], IRQ, XIRQ, EXTAL Ports A, B, C, D, F, G, H, MODA/LIR, RESET	C_{In}	— —	8 12	pF
Output load capacitance All outputs except PD[4:1], XOUT, XTAL, MODA/LIR PD[4:1] XOUT	C_L	— — —	90 200 30	pF

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted
2. V_{OH} specification for RESET and MODA is not applicable because they are open-drain pins. V_{OH} specification not applicable to ports C and D in wired-OR mode.
3. Refer to **12.10 Analog-to-Digital Converter Characteristics** for leakage current for port E.

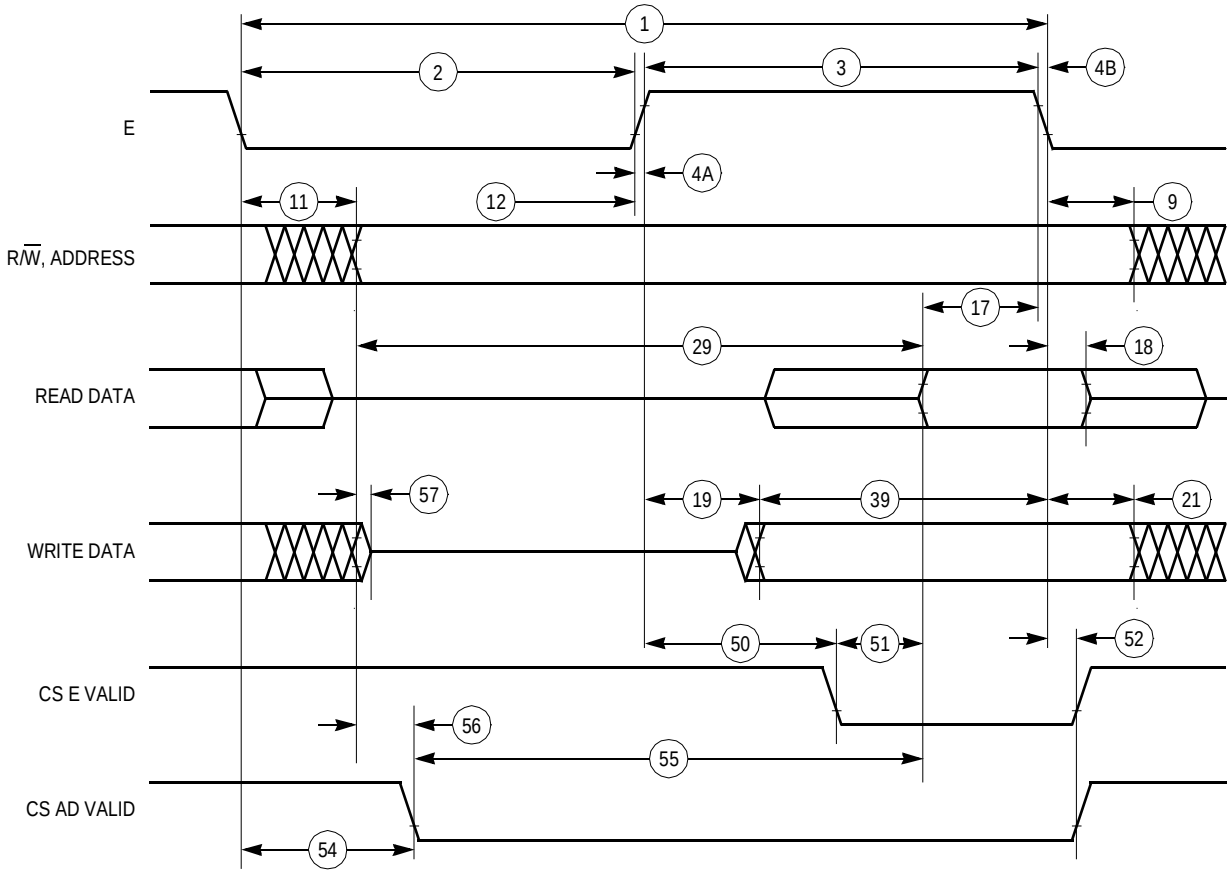
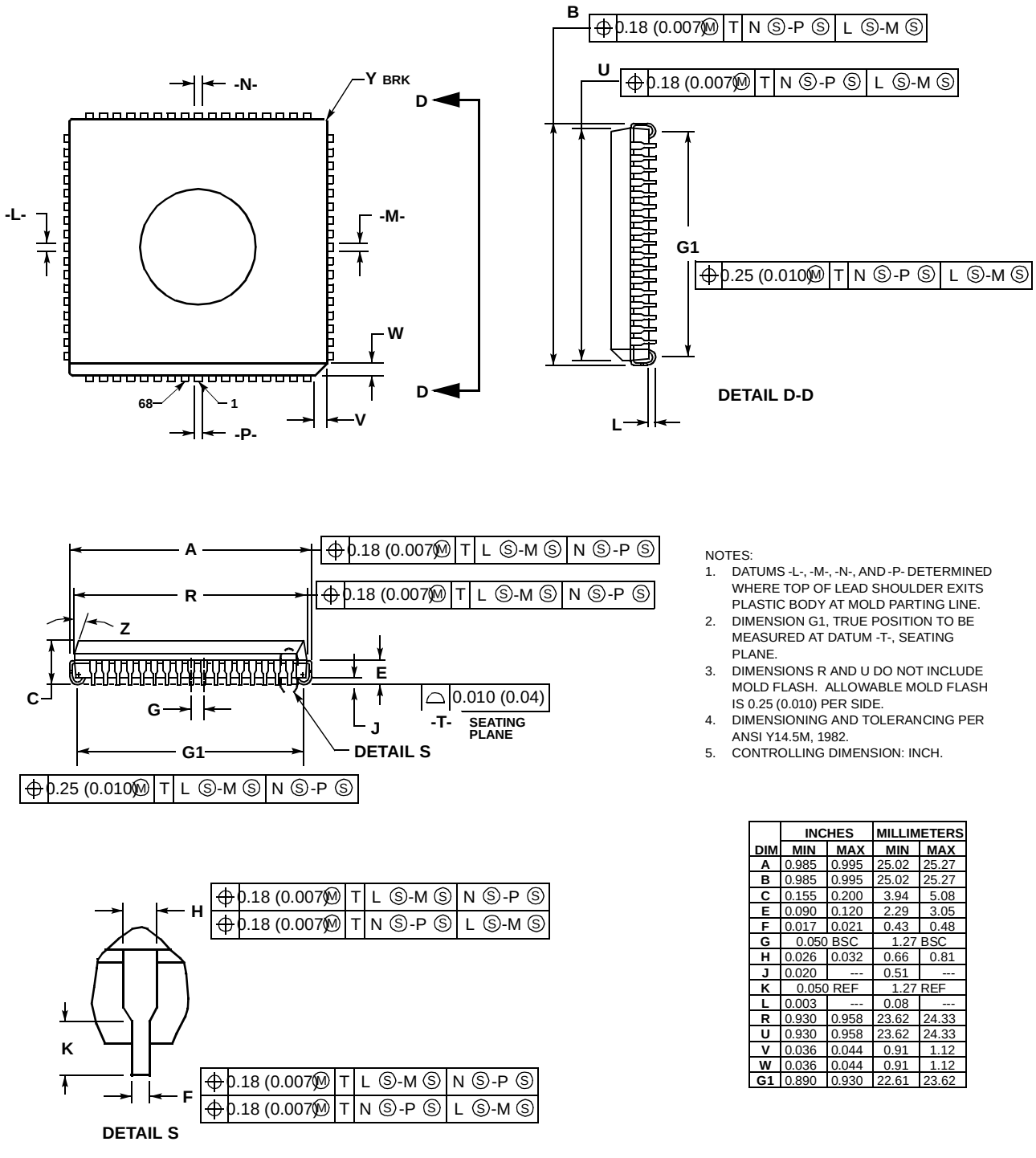


Figure 12-9. Expansion Bus Timing

13.8 68-Pin J-Cerquad (Case 779A)



NOTES:
1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.985	0.995	25.02	25.27
B	0.985	0.995	25.02	25.27
C	0.155	0.200	3.94	5.08
E	0.090	0.120	2.29	3.05
F	0.017	0.021	0.43	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.050 REF		1.27 REF	
L	0.003	---	0.08	---
R	0.930	0.958	23.62	24.33
U	0.930	0.958	23.62	24.33
V	0.036	0.044	0.91	1.12
W	0.036	0.044	0.91	1.12
G1	0.890	0.930	22.61	23.62

OPTION System Configuration Options
CME Clock Monitor Enable 111
CR[1:0] COP Timer Rate Select Bits. 109
DLY Enable Oscillator Startup Delay. 132
IRQE Configure IRQ for Edge-Sensitive Operation. 121

P

PACTL Pulse Accumulator Control
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