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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	4MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	37
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	640 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.29x29.29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc11k1cfn4

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2.1 Contents

2.2 Introduction

The M68HC11K Family is available in a variety of packages, as shown in **Table 1-1. M68HC11K Family Devices**. Most pins on this MCU serve two or more functions, as described in this section. Pin assignments for the various package types are shown in **Figure 2-1**, **Figure 2-2**, **Figure 2-3**, and **Figure 2-4**.

there are no special requirements for alignment of instructions or operands.

3.5 Opcodes and Operands

The M68HC11 Family of microcontrollers uses 8-bit opcodes. Every instruction requires a unique opcode for each of its addressing modes. The resulting number of opcodes exceeds the 256 available in an 8-bit binary number. A 4-page opcode map has been implemented to accommodate the extra instructions. An additional byte, called a prebyte, directs the processor from page 0 of the opcode map to one of the other three pages. As its name implies, the additional byte precedes the opcode.

A complete instruction consists of a prebyte, if any, an opcode, and zero to three operands. The operands contain information the CPU needs for executing the instruction. Complete instructions can be from one to five bytes long.

3.6 Addressing Modes

Six addressing modes can be used to access memory:

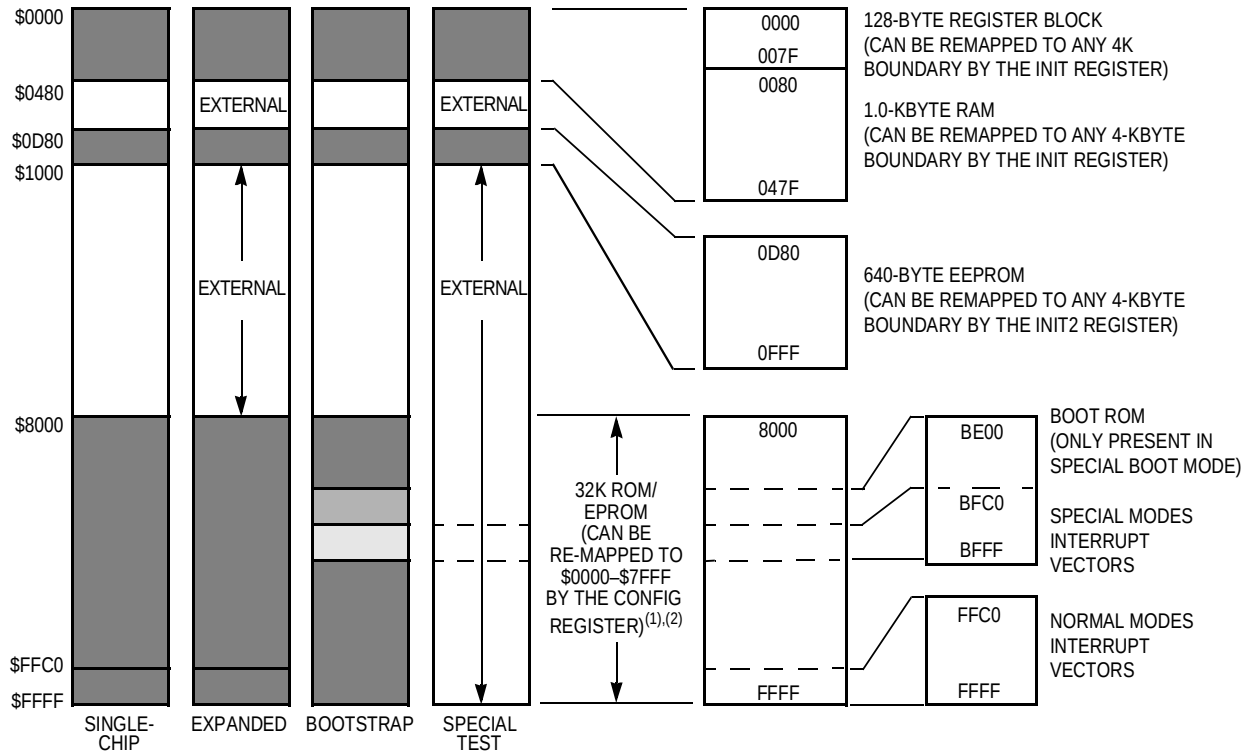
1. Immediate
2. Direct
3. Extended
4. Indexed
5. Inherent
6. Relative

All modes except inherent mode use an effective address. The effective address is the memory address where the argument is fetched or stored or the address from which execution is to proceed. The effective address can be specified within an instruction or it can be calculated.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0062	Pulse Width Modulation Timer Prescaler Register (PWSCAL) See page 215.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$0063	Pulse Width Modulation Timer Enable Register (PWEN) See page 216.	Read: Write:	TPWSL	DISCP	0	0	PWEN4	PWEN3	PWEN2	PWEN1
		Reset:	0	0	0	0	0	0	0	0
$0064	Pulse Width Modulation Timer Counter 1 Register (PWCNT1) See page 217.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$0065	Pulse Width Modulation Timer Counter 2 Register (PWCNT2) See page 217.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$0066	Pulse Width Modulation Timer Counter 3 Register (PWCNT3) See page 217.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$0067	Pulse Width Modulation Timer Counter 4 Register (PWCNT4) See page 217.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$0068	Pulse Width Modulation Timer Period 1 Register (PWPER1) See page 218.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$0069	Pulse Width Modulation Timer Period 2 Register (PWPER2) See page 218.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$006A	Pulse Width Modulation Timer Period 3 Register (PWPER3) See page 218.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$006B	Pulse Width Modulation Timer Period 4 Register (PWPER4) See page 218.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Undefined

Figure 4-1. Register and Control Bit Assignments (Sheet 9 of 11)



Note: 1.EPROM can be enabled in special test mode by setting the ROMON bit in the CONFIG register after reset.

Figure 4-4. M68HC11KS2 Family Memory Map

Table 4-4 shows the default memory map addresses for the M68HC11K Family devices.

Table 4-4. Default Memory Map Addresses

	[7]11K4	[7]11KS2
Registers	$0000–$007F	$0000–$007F
RAM	$0080–$037F	$0080–$047F
EEPROM	$0D80–$0FFF	$0D80–$0FFF
ROM/EPROM	$A000–$FFFF	$8000–$FFFF

Three registers are involved in COP operation:

- The CONFIG register contains a bit which determines whether the COP system is enabled or disabled.
- The OPTION register contains two bits which determine the COP timeout period.
- The COPRST register must be written by software to reset the watchdog timer.

NOTE: *Throughout this manual, the registers are discussed by function. In the event that not all bits in a register are referenced, the bits that are not discussed are shaded.*

5.3.3.1 System Configuration Register

In normal modes, COP is enabled out of reset and does not depend on software action. To disable the COP system, set the NOCOP bit in the CONFIG register (see **Figure 5-1**). In special test and bootstrap operating modes, the COP system is initially inhibited by the disable resets (DISR) control bit in the TEST1 register. The DISR bit can subsequently be written to 0 to enable COP resets.

Address: $003F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ROMAD	1	CLKX	PAREN	NOSEC	NOCOP	ROMON	EEON
Reset:	—	1	—	—	1	—	—	—

Figure 5-1. System Configuration Register (CONFIG)

NOTE: *CONFIG is writable once in normal modes and writable at any time in special modes.*

NOCOP — COP System Disable Bit
0 = COP enabled
1 = COP disabled

  - The RDRF, IDLE, OR, NF, FE, PF, and RAF receive-related status bits are cleared.

- Serial peripheral interface (SPI)
  - The SPI system is disabled by reset.
  - The port pins associated with this function default to being general-purpose I/O lines.
- Analog-to-digital (A/D) converter
  - The ADPU bit in the OPTION register is cleared, disabling the A/D system.
  - The conversion complete flag in the ADCTL register is also cleared.
- System
  - The external $\overline{\text{IRQ}}$ pin has the highest I-bit interrupt priority because PSEL[4:0] in the HPRIO register are initialized with the value %00110 (where % indicates a binary value).
  - The RBOOT, SMOD, and MDA bits in the HPRIO register reflect the status of the MODB and MODA inputs at the rising edge of reset.
  - The $\overline{\text{IRQ}}$ pin is configured for level-sensitive operation for wired-OR systems.
  - The DLY control bit in the OPTION register is set, enabling oscillator startup delay after recovery from stop mode.
  - The clock monitor system is disabled because the CME and FCME bits in the OPTION register are cleared.

5.5 Interrupts

The MCU has 18 interrupt vectors that support 22 interrupt sources. The 19 maskable interrupts are generated by on-chip peripheral systems. They are recognized when the I bit in the CCR is clear. The three non-maskable interrupt sources are illegal opcode trap, software interrupt, and $\overline{\text{XIRQ}}$ pin. **Table 5-5** lists the interrupt sources and vector assignments for each source.

The M68HC11K series offers several enhancements to the basic MC68HC11 SCI, including:

- 13-bit modulus prescaler in the baud generator
- Receiver-active flag
- Transmitter and receiver hardware parity
- Accelerated idle line detection

7.3 Data Format

The SCI uses the standard non-return to zero mark/space data format illustrated in **Figure 7-1**.

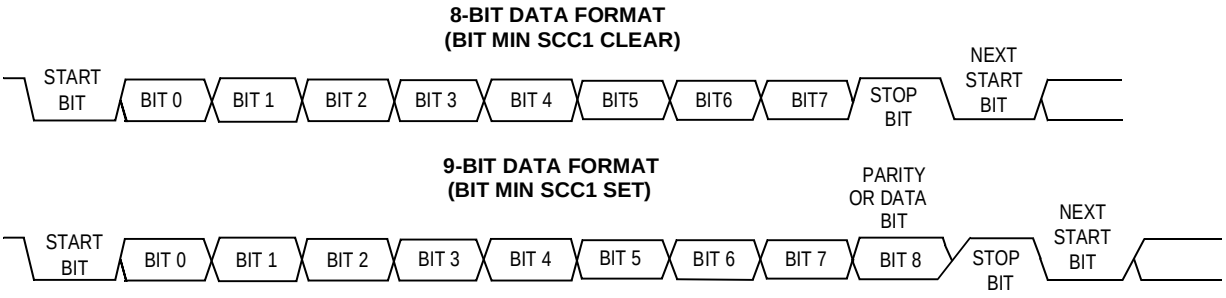


Figure 7-1. SCI Data Formats

Data is transmitted in frames consisting of a start bit, a word of eight or nine data bits, and a stop bit. The step-by-step transmission procedure is:

1. The transmission line is idle before a message is transmitted. This means that the line is in a logic 1 state for at least one frame time.
2. A start bit, logic 0, is transmitted, indicating the start of a frame.
3. An 8-bit or 9-bit word is transmitted, least significant bit (LSB) first.
4. A stop bit, logic 1, is transmitted to indicate the end of a frame.
5. An optional number of breaks can be transmitted. A break is the transmission of a logic low state for one frame time. After the last break character is sent, the line goes high for at least one bit time.

7.5 Receive Operation

During receive operations, data from the TxD pin is shifted into the serial shift register. A completed word is parallel-loaded to a receive data register (RDR), which can be read through SCDRH/L. This double-buffered operation allows reception of the current character while the MCU reads the previous character.

The SCI receiver has seven status flags, summarized in Table 7-1.

Table 7-1. SCI Receiver Flags

Flag	Name	Set When	Interrupt Enable Bit
RDRF	Receive data register full	Character transferred from shift register to RDR	RIE
IDLE	Idle-line detected	Active transmit line goes idle	ILIE
OR	Overrun error	Character ready for RDR while previous character unread	RIE
NF	Noise error	Samples of data bit not unanimous	—
FE	Frame error	0 detected where stop bit expected	—
PF	Parity error	Calculated parity does not match data parity bit	—
RAF	Receiver active	A character is being received	—

Three of the flags can generate interrupt requests if the corresponding enable bits in SCCR2 are set. The status flags are set by the SCI logic in response to specific conditions in the receiver. These flags can be read (polled) at any time by software. Each bit except RAF is cleared by reading SCSR1 and SCDR sequentially.

- The receive data register full (RDRF) flag is set when the last bit of a character is received and data is transferred from the shift register to the RDR.
- The IDLE flag is set after a transition on the RxD line from an active state to an idle state. This prevents repeated interrupts during the time RxD remains idle.

9.4.5 Pulse Accumulator Control Register

Address: $0026

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	PAEN	PAMOD	PEDGE	0	I4/O5	RTR1	RTR0
Reset:	0	0	0	0	0	0	0	0

Figure 9-7. Pulse Accumulator Control Register (PACTL)

I4/O5 — Input Capture 4/Output Compare 5 Bit
0 = Configure PA3 as OC5
1 = Configure PA3 as IC4

To configure PA3 as input compare 4, clear DDA3 and set I4/05. To configure PA3 as output compare 5, set DDA3 and clear I4/05. If the DDA3 bit is set (configuring PA3 as an output) and IC4 is enabled, writing a one to TI4/O5 causes an input capture. Writing to TI4/O5 has no effect when DDA3 is cleared and/or OC5 is enabled.

9.5 Input Capture (IC)

The input capture function records the time an external event occurs by latching the value of the free-running counter into one of the timer input capture (TIC) registers when a selected edge is detected at its associated timer input pin. Software can store latched values and use them to compute the period and duration of events. For example, by storing the times of successive edges of an incoming signal, software can determine the period and pulse width of a signal. To measure the period, two successive edges of the same polarity are captured. To measure pulse width, two alternate polarity edges are captured.

Capture requests are latched on the opposite half cycle of PH2 from when the timer counter is being incremented. This synchronization process introduces a delay between edge occurrence and counter value detection. Because these delays offset each other when the time between two edges is measured, they can be ignored. There is a similar delay for output compare between the actual compare point and when the output pin changes state.

9.5.3 Timer Interrupt Flag 1 Register

Address: $0023

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F
Reset:	0	0	0	0	0	0	0	0

Figure 9-10. Timer Interrupt Flag 1 Register (TFLG1)

Clear each flag by writing a 1 to the corresponding bit position.

ICxF — Input Capture x Flag

Set each time a selected active edge is detected on the corresponding input capture line.

I4/O5F — Input Capture 4/Output Compare 5 Flag

Set each time a selected active edge is detected on the IC4 line if IC4 is enabled.

9.5.4 Timer Interrupt Mask 1 Register

Address: $0022

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I
Reset:	0	0	0	0	0	0	0	0

Figure 9-11. Timer Interrupt Mask 1 Register (TMSK1)

Bits in TMSK1 correspond bit for bit with flag bits in TFLG1.

ICxI — Input Capture Interrupt Enable Bit

If the ICxI enable bit is set when the ICxF flag bit is set, a hardware interrupt sequence is requested.

10.4.3 Analog-to-Digital Converter Result Registers

These read-only registers hold an 8-bit conversion result. Writes to these registers have no effect. Data in the A/D converter result registers is valid when the CCF flag in the ADCTL register is set, indicating a conversion sequence is complete. If conversion results are needed sooner, refer to **Figure 10-2**, which shows the A/D conversion sequence diagram.

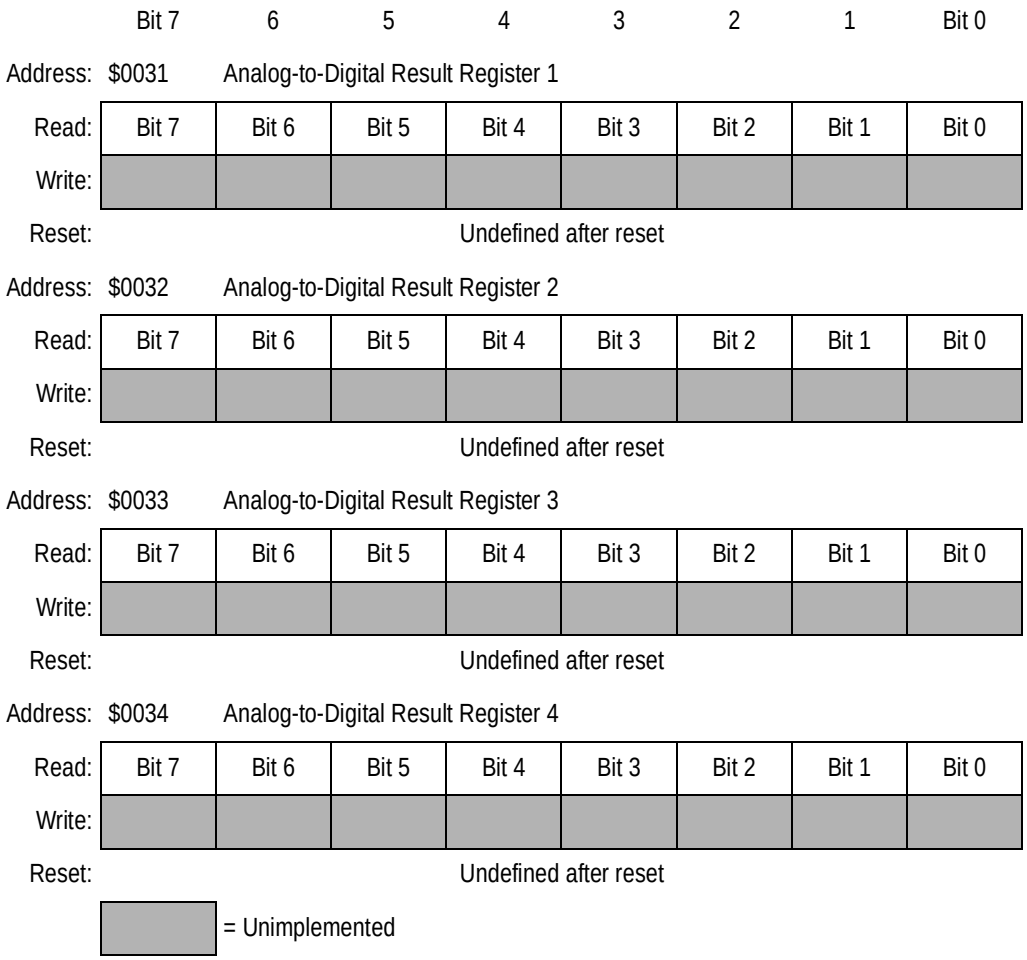


Figure 10-5. Analog-to-Digital Result Registers (ADR1–ADR4))

11.3.2.3 Memory Mapping Window Base Register

The memory mapping window base register (MMWBR) defines the starting address of each of the two windows within the CPU 64-Kbyte address range. The windows normally begin at a boundary related to their size (an 8-Kbyte window can begin on any 8-Kbyte boundary, beginning at $0000).

Address: $0057

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	W2A15	W2A14	W2A13	0	W1A15	W1A14	W1A13	0
Reset:	0	0	0	0	0	0	0	0

Figure 11-3. Memory Mapping Window Base Register (MMWBR)

W2A[15:13] — Window 2 Base Address Bits

Selects the three most significant bits (MSB) of the base address for memory mapping window 2. Refer to **Table 11-3**.

W1A[15:13] — Window Base 1 Address Bits

Selects the three MSB of the base address for memory mapping window 1. Refer to **Table 11-3**.

Table 11-3. Memory Expansion Window Base Address

MSB Bits	Window Base Address		
WxA[15:13]	8 Kbytes	16 Kbytes	32 Kbytes
000	$0000	$0000	$0000
001	$2000	$0000	$0000
010	$4000	$4000	$4000
011	$6000	$4000	$4000
100	$8000	$8000	$8000
101	$A000	$8000	$8000
110	$C000	$C000	$8000
111	$E000	$C000	$8000

11.4.3.3 General-Purpose Chip Select 1 Control Register

Address: $005D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	G1DG2	G1DPC	G1POL	G1AV	G1SZA	G1SZB	G1SCC	G1SZD
Reset:	0	0	0	0	0	0	0	0

Figure 11-9. General-Purpose Chip Select 1 Control Register (GPCS1C)

G1POL — General-Purpose Chip Select 1 Polarity Select Bit

0 = CSGP1 active low

1 = CSGP1 active high

G1AV — General-Purpose Chip Select 1 Address Valid Select Bit

0 = CSGP1 is valid during E high time.

1 = CSGP1 is valid during address valid time.

G1SZ[A:D] — General-Purpose Chip Select 1 Size Bits

They select the range of GPCS1. Refer to **Table 11-6**.

Table 11-6. General-Purpose Chip Select 1 Size Control

G1SZ[A:D]	Size (Bytes)	Valid Bits (MXGS1 = 0)	Valid Bits (MXGS1 = 1)
0 0 0 0	Disabled	None	None
0 0 0 1	2 K	G1A[15:11]	G1A[18:11]
0 0 1 0	4 K	G1A[15:11]	G1A[18:12]
0 0 1 1	8 K	G1A[15:13]	G1A[18:13]
0 1 0 0	16 K	G1A[15:14]	G1A[18:14]
0 1 0 1	32 K	G1A[15]	G1A[18:15]
0 1 1 0	64 K	None	G1A[18:16]
0 1 1 1	128 K	None	G1A[18:17]
1 0 0 0	256 K	None	G1A18
1 0 0 1	512 K	None	None
1 0 1 0	Follow window 1	None	None
1 0 1 1	Follow window 2	None	None
1100–1111	Default to 512 K	None	None

Table 11-8. One Chip Select Driving Another

G1DG2	G1DPC	G2DPC	Program CS Pin is Asserted When Address is in:	General 2 CS Pin is Asserted When Address is in:	General 1 CS Pin is Asserted When Address is in:
0	0	0	A valid program area	A valid general 2 area	A valid general 1 area
0	0	1	A valid program or general 2 area	Never asserted	A valid general 1 area
0	1	0	A valid program or general 1 area	A valid general 2 area	Never asserted
0	1	1	A valid program or general 1 or 2 area	Never asserted	Never asserted
1	0	0	A valid program area	A valid general 2 or general 1 area	Never asserted
1	0	1	A valid program or general 2 area	Never asserted	A valid general 1 area
1	1	0	A valid program or general 1 area	A valid general 2 area	Never asserted
1	1	1	A valid program or general 1 or 2 area	Never asserted	Never asserted

11.4.5 Clock Stretching

Chip select and bus control signals are synchronized with the external E clock. To accommodate devices that are slower than the MCU, the E clock can be stretched when a chip select is asserted so that it remains high for one to three extra bus cycles. During this stretch, which can occur only during accesses to addresses in that chip select's address range, the other clocks continue running normally, maintaining the integrity of the timers and baud generators. Each chip select has two associated bits in the chip-select clock stretch (CSCSTR) register that set its clock stretching from zero (disabled) to three cycles.

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