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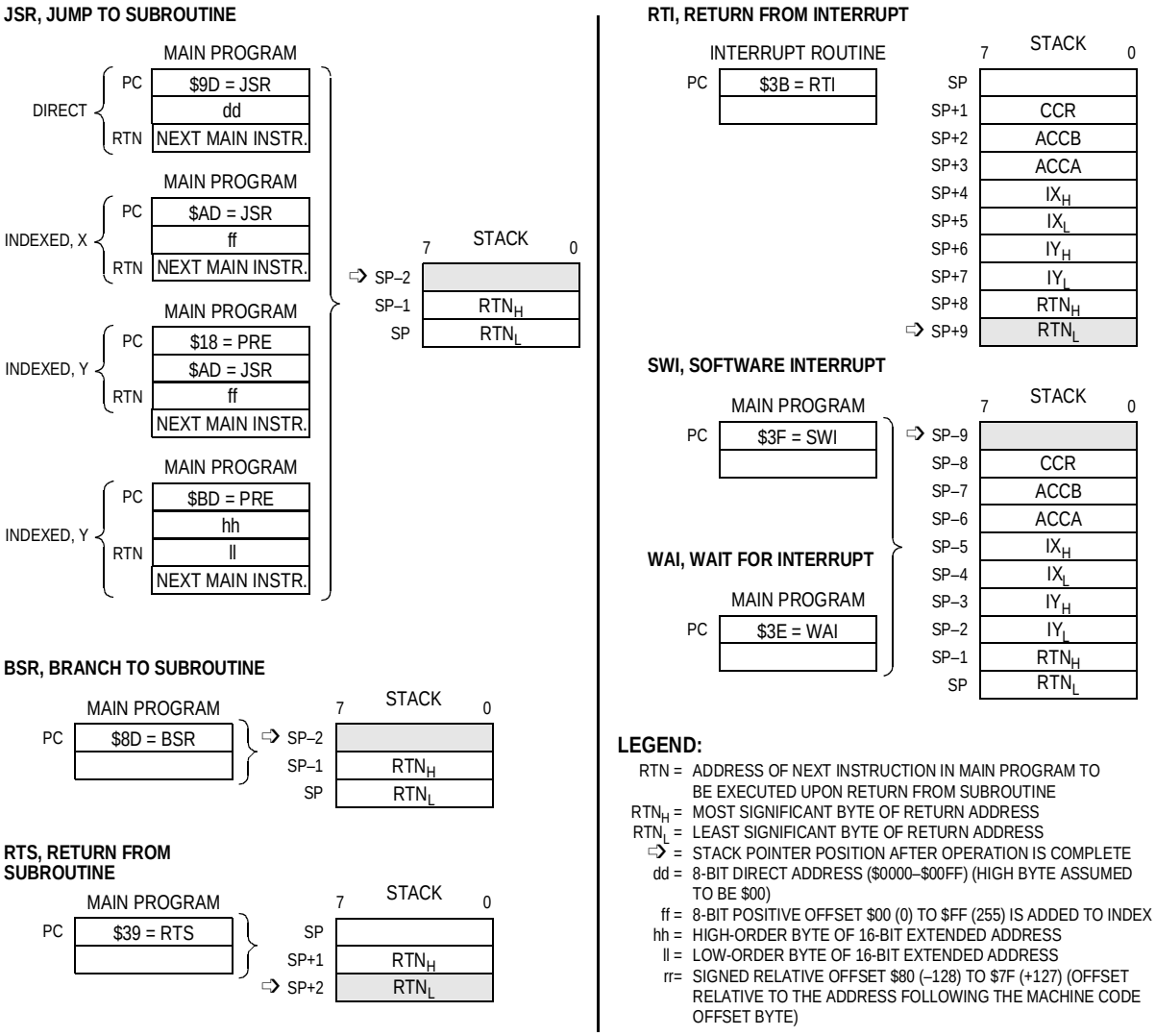
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	3MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	37
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	640 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.29x29.29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc11k1cfne3



LEGEND:

RTN = ADDRESS OF NEXT INSTRUCTION IN MAIN PROGRAM TO BE EXECUTED UPON RETURN FROM SUBROUTINE
RTN_H = MOST SIGNIFICANT BYTE OF RETURN ADDRESS
RTN_L = LEAST SIGNIFICANT BYTE OF RETURN ADDRESS
⇨ = STACK POINTER POSITION AFTER OPERATION IS COMPLETE
dd = 8-BIT DIRECT ADDRESS ($0000–$00FF) (HIGH BYTE ASSUMED TO BE $00)
ff = 8-BIT POSITIVE OFFSET $00 (0) TO $FF (255) IS ADDED TO INDEX
hh = HIGH-ORDER BYTE OF 16-BIT EXTENDED ADDRESS
ll = LOW-ORDER BYTE OF 16-BIT EXTENDED ADDRESS
rr= SIGNED RELATIVE OFFSET $80 (–128) TO $7F (+127) (OFFSET RELATIVE TO THE ADDRESS FOLLOWING THE MACHINE CODE OFFSET BYTE)

Figure 3-2. Stacking Operations

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0028	Serial Peripheral Control Register (SPCR) See page 174.	Read: Write:	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
		Reset:	0	0	0	0	0	1	U	U
$0029	Serial Peripheral Status Register (SPSR) See page 176.	Read: Write:	SPIF	WCOL	0	MODF	0	0	0	0
		Reset:	0	0	0	0	0	0	0	0
$002A	Serial Peripheral Data Register (SPDR) See page 177.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	Undefined after reset							
$002B	EPROM Programming Control Register (EPROG)(1) See page 91.	Read: Write:	R	0	ELAT	EXCOL	EXROW	0	0	EPGM
		Reset:	0	0	0	0	0	0	0	0

1. Present only in EPROM (711) devices

$002C	Port Pullup Assignment Register (PPAR) See page 147.	Read: Write:	0	0	0	0	HPPUE	GPPUE	FPPUE	BPPUE
		Reset:	0	0	0	0	1	1	1	1
$002D	Port G Assignment Register (PGAR) See page 235.	Read: Write:	0	0	PGAR5	PGAR4	PGAR3	PGAR2	PGAR1	PGAR0
		Reset:	0	0	0	0	0	0	0	0
$002E	System Configuration Options 3 Register (OPT3)(2) See page 132.	Read: Write:		SM						
		Reset:	0	0	0	0	0	0	0	0

2. Not available on M68HC11K4 devices

$002F	Reserved		R	R	R	R	R	R	R	R
$0030	Analog-to-Digital Control/Status Register (ADCTL) See page 227.	Read: Write:	CCF	0	SCAN	MULT	CD	CC	CB	CA
		Reset:	0	0	U	U	U	U	U	U
$0031	Analog-to-Digital Results Register 1 (ADR1) See page 229.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Undefined after reset							

= Unimplemented R = Reserved U = Undefined

Figure 4-1. Register and Control Bit Assignments (Sheet 5 of 11)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$006C	Pulse Width Modulation Timer Duty Cycle 1 Register (PWDTY1) See page 219.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$006D	Pulse Width Modulation Timer Duty Cycle 2 Register (PWDTY2) See page 219.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$006E	Pulse Width Modulation Timer Duty Cycle 3 Register (PWDTY3) See page 219.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$006F	Pulse Width Modulation Timer Duty Cycle 4 Register (PWDTY4) See page 219.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$0070	SCI Baud Rate Control Register High (SCBDH) See page 158.	Read: Write:	BTST	BSPL	0	SBR12	SBR11	SBR10	SBR9	SBR8
		Reset:	0	0	0	0	0	0	0	0
$0071	SCI Baud Rate Control Register Low (SCBDL) See page 158.	Read: Write:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		Reset:	0	0	0	0	0	1	0	0
$0072	SCI Control Register 1 (SCCR1) See page 160.	Read: Write:	LOOPS	WOMS	0	M	WAKE	ILT	PE	PT
		Reset:	U	U	0	0	0	0	0	0
$0073	SCI Control Register 2 (SCCR2) See page 161.	Read: Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Reset:	0	0	0	0	0	0	0	0
$0074	SCI Status Register 1 (SCSR1) See page 162.	Read: Write:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Reset:	0	0	0	0	0	0	0	0
$0075	SCI Status Register 2 (SCSR2) See page 164.	Read:	0	0	0	0	0	0	0	RAF
		Write:								
		Reset:	1	1	0	0	0	0	0	0
$0076	SCI Data Register (SCDR) See page 165.	Read: Write:	R8	T8	0	0	0	0	0	0
		Reset:	Undefined after reset							

= Unimplemented R = Reserved U = Undefined

Figure 4-1. Register and Control Bit Assignments (Sheet 10 of 11)

Port B provides the high-order address byte (Addr[15:8]), port F the low-order address byte (Addr[7:0]), port C the data bus (Data[7:0]), and port G pin 7 the read/write line (R/$\overline{W}$) which controls direction of data flow.

Additionally, the E clock output can be used to synchronize external decoders for enable signals.

Expanded mode also enables these two special features available only on the K4 Family devices:

1. Memory expansion uses port G[5:0] to increase the available external address space to 1 Mbyte.
2. Four chip-select lines on port H[7:4] simplify selection of external memory devices.

Both of these features are described in **Section 11. Memory Expansion and Chip Selects**.

4.5.3 Bootstrap Mode

Resetting the MCU in special bootstrap mode selects a reset vector to a special ROM bootloader program at addresses $BE00–$BFFF. The bootloader program is used to download code, such as programming algorithms, into on-chip RAM through the SCI. To do this:

1. Send a synchronization character (see **Table 4-2**) to the SCI receiver at the specified baud rate.
2. Download up to 768 bytes (1 Kbyte for KS2) of program data, which the CPU places into RAM starting at $0080 and also echoes back on the TxD signal. The bootloader program ends the download after the RAM is full or when the received data line is idle for at least four character times. See **Table 4-2**.

When loading is complete, the MCU jumps to location $0080 and begins executing the code. Interrupt vectors are directed to RAM, which allows the use of interrupts through a jump table. The SCI transmitter requires an external pullup resistor since it is part of port D, which the bootloader configures for wired-OR operation.

LVPI — Low-Voltage Programming Inhibit Bit

LVPI is a read-only bit which always reads as 0. The functionality of this status bit was changed from early versions of the M68HC11K Family. The low-voltage programming inhibit function is disabled on all recent devices.

BYTE — Byte/Other EEPROM Erase Mode Bit

0 = Row or bulk erase mode used
1 = Erase only one byte of EEPROM

ROW — Row/All EEPROM Erase Mode Bit

0 = All 640 bytes of EEPROM erased
1 = Erase only one 16-byte row of EEPROM

NOTE: *ROW is valid only when BYTE = 0.*

The BYTE and ROW bits work together to determine the scope of erasing, as shown in **Table 4-8**.

Table 4-8. Scope of EEPROM Erase

BYTE	ROW	Action
0	0	Bulk erase; all 640 bytes
0	1	Row erase; 16 bytes
1	0	Byte erase
1	1	Byte erase

ERASE — Erase/Normal Control for EEPROM Bit

0 = Normal read or program mode
1 = Erase mode

EELAT — EEPROM Latch Control Bit

0 = EEPROM address and data bus configured for normal reads
1 = EEPROM address and data bus configured for programming or erasing

EEPGM — EEPROM Program Command Bit

0 = Program or erase voltage switched off to EEPROM array
1 = Program or erase voltage switched on to EEPROM array

4.8.2.2 EEPROM Bulk Erase

```
BULKE   LDAB    #$06
        STAB    $003B   Set EELAT and ERASE.
        STAA    $0,X    Store any data to any EEPROM address
        LDAB    #$07
        STAB    $002B   Set EEPGM bit as well
                        to enable EEPROM programming voltage
        JSR     DLY10   Delay 10 ms
        CLR     $003B   Turn off programming voltage and set
                        to READ mode
```

4.8.2.3 EEPROM Row Erase

```
ROWE    LDAB    #$07
        STAB    $003B   Set EELAT, ERASE and ROW.
        STAA    $0,X    Store any data to any EEPROM address
                        in row
        LDAB    #$07
        STAB    $002B   Set EEPGM bit as well
                        to enable EEPROM programming voltage
        JSR     DLY10   Delay 10 ms
        CLR     $003B   Turn off programming voltage and set
                        to READ mode
```

4.8.2.4 EEPROM Byte Erase

```
BYTEE   LDAB    #$16
        STAB    $003B   Set EELAT, ERASE and BYTE.
        STAA    $0,X    Store any data to targeted EEPROM
                        address
        LDAB    #$17
        STAB    $002B   Set EEPGM bit as well
                        to enable EEPROM programming voltage
        JSR     DLY10   Delay 10 ms
        CLR     $003B   Turn off programming voltage and set
                        to READ mode
```

4.8.3 CONFIG Register Programming

The CONFIG register is implemented with EEPROM cells, so EEPROM procedures are required to change it. CONFIG can be programmed or erased (including byte erase) while the MCU is operating in any mode, provided that PTCON in BPROT is clear.

Address: $0035

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BULKP	LVPEN	BPRT4	PTCON	BPRT3	BPRT2	BPRT1	BPRT0
Reset:	1	1	1	1	1	1	1	1

Figure 4-12. Block Protect Register (BPROT)

PTCON — Protect for CONFIG Bit

0 = CONFIG register can be programmed or erased normally.

1 = CONFIG register cannot be programmed or erased.

To change the value in the CONFIG register, complete this procedure. Do not initiate a reset until the procedure is complete.

- Erase the CONFIG register.
- Program the new value to the CONFIG address.
- Initiate reset.

4.8.4 RAM and EEPROM Security

The NOSEC bit in the CONFIG register enables and disables an optional security feature which protects the contents of EEPROM and RAM from unauthorized access. This is done by restricting operation to single-chip modes, preventing the memory locations from being monitored externally. Single-chip modes do not allow visibility of the internal address and data buses. Resident programs, however, have unlimited access to the internal EEPROM and RAM and can read, write, or transfer the contents of these memories.

Three registers are involved in COP operation:

- The CONFIG register contains a bit which determines whether the COP system is enabled or disabled.
- The OPTION register contains two bits which determine the COP timeout period.
- The COPRST register must be written by software to reset the watchdog timer.

NOTE: *Throughout this manual, the registers are discussed by function. In the event that not all bits in a register are referenced, the bits that are not discussed are shaded.*

5.3.3.1 System Configuration Register

In normal modes, COP is enabled out of reset and does not depend on software action. To disable the COP system, set the NOCOP bit in the CONFIG register (see **Figure 5-1**). In special test and bootstrap operating modes, the COP system is initially inhibited by the disable resets (DISR) control bit in the TEST1 register. The DISR bit can subsequently be written to 0 to enable COP resets.

Address: $003F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ROMAD	1	CLKX	PAREN	NOSEC	NOCOP	ROMON	EEON
Reset:	—	1	—	—	1	—	—	—

Figure 5-1. System Configuration Register (CONFIG)

NOTE: *CONFIG is writable once in normal modes and writable at any time in special modes.*

NOCOP — COP System Disable Bit
0 = COP enabled
1 = COP disabled

NOTE: *The slow mode function should not be enabled while using the A/D converter or during an erase/program operation of the EEPROM, unless the internal RC oscillator is turned on.*

The clock monitor function should not be used if the resultant E clock will be slower than 200 kHz.

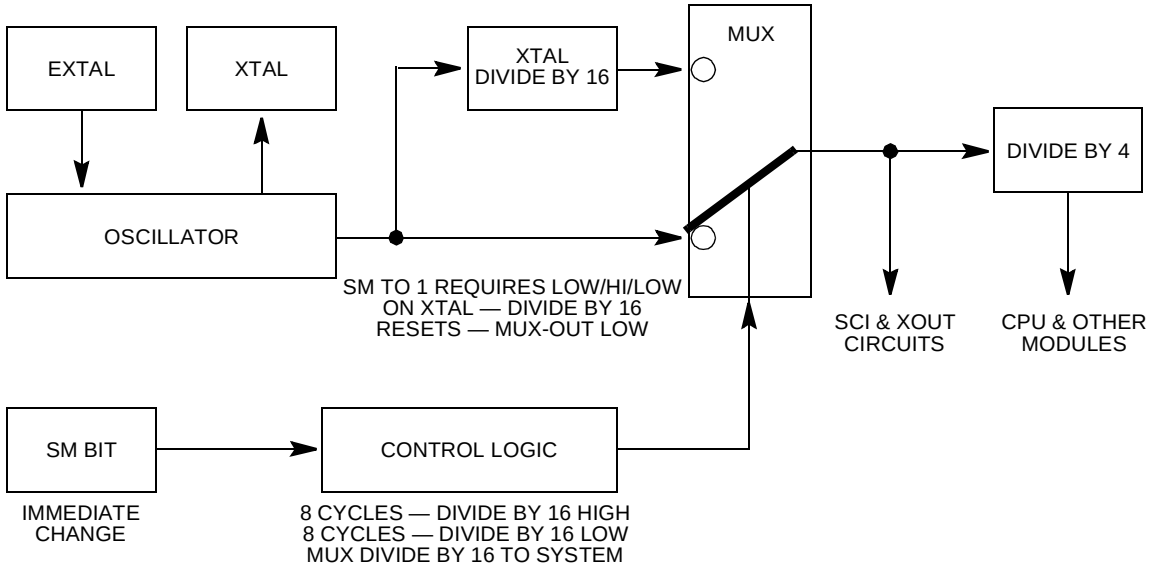


Figure 5-13. Slow Mode Example for M68HC(7)11KS Devices Only

6.11 Internal Pullup Resistors

M68HC11KS series devices contain selectable internal pullup resistors for ports B, F, G, and H. The resistors for each port are enabled by setting the corresponding bit in the PPAR register. PPAR itself must be enabled by setting the PAREN bit in the system configuration register (CONFIG). Refer to **Figure 6-17** and **Figure 6-18**.

Address: $002C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	HPPUE	GPPUE	FPPUE	BPPUE
Write:								
Reset:	0	0	0	0	1	1	1	1

Figure 6-17. Port Pullup Assignment Register (PPAR)

xPPUE — Port x Pin Pullup Enable Bits

Only active when enabled by the PAREN bit in the CONFIG register

0 = Port x pin on-chip pullup devices disabled

1 = Port x pin on-chip pullup devices enabled

NOTE: *FPPUE and BPPUE do not apply in expanded mode because port F and B are address outputs.*

Address: $003F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	ROMAD	1	CLKX	PAREN	NOSEC	NOCOP	ROMON	EEON
Write:								
Reset:	—	1	—	—	1	—	—	—

Figure 6-18. System Configuration Register (CONFIG)

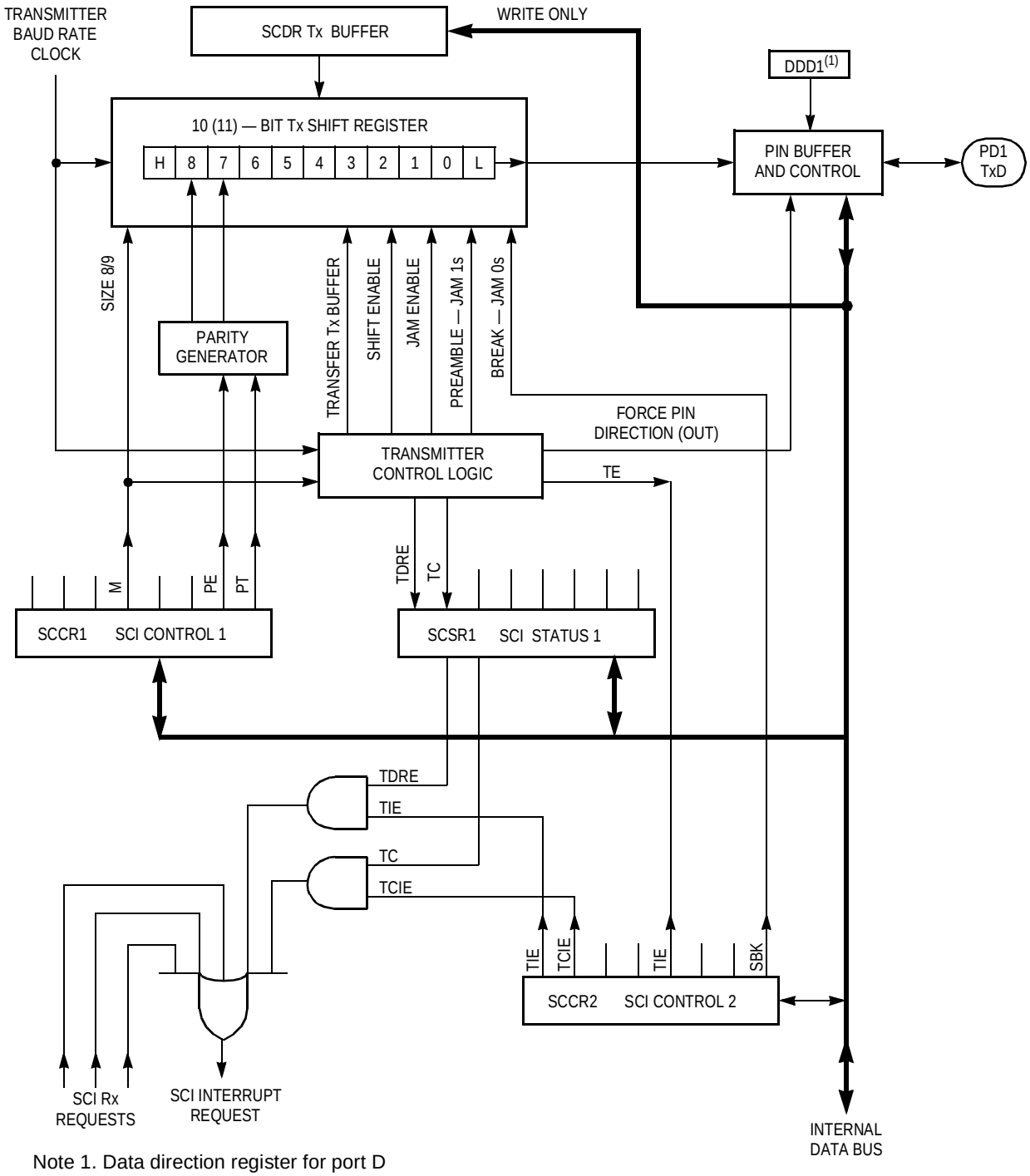
NOTE: *CONFIG is writable once in normal modes and writable at any time in special modes.*

PAREN — Pullup Assignment Register Enable Bit

0 = PPAR register disabled

1 = PPAR register enabled; pullups can be enabled through PPAR

Figure 7-2 is a block diagram of the SCI transmitter.



Note 1. Data direction register for port D

Figure 7-2. SCI Transmitter Block Diagram

7.9.2 Serial Communications Control Register 1

Address $0072

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	LOOPS	WOMS	0	M	WAKE	ILT	PE	PT
Reset:	U	U	0	0	0	0	0	0

U = Undefined

Figure 7-7. SCI Control Register 1 (SCCR1)

LOOPS — SCI Loop Mode Enable Bit

Both the transmitter and receiver must be enabled to use the loop mode. When the loop mode is enabled, the TxD pin is driven high (idle line state) if the transmitter is enabled.

0 = SCI transmit and receive operate normally.
1 = SCI transmit and receive are disconnected from TxD and RxD pins, and transmitter output is fed back into the receiver input.

WOMS — Wired-OR Mode for SCI Pins PD[1:0] Bits

See also **8.6.1 Serial Peripheral Control Register** for a description of the DWOM (port D wired-OR mode) bit in the serial peripheral control register (SPCR).

0 = TxD and RxD operate normally.
1 = TxD and RxD are open drains if operating as outputs.

M — Mode (SCI Word Size) Bit

0 = Start bit, 8 data bits, 1 stop bit
1 = Start bit, 9 data bits, 1 stop bit

WAKE — Wakeup Mode Bit

0 = Wake up by idle line recognition
1 = Wake up by address mark (most significant data bit set)

ILT — Idle Line Type Bit

0 = Short (SCI counts consecutive 1s after start bit.)
1 = Long (SCI counts one only after stop bit.)

NOTE: *Throughout this manual, the registers are discussed by function. In the event that not all bits in a register are referenced, the bits that are not discussed are shaded.*

8.6.1 Serial Peripheral Control Register

Address: $0028

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR2
Reset:	0	0	0	0	0	1	U	U

U = Undefined

Figure 8-3. Serial Peripheral Control Register (SPCR)

SPIE — Serial Peripheral Interrupt Enable Bit

0 = SPI interrupt disabled

1 = SPI interrupt is enabled each time the SPIF or MODF status flag in SPSR is set.

SPE — Serial Peripheral System Enable Bit

0 = SPI off

1 = SPI on — PD[5:2] function as SPI signals

DWOM — Port D Wired-OR Mode Bit

DWOM affects only the four SPI pins on port D, PD[5:2]. See also **7.9.2 Serial Communications Control Register 1** for a discussion of the WOMS (wired-OR Mode for SCI pins) bit in the serial communications control register 1 (SCCR1).

0 = Normal CMOS outputs

1 = Open-drain outputs

MSTR — Master Mode Select Bit

0 = Slave mode

1 = Master mode

The three clocks are derived from the E clock by writing to registers which determine their scaling factors. The clock A frequency is equal to E divided by 1, 2, 4, or 8, depending on which bits (PCKA[2:1]) in the PWCLK register are set. The clock B frequency is equal to the E clock divided by a power of two determined by bits PCKB[3:1] in the PWCLK register. Clock S is derived by dividing clock A by the integer (1 to 256) stored in the PWSCAL register, then by two.

Two channels can be concatenated by setting the appropriate bit (CON34 or CON12) in the PWCLK register. In this mode, the clock source is determined by the low-order channel, which is channel two in CON12 and channel four in CON34. The output is also placed on the pin associated with the low-order channels, so when two channels are concatenated the pin associated with the high-order channel (PH0 and/or PH2) can be used for GPIO. A read of the high-order byte causes the low-order byte to be latched for one cycle to guarantee that double-byte reads are accurate. A write to the low-order byte of the counter causes reset of the entire counter. A write to the high-order byte of the counter has no effect.

9.9.2 Pulse-Width Modulation Control Registers

The PWM control registers are described here.

9.9.2.1 Pulse-Width Modulation Timer Clock Select Register

Address: $0060

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	CON34	CON12	PCKA2	PCKA1	0	PCKB3	PCKB2	PCKB1
Reset:	0	0	0	0	0	0	0	0

Figure 9-31. Pulse-Width Modulation Timer Clock Select (PWCLK)

9.9.2.4 Pulse-Width Modulation Timer Enable Register

Address: $0063

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TPWSL	DISCP	0	0	PWEN4	PWEN3	PWEN2	PWEN1
Reset:	0	0	0	0	0	0	0	0

Figure 9-34. Pulse-Width Modulation Timer Enable Register (PWEN)

TPWSL — PWM Scaled Clock Test Bit — factory use only; only accessible in special test mode

0 = Normal operation

1 = Clock S is output to PWSCAL register (test only)

DISCP — Disable Compare Scaled E-Clock Bit — factory use only; only accessible in special test mode

0 = Normal operation

1 = Match of period does not reset associated count register (test only)

PWEN[4:1] — Pulse-Width Enable for Channels [4:1] Bits

0 = Channel disabled

1 = Channel enabled at port H bits [3:0]

Address: $0039

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ADPU	CSEL	IRQE	DLY(1)	CME	FCME	CR1	CR0
Reset:	0	0	0	1	0	0	0	0

1. DLY can be written only once in the first 64 cycles out of reset in normal modes or at any time in special modes.

Figure 10-3. System Configuration Options Register (OPTION)

ADPU — A/D Power-up
0 = A/D powered down
1 = A/D powered up

CSEL — Clock Select
0 = A/D and EEPROM use system E clock.
1 = A/D and EEPROM use internal RC clock.

10.4.2 A/D Control/Status Register

All bits in this register can be read or written except bit 7, which is a read-only status indicator, and bit 6, which always reads as 0. Writing to ADCTL initiates a conversion, aborting any conversion in progress.

Address: $0030

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CCF		SCAN	MULT	CD	CC	CB	CA
Write:								
Reset:	0	0	U	U	U	U	U	U

= Unimplemented U = Unaffected by reset

Figure 10-4. Analog-to-Digital Control/Status Register (ADCTL)

11.3 Memory Expansion

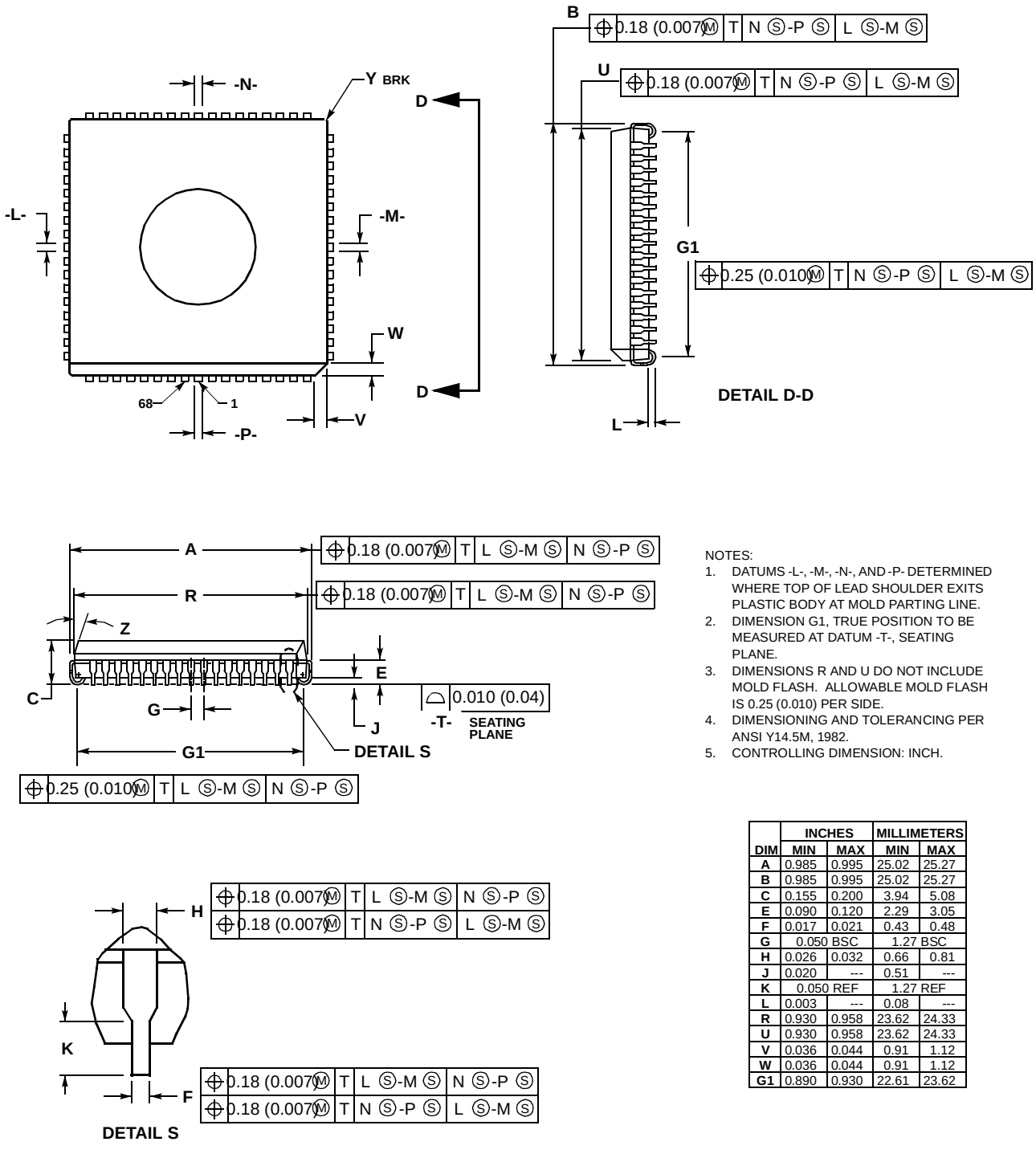
The M68HC11K Family devices employ a register-based paging scheme to extend their address range beyond the physical 64-Kbyte limit of the 16 CPU address lines. Pages are selected using the expansion address lines XA[18:13] available on port G. This selection can be facilitated by the chip-select lines on port H, discussed in **11.4 Chip Selects**. The M68HC11KS devices do not provide these features since they lack the required port G and port H lines. Refer to **Figure 1-2. M68HC11KS Family Block Diagram**.

11.3.1 Memory Size and Address Line Allocation

To access expanded memory, the user first allocates portion(s) of the 64 Kbyte address space, or window(s), through which the CPU will view external memory. One or two windows can be designated, and the size of each window can be 0 (disabled), 8, 16, or 32 Kbytes.

Expanded memory is addressed with a combination of the CPU's normal address lines ADDR[15:0] and the expansion address lines XA[18:13]. The expansion address lines select a memory bank, and the CPU's normal address lines select a particular location within the bank. The size of the window(s) and the number of memory banks determine exactly which expansion address lines are used. The port G assignment register (PGAR) controls which port G pins function as expanded address lines. Any port G pins not allocated for memory expansion can serve as general-purpose input/output (GPIO). When a configuration uses any of the lower three expansion address lines XA[15:13] they replace the CPU's equivalent address lines (ADDR[15:13]). **Table 11-1** shows how address and expansion lines are allocated for various combinations of memory banks and window size.

13.8 68-Pin J-Cerquad (Case 779A)



NOTES:
1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.985	0.995	25.02	25.27
B	0.985	0.995	25.02	25.27
C	0.155	0.200	3.94	5.08
E	0.090	0.120	2.29	3.05
F	0.017	0.021	0.43	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.050 REF		1.27 REF	
L	0.003	---	0.08	---
R	0.930	0.958	23.62	24.33
U	0.930	0.958	23.62	24.33
V	0.036	0.044	0.91	1.12
W	0.036	0.044	0.91	1.12
G1	0.890	0.930	22.61	23.62

Ordering Information