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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	4MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	37
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	640 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.29x29.29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc11k1cfne4

Section 5. Resets and Interrupts

List of Figures

Table 3-1. Instruction Set (Sheet 6 of 7)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
SBA	Subtract B from A	A – B ⇒ A	INH	10	—	2	—	—	—	—	Δ	Δ	Δ	Δ
SBCA (opr)	Subtract with Carry from A	A – M – C ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	82 92 B2 A2 18 A2	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	Δ	Δ
SBCB (opr)	Subtract with Carry from B	B – M – C ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	C2 D2 F2 E2 18 E2	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	Δ	Δ
SEC	Set Carry	1 ⇒ C	INH	0D	—	2	—	—	—	—	—	—	—	1
SEI	Set Interrupt Mask	1 ⇒ I	INH	0F	—	2	—	—	—	1	—	—	—	—
SEV	Set Overflow Flag	1 ⇒ V	INH	0B	—	2	—	—	—	—	—	—	1	—
STAA (opr)	Store Accumulator A	A ⇒ M	A DIR A EXT A IND,X A IND,Y	97 B7 A7 18 A7	dd hh ll ff ff	3 4 4 5	—	—	—	—	Δ	Δ	0	—
STAB (opr)	Store Accumulator B	B ⇒ M	B DIR B EXT B IND,X B IND,Y	D7 F7 E7 18 E7	dd hh ll ff ff	3 4 4 5	—	—	—	—	Δ	Δ	0	—
STD (opr)	Store Accumulator D	A ⇒ M, B ⇒ M + 1	DIR EXT IND,X IND,Y	DD FD ED 18 ED	dd hh ll ff ff	4 5 5 6	—	—	—	—	Δ	Δ	0	—
STOP	Stop Internal Clocks	—	INH	CF	—	2	—	—	—	—	—	—	—	—
STS (opr)	Store Stack Pointer	SP ⇒ M : M + 1	DIR EXT IND,X IND,Y	9F BF AF 18 AF	dd hh ll ff ff	4 5 5 6	—	—	—	—	Δ	Δ	0	—
STX (opr)	Store Index Register X	IX ⇒ M : M + 1	DIR EXT IND,X IND,Y	DF FF EF CD EF	dd hh ll ff ff	4 5 5 6	—	—	—	—	Δ	Δ	0	—
STY (opr)	Store Index Register Y	IY ⇒ M : M + 1	DIR EXT IND,X IND,Y	18 DF 18 FF 1A EF 18 EF	dd hh ll ff ff	5 6 6 6	—	—	—	—	Δ	Δ	0	—
SUBA (opr)	Subtract Memory from A	A – M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	80 90 B0 A0 18 A0	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	Δ	Δ
SUBB (opr)	Subtract Memory from B	B – M ⇒ B	A IMM A DIR A EXT A IND,X A IND,Y	C0 D0 F0 E0 18 E0	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	Δ	Δ
SUBD (opr)	Subtract Memory from D	D – M : M + 1 ⇒ D	IMM DIR EXT IND,X IND,Y	83 93 B3 A3 18 A3	jj kk dd hh ll ff ff	4 5 6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
SWI	Software Interrupt	See **Figure 3-2**	INH	3F	—	14	—	—	—	1	—	—	—	—
TAB	Transfer A to B	A ⇒ B	INH	16	—	2	—	—	—	—	Δ	Δ	0	—
TAP	Transfer A to CC Register	A ⇒ CCR	INH	06	—	2	Δ	↓	Δ	Δ	Δ	Δ	Δ	Δ
TBA	Transfer B to A	B ⇒ A	INH	17	—	2	—	—	—	—	Δ	Δ	0	—
TEST	TEST (Only in Test Modes)	Address Bus Counts	INH	00	—	*	—	—	—	—	—	—	—	—

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0058	Memory Mapping Window 1 Control Register (MM1CR)(1) See page 237.	Read: Write:	0	X1A18	X1A17	X1A16	X1A15	X1A14	X1A13	0
		Reset:	0	0	0	0	0	0	0	0
$0059	Memory Mapping Window 2 Control Register (MM2CR)(1) See page 237.	Read: Write:	0	X2A18	X2A17	X2A16	X2A15	X2A14	X2A13	0
		Reset:	0	0	0	0	0	0	0	0
$005A	Chip Select Clock Stretch Register (CSCSTR)(1) See page 249.	Read: Write:	IOSA	IOSB	GP1SA	GP1SB	GP2SA	GP2SB	PCSA	PCSB
		Reset:	0	0	0	0	0	0	0	0
$005B	Chip Select Control Register (CSCTL)(1) See pages 240, 241	Read: Write:	IOEN	IOPL	IOCSA	IOSZ	GCSPR	PCSEN	PCSZA	PCSZB
		Reset:	0	0	0	0	0	1	0	0
$005C	General-Purpose Chip Select 1 Address Register (GPCS1A)(1) See page 243.	Read: Write:	G1A18	G1A17	G1A16	G1A15	G1A14	G1A13	G1A12	G1A11
		Reset:	0	0	0	0	0	0	0	0
$005D	General-Purpose Chip Select 1 Control Register (GPCS1C)(1) See pages 244, 247	Read: Write:	G1DG2	G1DPC	G1POL	G1AV	G1SZA	G1SZB	G1SZC	G1SZD
		Reset:	0	0	0	0	0	0	0	0
$005E	General-Purpose Chip Select 2 Address Register (GPCS2A)(1) See page 245.	Read: Write:	G2A18	G2A17	G2A16	G2A15	G2A14	G2A13	G2A12	G2A11
		Reset:	0	0	0	0	0	0	0	0
$005F	General-Purpose Chip Select 2 Control Register (GPCS2C)(1) See pages 245, 247	Read: Write:	0	G2DPC	G2POL	G2AV	G2SZA	G2SZB	G2SZC	G2SZD
		Reset:	0	0	0	0	0	0	0	0
$0060	Pulse Width Modulation Timer Clock Select Register (PWCLK) See page 213.	Read: Write:	CON34	CON12	PCKA2	PCKA1	0	PCKB3	PCKB2	PCKB1
		Reset:	0	0	0	0	0	0	0	0
$0061	Pulse Width Modulation Timer Polarity Register (PWPOL) See page 215.	Read: Write:	PCLK4	PCLK3	PCLK2	PCLK1	PPOL4	PPOL3	PPOL2	PPOL1
		Reset:	0	0	0	0	0	0	0	0

1. Not available on M68HC11KS devices

= Unimplemented R = Reserved U = Undefined

Figure 4-1. Register and Control Bit Assignments (Sheet 8 of 11)

4.6.1 Control Registers and RAM

Out of reset, the 128-byte register block is mapped to $0000 and the 768-byte RAM (1 Kbyte on the [7]11KS2) is mapped to $0080. Both the register block and the RAM can be placed at any other 4-Kbyte boundary ($x000 and $x080, respectively) by writing the appropriate value to the INIT register.

Address: $003D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0
Reset:	0	0	0	0	0	0	0	0

Figure 4-5. RAM and I/O Mapping Register (INIT)

NOTE: *INIT is writable once in normal modes and writable at any time in special modes.*

RAM[3:0] — RAM Map Position Bits

These four bits determine the position of RAM in the memory map by specifying the upper hexadecimal digit of the RAM address. Refer to **Table 4-5**.

REG[3:0] — Register Block Position Bits

These four bits determine the position of the register block in memory by specifying the upper hexadecimal digit of the block address. Refer to **Table 4-6**.

registers to default values, then receives data from an external host and programs it into the EPROM. The value in the X index register determines programming delay time. The value in the Y index register is a pointer to the first address in EPROM to be programmed. The default starting address is $8000 for the M68HC11KS2.

When the utility program is ready to receive programming data, it sends the host a $FF character and waits for a reply. When the host sees the $FF character, it sends the EPROM programming data, starting with the first location in the EPROM array. After the MCU receives the last byte to be programmed and returns the corresponding verification data, it terminates the programming operation by initiating a reset. Refer to the Motorola application note entitled *MC68HC11 Bootstrap Mode,* document order number AN1060/D.

4.7.2 Programming the EPROM from Memory

In this method, software programs the EPROM one byte at a time. Each byte is read from memory, then latched and programmed into the EPROM using the EPROM programming control register (EPROG). This procedure can be done in any operating mode.

Address: $002B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	R	0	ELAT	EXCOL	EXROW	0	0	EPGM
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 4-8. EPROM Programming Control Register (EPROG)

MBE — Multiple-Byte Program Enable Bit

MBE is for factory use only and is accessible only in special test mode. When MBE is set, the MCU ignores address bit 5, so that bytes with ADDR5 = 0 and ADDR5 = 1 both get programmed with the same data.

0 = Normal programming
1 = Multiple-byte programming enabled

5.3.4.1 System Configuration Options Register

The clock monitor function is enabled or disabled by the CME control bit in the OPTION register (see **Figure 5-4**). The FCME bit in OPTION overrides CME and enables the clock monitor until the next reset.

Address: $0030

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ADPU	CSEL	IRQE	DLY	CME	FCME	CR1	CR0
Reset:	0	0	0	1	0	0	0	0

Figure 5-4. System Configuration Options Register (OPTION)

NOTE: *In normal operating modes, these bits can be written only once within 64 bus cycles after reset.*

CME — Clock Monitor Enable Bit

This control bit can be read or written at any time and controls whether or not the internal clock monitor circuit triggers a reset sequence when the system clock is slow or absent. When it is clear, the clock monitor circuit is disabled. When it is set, the clock monitor circuit is enabled. Reset clears the CME bit.

0 = Clock monitor disabled
1 = Clock monitor enabled

FCME — Force Clock Monitor Enable Bit

0 = Clock monitor follows the state of the CME bit.
1 = Clock monitor is enabled until the next reset.

Semiconductor wafer processing causes variations of the RC timeout values between individual devices. An E-clock frequency below 10 kHz generates a clock monitor error. An E-clock frequency of 200 kHz or more prevents clock monitor errors. Using the clock monitor function when the E clock is below 200 kHz is not recommended.

7.9.2 Serial Communications Control Register 1

Address $0072

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	LOOPS	WOMS	0	M	WAKE	ILT	PE	PT
Reset:	U	U	0	0	0	0	0	0

U = Undefined

Figure 7-7. SCI Control Register 1 (SCCR1)

LOOPS — SCI Loop Mode Enable Bit

Both the transmitter and receiver must be enabled to use the loop mode. When the loop mode is enabled, the TxD pin is driven high (idle line state) if the transmitter is enabled.

0 = SCI transmit and receive operate normally.
1 = SCI transmit and receive are disconnected from TxD and RxD pins, and transmitter output is fed back into the receiver input.

WOMS — Wired-OR Mode for SCI Pins PD[1:0] Bits

See also **8.6.1 Serial Peripheral Control Register** for a description of the DWOM (port D wired-OR mode) bit in the serial peripheral control register (SPCR).

0 = TxD and RxD operate normally.
1 = TxD and RxD are open drains if operating as outputs.

M — Mode (SCI Word Size) Bit

0 = Start bit, 8 data bits, 1 stop bit
1 = Start bit, 9 data bits, 1 stop bit

WAKE — Wakeup Mode Bit

0 = Wake up by idle line recognition
1 = Wake up by address mark (most significant data bit set)

ILT — Idle Line Type Bit

0 = Short (SCI counts consecutive 1s after start bit.)
1 = Long (SCI counts one only after stop bit.)

TE — Transmitter Enable Bit

When TE goes from 0 to 1, one unit of idle character time (logic 1) is queued as a preamble.

0 = Transmitter disabled
1 = Transmitter enabled

RE — Receiver Enable Bit

0 = Receiver disabled
1 = Receiver enabled

RWU — Receiver Wakeup Control

0 = Normal SCI receiver operation
1 = Wakeup is enabled and receiver interrupts are inhibited.

SBK — Send Break Bit

At least one character time of break is queued and sent each time SBK is written to 1. Multiple breaks may be sent if the transmitter is idle at the time the SBK bit is toggled on and off, as the baud rate clock edge could occur between writing the 1 and writing the 0 to SBK.

0 = Break generator off
1 = Break codes generated as long as SBK = 1

7.9.4 Serial Communication Status Register 1

The SCSR provides flags for various SCI conditions which can be polled or used to generate SCI system interrupts. To clear any set flag, read SCSR while the flag is set and then write to SCDR.

Address $0074

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
Reset:	1	1	0	0	0	0	0	0

Figure 7-9. SCI Status Register 1 (SCSR1)

	Bit 7	6	5	4	3	2	1	Bit 0
Address:	$001A— TOC3 (High)							
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1
Address:	$001B — TOC3 (Low)							
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1
Address:	$001C— TOC4 (High)							
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1
Address:	$001D — TOC4 (Low)							
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1

Figure 9-13. Timer Output Compare Registers (TOC1–TOC4) (Continued)

All output compare registers are 16-bit read-write. Any of these registers can be used as a storage location if it is not used for output compare or input capture.

9.8.3 Pulse Accumulator Control Register

Address: $0026

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	PAEN	PAMOD	PEDGE	0	I4/O5	RTR1	RTR0
Reset:	0	0	0	0	0	0	0	0

Figure 9-29. Pulse Accumulator Control Register (PACTL)

RTR[1:0] — Real-Time Interrupt Rate Select Bits

These two bits select a divisor (1, 2, 4, or 8) for the $E \div 2^{13}$ RTI clock. Refer to **Table 9-7**.

Table 9-7. Real-Time Interrupt Rate versus RTR[1:0]

RTR[1:0]	Rate	XTAL = 12.0 MHz	XTAL = 2^{23}	XTAL = 8.0 MHz	XTAL = 4.9152 MHz	XTAL = 4.0 MHz	XTAL = 3.6864 MHz
0 0	$2^{13} \div E$	2.730 ms	3.91 ms	4.10 ms	6.67 ms	8.19 ms	8.89 ms
0 1	$2^{14} \div E$	5.461 ms	7.81 ms	8.19 ms	13.33 ms	16.38 ms	17.78 ms
1 0	$2^{15} \div E$	10.92 ms	15.62 ms	16.38 ms	26.67 ms	32.77 ms	35.56 ms
1 1	$2^{16} \div E$	21.84 ms	31.25 ms	32.77 ms	53.33 ms	65.54 ms	71.11 ms
	E =	**3.0 MHz**	**2.1 MHz**	**2.0 MHz**	**1.2288 MHz**	**1.0 MHz**	**921.6 kHz**

9.9 Pulse-Width Modulator (PWM)

Four 8-bit pulse-width modulation channels are available in the M68HC11K Family devices. They are output on port H pins 3–0. Pairs of channels can be concatenated to produce 16-bit outputs. Three programmable clocks and a flexible clock selection scheme provide a wide range of frequencies.

The 8-bit mode with E = 4 MHz can produce waveforms from 40 kHz at 1 percent duty cycle resolution to less than 10 Hz at 0.4 percent duty cycle resolution. In 16-bit mode, a duty cycle resolution down to 15 parts per million can be achieved (at a frequency of 60 Hz). At 1 kHz, the duty cycle resolution is 250 ppm.

9.9.1 PWM System Description

Figure 9-30 shows a block diagram of the PWM system. Each of four channels is enabled by bit PWENx in the PWEN register. Each channel has an 8-bit counter (PWCNTx), a period register (PWPERx), and a duty cycle register (PWDTYx). The counter is driven by one of three user-scaled clock sources — clock A, B, or S — selected by the pulse-width channel select (PCLKx) bit in the pulse-width modulation timer polarity (PWPOL) register.

A pulse-width modulation period begins when the counter matches the value stored in the period register. When this happens, a logic value determined by the polarity bit (PPOLx) in the PWPOL register is driven on the associated port H output pin, and the counter is reset to 0. When the counter matches the number stored in the duty cycle register, the output reverses polarity. The period and duty cycle registers are double buffered so they can be changed without disturbing the current waveform. A new period or duty cycle can be forced by writing to the period (PWPERx) or duty cycle register (PWDTYx) and then to the counter (PWCNTx). Writing to the counter always resets it to 0.

10.3 Functional Description

The A/D converter system consists of four functional blocks as shown in **Figure 10-1**:

- Multiplexer
- Analog converter
- Result storage
- Digital control

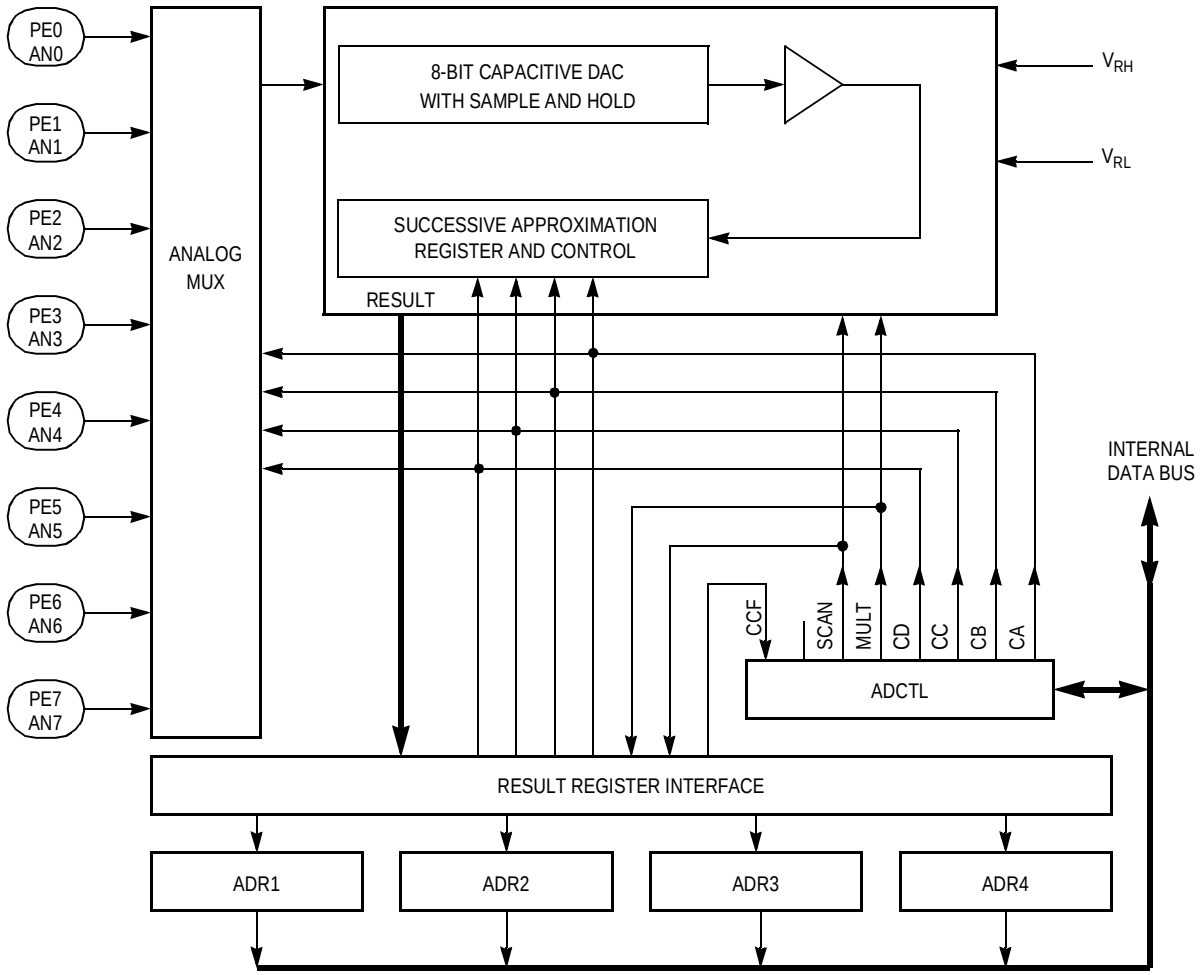


Figure 10-1. A/D Converter Block Diagram

Address: $0039

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ADPU	CSEL	IRQE	DLY(1)	CME	FCME	CR1	CR0
Reset:	0	0	0	1	0	0	0	0

1. DLY can be written only once in the first 64 cycles out of reset in normal modes or at any time in special modes.

Figure 10-3. System Configuration Options Register (OPTION)

ADPU — A/D Power-up
0 = A/D powered down
1 = A/D powered up

CSEL — Clock Select
0 = A/D and EEPROM use system E clock.
1 = A/D and EEPROM use internal RC clock.

10.4.2 A/D Control/Status Register

All bits in this register can be read or written except bit 7, which is a read-only status indicator, and bit 6, which always reads as 0. Writing to ADCTL initiates a conversion, aborting any conversion in progress.

Address: $0030

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CCF		SCAN	MULT	CD	CC	CB	CA
Write:								
Reset:	0	0	U	U	U	U	U	U

= Unimplemented U = Unaffected by reset

Figure 10-4. Analog-to-Digital Control/Status Register (ADCTL)

Section 11. Memory Expansion and Chip Selects

11.1 Contents

11.2 Introduction

This section provides descriptions of the expanded memory and the chip selects.

12.4 Functional Operating Range

Rating	Symbol	Value	Unit
Operating temperature range MC68HC(7)11KC MC68HC(7)11KV MC68HC(7)11KM	T_A	T_L to T_H –40 to +85 –40 to +105 –40 to +125	°C
Operating voltage range	V_{DD}	5.0 ± 10%	V

12.5 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Average junction temperature	T_J	$T_A + (P_D \times \Theta_{JA})$	°C
Ambient temperature	T_A	User-determined	°C
Package thermal resistance (junction-to-ambient) 80-pin low-profile quad flat pack 68-pin plastic leaded chip carrier 68-pin windowed ceramic cerquad (EPROM) 84-pin plastic leaded chip carrier 80-pin quad flat pack 84-pin J-cerquad	Θ_{JA}	 80 50 60 50 85 50	°C/W
Total power dissipation(1)	P_D	$P_{INT} + P_{I/O}$ $K / T_J + 273$ °C	W
Device internal power dissipation	P_{INT}	$I_{DD} \times V_{DD}$	W
I/O pin power dissipation(2)	$P_{I/O}$	User-determined	W
A constant(3)	K	$P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2$	W/°C

1. This is an approximate value, neglecting $P_{I/O}$.
2. For most applications, $P_{I/O} \leq P_{INT}$ and can be neglected.
3. K is a constant pertaining to the device. Solve for K with a known T_A and a measured P_D (at equilibrium). Use this value of K to solve for P_D and T_J iteratively for any value of T_A.

12.11 Expansion Bus Timing

Num	Characteristic[1]	Symbol	2.0 MHz		3.0 MHz		4.0 MHz		Unit
			Min	Max	Min	Max	Min	Max	
	Frequency of operation (E clock)[2]	f_o	dc	2.0	dc	3.0	dc	4.0	MHz
1	Cycle time, $t_{cyc} = 1/f_o$	t_{cyc}	500	—	333	—	250	—	ns
2	Pulse width, E low, $PW_{EL} = 1/2\ t_{cyc} - 20$ ns	PW_{EL}	230	—	147	—	105	—	ns
3	Pulse width, E high[3] $PW_{EH} = 1/2\ t_{cyc} - 25$ ns	PW_{EH}	225	—	142	—	100	—	ns
4A 4B	E clock Rise time Fall time	 t_r t_f	 — —	 20 20	 — —	 20 18	 — —	 20 15	ns
9	Address hold time, $t_{AH} = 1/8\ t_{cyc} - 10$ ns	t_{AH}	53	—	32	—	21	—	ns
11	Address delay time, $t_{AD} = 1/8\ t_{cyc} + 40$ ns	t_{AD}	—	103	—	82	—	71	ns
12	Address valid time to E rise $t_{AV} = PW_{EL} - t_{AD}$	t_{AV}	128	—	65	—	34	—	ns
17	Read data setup time	t_{DSR}	30	—	30	—	20	—	ns
18	Read data hold time	t_{DHR}	0	—	0	—	0	—	ns
19	Write data delay time	t_{DDW}	—	40	—	40	—	40	ns
21	Write data hold time, $t_{DHW} = 1/8\ t_{cyc}$	t_{DHW}	63	—	42	—	31	—	ns
29	MPU address access time[3] $t_{ACCA} = t_{cyc} - t_f - t_{DSR} - t_{AD}$	t_{ACCA}	348	—	203	—	144	—	ns
39	Write data setup time[3] $t_{DSW} = PW_{EH} - t_{DDW}$	t_{DSW}	185	—	102	—	60	—	ns
50	E valid chip-select delay time	t_{ECSD}	—	40	—	40	—	40	ns
51	E valid chip-select access time[3] $t_{ECSA} = PW_{EH} - t_{ECSD} - t_{DSR}$	t_{ECSA}	155	—	72	—	40	—	ns
52	Chip select hold time	t_{CH}	0	20	0	20	0	20	ns
54	Address valid chip-select delay time $t_{ACSD} = 1/4\ t_{cyc} + 40$ ns	t_{ACSD}	—	165	—	123	—	103	ns
55	Address valid chip-select access time $t_{ACSA} = t_{cyc} - t_f - t_{DSR} - t_{ACSD}$[3]	t_{ACSA}	285	—	162	—	113	—	ns
56	Address valid to chip-select time	t_{AVCS}	10	—	10	—	10	—	ns
57	Address valid to data three-state time	t_{AVDZ}	—	10	—	10	—	10	ns

1. $V_{DD} = 5.0 \pm 10\%$, $V_{SS} = 0$ Vdc, $T_A = T_L$ to T_H, unless otherwise noted
   All timing measurements refer to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Input clocks with duty cycles other than 50% affect bus performance.
3. This parameter is affected by clock stretching. Add n(t_{cyc}) to parameter value, where n = 1, 2, or 3 depending on values written to CSCSTR register or n = 1 for STRCH = 1 on KS parts.

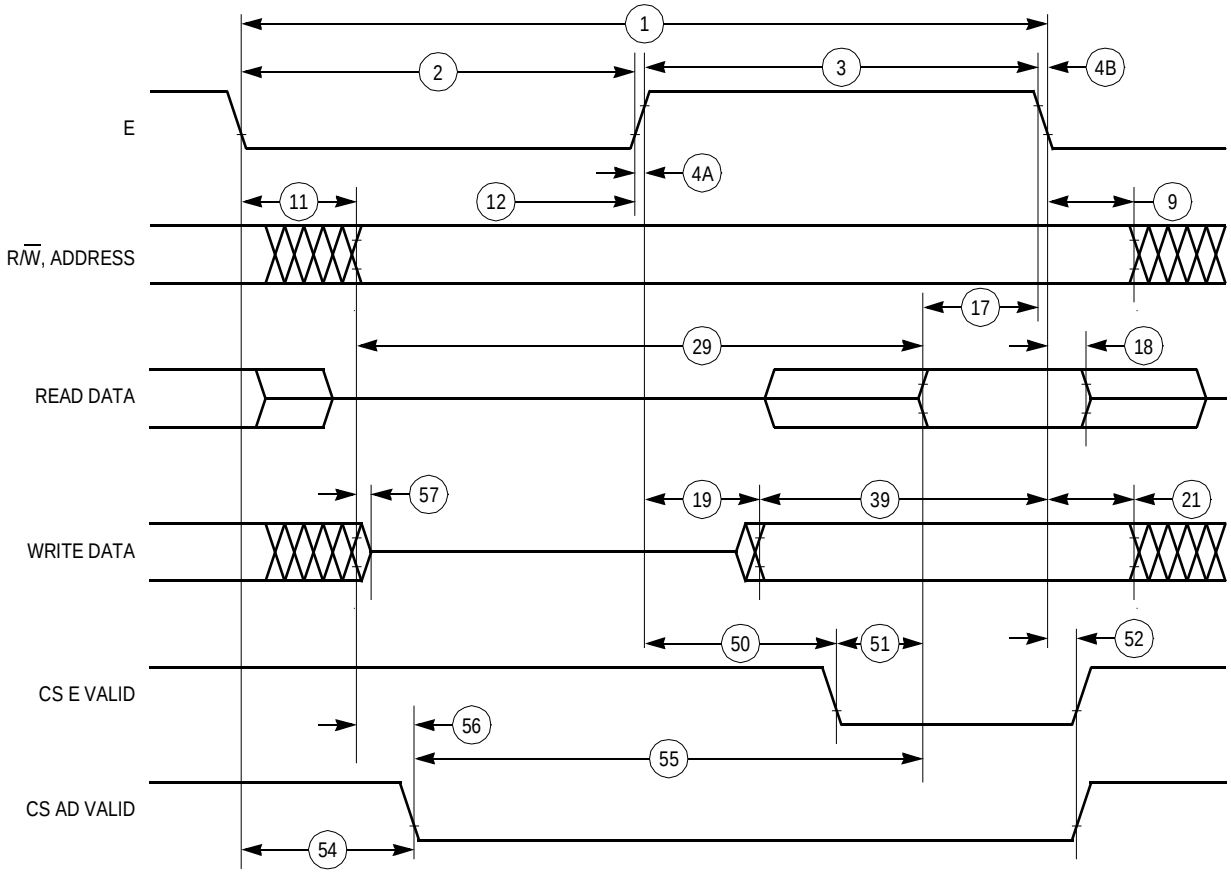
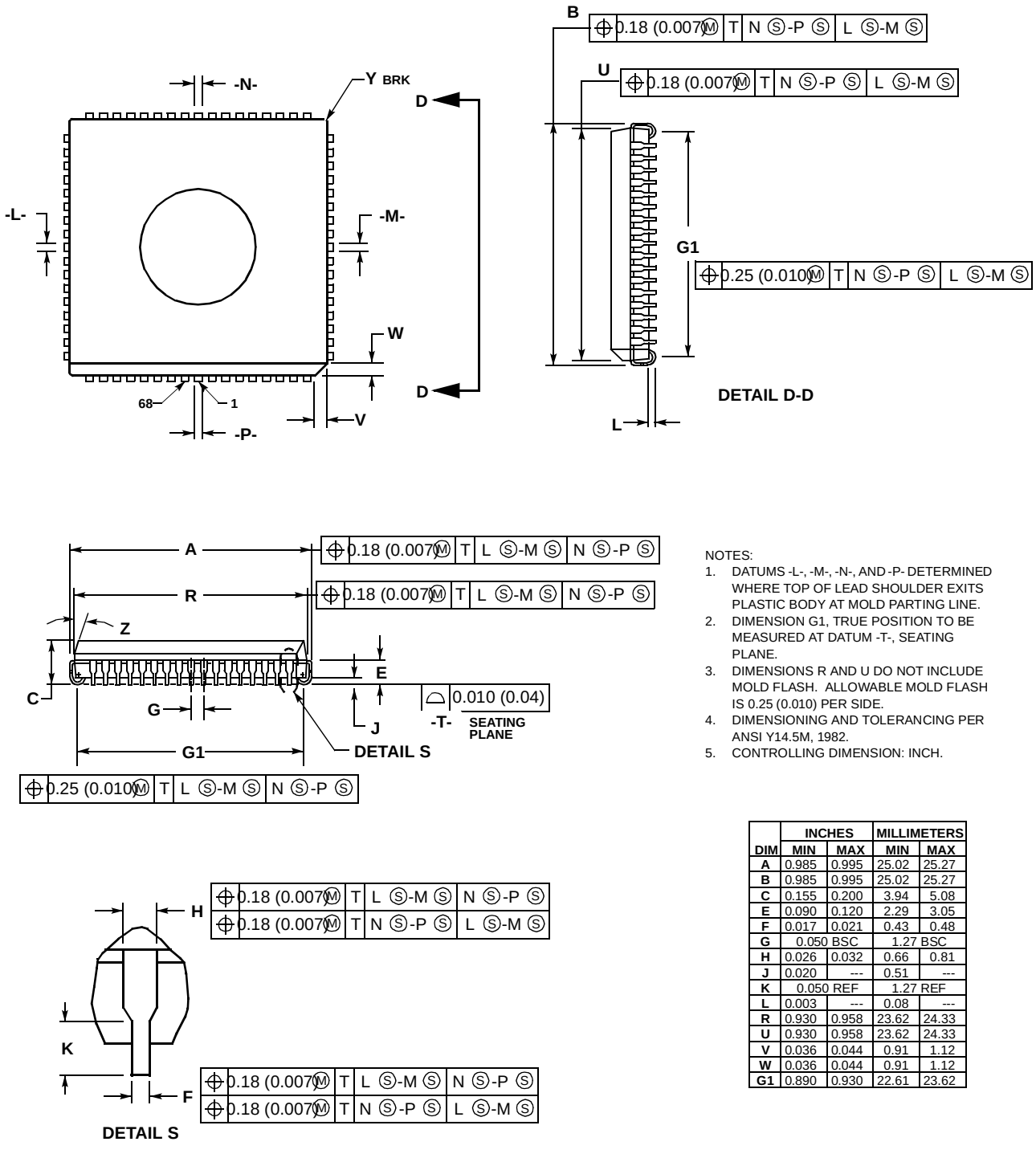


Figure 12-9. Expansion Bus Timing

13.8 68-Pin J-Cerquad (Case 779A)



NOTES:
1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.985	0.995	25.02	25.27
B	0.985	0.995	25.02	25.27
C	0.155	0.200	3.94	5.08
E	0.090	0.120	2.29	3.05
F	0.017	0.021	0.43	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.050 REF		1.27 REF	
L	0.003	---	0.08	---
R	0.930	0.958	23.62	24.33
U	0.930	0.958	23.62	24.33
V	0.036	0.044	0.91	1.12
W	0.036	0.044	0.91	1.12
G1	0.890	0.930	22.61	23.62

Section 14. Ordering Information

Use Table 14-1 to determine part numbers when placing an order.

Table 14-1. M68HC11K Family Devices

Device Number	ROM or EPROM	RAM	EEPROM	I/O	Chip Select	Slow Mode	Packages
MC68HC(L)11K0 MC68HC(L)11K1 MC68HC(L)11K4	0 0 24 K	768 768 768	0 640 640	37 37 62	Yes Yes Yes	No No No	84-pin PLCC(1) 80-pin QFP(2)
MC68HC711K4	24 K	768	640	62	Yes	No	84-pin J-cerquad(3) 84-pin PLCC 80-pin QFP
MC68HC11KS2	32 K	1 K	640	51	No	Yes	68-pin PLCC 80-pin LQFP(4)
MC68HC711KS2	32 K	1 K	640	51	No	Yes	68-pin PLCC 80-pin LQFP 68-pin J-cerquad

1. PLCC = Plastic leaded chip carrier
2. QFP = Quad flat pack
3. J-cerquad = Ceramic windowed version of PLCC
4. LQFP = Low-profile quad flat pack