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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	3MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	37
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	640 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc11k1cfue3

Section 3. Central Processor Unit (CPU)

2.3 Power Supply (V_{DD}, V_{SS}, AV_{DD}, and AV_{SS})

The MCU operates from a single 5-volt (nominal) power supply. V_{DD} is the positive power input and V_{SS} is ground. There are three V_{DD}/V_{SS} pairs of pins on the K series devices and two sets on the KS devices. All devices contain a separate pair of power inputs, AV_{DD} and AV_{SS}, for the analog-to-digital (A/D) converter, so that the A/D circuitry can be bypassed independently.

Very fast signal transitions occur on the MCU pins. The short rise and fall times place high, short duration current demands on the power supply. To prevent noise problems, provide good power supply bypassing at the MCU. Also, use bypass capacitors that have good high-frequency characteristics and situate them as close to the MCU as possible. Bypass requirements vary, depending on how heavily the MCU pins are loaded.

2.4 Reset ($\overline{\text{RESET}}$)

This active-low, bidirectional control signal acts as an input to initialize the MCU to a known start-up state. It also serves as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or computer operating properly (COP) watchdog circuit.

The CPU distinguishes between internal and external reset conditions by counting the number of E-clock cycles that occur between the start of reset and the presence of a logic 1 voltage level on the reset pin. Less than two cycles indicates an internal reset; greater than two, an external reset. To prevent the device from misinterpreting the kind of reset that occurs, do not connect an external resistor-capacitor (RC) power-up delay circuit directly to the reset pin.

Table 2-2. Port Signal Summary

Port/Bit	Single-Chip and Bootstrap Modes	Expanded and Special Test Modes
PA0	PA0/IC3	
PA1	PA1/IC2	
PA2	PA2/IC1	
PA3	PA3/OC5/IC4/and-or OC1	
PA4	PA4/OC4/and-or OC1	
PA5	PA5/OC3/and-or OC1	
PA6	PA6/OC2/and-or OC1	
PA7	PA7/PAI/and-or OC1	
PB[7:0]	PB[7:0]	ADDR[15:8]
PC[7:0]	PC[7:0]	DATA[7:0]
PD0	PD0/RxD	
PD1	PD1/TxD	
PD2	PD2/MISO	
PD3	PD3/MOSI	
PD4	PD4/SCK	
PD5	PD5/$\overline{SS}$	
PE[7:0]	PE[7:0]/AN[7:0]	
PF[7:0]	PF[7:0]	ADDR[7:0]
PG0	PG0	PG0/XA13
PG1	PG1	PG1/XA14
PG2	PG2	PG2/XA15
PG3	PG3	PG3/XA16
PG4	PG4	PG4/XA17
PG5	PG5	PG5/XA18
PG6	PG6	PG6
PG7	PG7	PG7/R/$\overline{W}$
PH0	PH0/PW1	
PH1	PH1/PW2	
PH2	PH2/PW3	
PH3	PH3/PW4	
PH4	PH4	PH4/CSIO
PH5	PH5	PH5/CSGP1
PH6	PH6	PH6/CSGP2
PH7	PH7	PH7/CSPROG

Table 3-1. Instruction Set (Sheet 1 of 7)

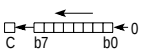
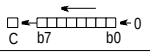
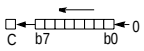
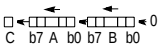
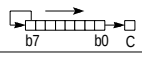
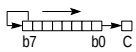
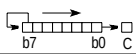
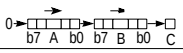
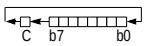
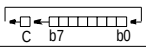
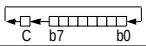
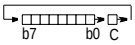
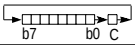
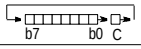
Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
ABA	Add Accumulators	A + B ⇒ A	INH	1B		2			Δ		Δ	Δ	Δ	Δ
ABX	Add B to X	IX + (00 : B) ⇒ IX	INH	3A		3								
ABY	Add B to Y	IY + (00 : B) ⇒ IY	INH	18 3A		4								
ADCA (opr)	Add with Carry to A	A + M + C ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	89 99 B9 A9 18 A9	ii dd hh ll ff ff	2 3 4 4 5			Δ		Δ	Δ	Δ	Δ
ADCB (opr)	Add with Carry to B	B + M + C ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	C9 D9 F9 E9 18 E9	ii dd hh ll ff ff	2 3 4 4 5			Δ		Δ	Δ	Δ	Δ
ADDA (opr)	Add Memory to A	A + M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	8B 9B BB AB 18 AB	ii dd hh ll ff ff	2 3 4 4 5			Δ		Δ	Δ	Δ	Δ
ADDB (opr)	Add Memory to B	B + M ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	CB DB FB EB 18 EB	ii dd hh ll ff ff	2 3 4 4 5			Δ		Δ	Δ	Δ	Δ
ADDD (opr)	Add 16-Bit to D	D + (M : M + 1) ⇒ D	IMM DIR EXT IND,X IND,Y	C3 D3 F3 E3 18 E3	jj kk dd hh ll ff ff	4 5 6 6 7					Δ	Δ	Δ	Δ
ANDA (opr)	AND A with Memory	A M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	84 94 B4 A4 18 A4	ii dd hh ll ff ff	2 3 4 4 5					Δ	Δ	0	
ANDB (opr)	AND B with Memory	B M ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	C4 D4 F4 E4 18 E4	ii dd hh ll ff ff	2 3 4 4 5					Δ	Δ	0	
ASL (opr)	Arithmetic Shift Left		EXT IND,X IND,Y	78 68 18 68	hh ll ff ff	6 6 7					Δ	Δ	Δ	Δ
ASLA	Arithmetic Shift Left A		A INH	48		2					Δ	Δ	Δ	Δ
ASLB	Arithmetic Shift Left B		B INH	58		2					Δ	Δ	Δ	Δ
ASLD	Arithmetic Shift Left D		INH	05		3					Δ	Δ	Δ	Δ
ASR	Arithmetic Shift Right		EXT IND,X IND,Y	77 67 18 67	hh ll ff ff	6 6 7					Δ	Δ	Δ	Δ
ASRA	Arithmetic Shift Right A		A INH	47		2					Δ	Δ	Δ	Δ
ASRB	Arithmetic Shift Right B		B INH	57		2					Δ	Δ	Δ	Δ
BCC (rel)	Branch if Carry Clear	? C = 0	REL	24	rr	3								
BCLR (opr) (msk)	Clear Bit(s)	M $\overline{(mm)}$ ⇒ M	DIR IND,X IND,Y	15 1D 18 1D	dd mm ff mm ff mm	6 7 8					Δ	Δ	0	
BCS (rel)	Branch if Carry Set	? C = 1	REL	25	rr	3								

Table 3-1. Instruction Set (Sheet 2 of 7)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
BEQ (rel)	Branch if = Zero	? Z = 1	REL	27	rr	3								
BGE (rel)	Branch if Δ Zero	? N ⊕ V = 0	REL	2C	rr	3								
BGT (rel)	Branch if > Zero	? Z + (N ⊕ V) = 0	REL	2E	rr	3								
BHI (rel)	Branch if Higher	? C + Z = 0	REL	22	rr	3								
BHS (rel)	Branch if Higher or Same	? C = 0	REL	24	rr	3								
BITA (opr)	Bit(s) Test A with Memory	A M	A IMM A DIR A EXT A IND,X A IND,Y	85 95 B5 A5 18 A5	ii dd hh ll ff ff	2 3 4 4 5					Δ	Δ	0	
BITB (opr)	Bit(s) Test B with Memory	B M	B IMM B DIR B EXT B IND,X B IND,Y	C5 D5 F5 E5 18 E5	ii dd hh ll ff ff	2 3 4 4 5					Δ	Δ	0	
BLE (rel)	Branch if Δ Zero	? Z + (N ⊕ V) = 1	REL	2F	rr	3								
BLO (rel)	Branch if Lower	? C = 1	REL	25	rr	3								
BLS (rel)	Branch if Lower or Same	? C + Z = 1	REL	23	rr	3								
BLT (rel)	Branch if < Zero	? N ⊕ V = 1	REL	2D	rr	3								
BMI (rel)	Branch if Minus	? N = 1	REL	2B	rr	3								
BNE (rel)	Branch if not = Zero	? Z = 0	REL	26	rr	3								
BPL (rel)	Branch if Plus	? N = 0	REL	2A	rr	3								
BRA (rel)	Branch Always	? 1 = 1	REL	20	rr	3								
BRCLR(opr) (msk) (rel)	Branch if Bit(s) Clear	? M mm = 0	DIR IND,X IND,Y	13 1F 18 1F	dd mm rr ff mm rr ff mm rr	6 7 8								
BRN (rel)	Branch Never	? 1 = 0	REL	21	rr	3								
BRSET(opr) (msk) (rel)	Branch if Bit(s) Set	? (M) mm = 0	DIR IND,X IND,Y	12 1E 18 1E	dd mm rr ff mm rr ff mm rr	6 7 8								
BSET (opr) (msk)	Set Bit(s)	M + mm ⇒ M	DIR IND,X IND,Y	14 1C 18 1C	dd mm ff mm ff mm	6 7 8					Δ	Δ	0	
BSR (rel)	Branch to Subroutine	See Figure 3-2	REL	8D	rr	6								
BVC (rel)	Branch if Overflow Clear	? V = 0	REL	28	rr	3								
BVS (rel)	Branch if Overflow Set	? V = 1	REL	29	rr	3								
CBA	Compare A to B	A B	INH	11		2					Δ	Δ	Δ	Δ
CLC	Clear Carry Bit	0 ⇒ C	INH	0C		2								0
CLI	Clear Interrupt Mask	0 ⇒ I	INH	0E		2				0				
CLR (opr)	Clear Memory Byte	0 ⇒ M	EXT IND,X IND,Y	7F 6F 18 6F	hh ll ff ff	6 6 7					0	1	0	0
CLRA	Clear Accumulator A	0 ⇒ A	A INH	4F		2					0	1	0	0
CLRB	Clear Accumulator B	0 ⇒ B	B INH	5F		2					0	1	0	0
CLV	Clear Overflow Flag	0 ⇒ V	INH	0A		2							0	
CMPA (opr)	Compare A to Memory	A M	A IMM A DIR A EXT A IND,X A IND,Y	81 91 B1 A1 18 A1	ii dd hh ll ff ff	2 3 4 4 5					Δ	Δ	Δ	Δ
CMPB (opr)	Compare B to Memory	B M	B IMM B DIR B EXT B IND,X B IND,Y	C1 D1 F1 E1 18 E1	ii dd hh ll ff ff	2 3 4 4 5					Δ	Δ	Δ	Δ

Table 3-1. Instruction Set (Sheet 5 of 7)

Mnemonic	Operation	Description	Addressing Mode	Instruction Opcode	Instruction Operand	Instruction Cycles	Condition Codes S	X	H	I	N	Z	V	C
LSRD	Logical Shift Right Double		INH	04		3					0	Δ	Δ	Δ
MUL	Multiply 8 by 8	A * B ⇒ D	INH	3D		10								Δ
NEG (opr)	Two s Complement Memory Byte	0 M ⇒ M	EXT IND,X IND,Y	70 60 18 60	hh ll ff ff	6 6 7					Δ	Δ	Δ	Δ
NEGA	Two s Complement A	0 A ⇒ A	A INH	40		2					Δ	Δ	Δ	Δ
NEGB	Two s Complement B	0 B ⇒ B	B INH	50		2					Δ	Δ	Δ	Δ
NOP	No operation	No Operation	INH	01		2								
ORAA (opr)	OR Accumulator A (Inclusive)	A + M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	8A 9A BA AA 18 AA	ii dd hh ll ff ff	2 3 4 4 5					Δ	Δ	0	
ORAB (opr)	OR Accumulator B (Inclusive)	B + M ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	CA DA FA EA 18 EA	ii dd hh ll ff ff	2 3 4 4 5					Δ	Δ	0	
PSHA	Push A onto Stack	A ⇒ Stk,SP = SP 1	A INH	36		3								
PSHB	Push B onto Stack	B ⇒ Stk,SP = SP 1	B INH	37		3								
PSHX	Push X onto Stack (Lo First)	IX ⇒ Stk,SP = SP 2	INH	3C		4								
PSHY	Push Y onto Stack (Lo First)	IY ⇒ Stk,SP = SP 2	INH	18 3C		5								
PULA	Pull A from Stack	SP = SP + 1, A ⇐ Stk	A INH	32		4								
PULB	Pull B from Stack	SP = SP + 1, B ⇐ Stk	B INH	33		4								
PULX	Pull X From Stack (Hi First)	SP = SP + 2, IX ⇐ Stk	INH	38		5								
PULY	Pull Y from Stack (Hi First)	SP = SP + 2, IY ⇐ Stk	INH	18 38		6								
ROL (opr)	Rotate Left		EXT IND,X IND,Y	79 69 18 69	hh ll ff ff	6 6 7					Δ	Δ	Δ	Δ
ROLA	Rotate Left A		A INH	49		2					Δ	Δ	Δ	Δ
ROLB	Rotate Left B		B INH	59		2					Δ	Δ	Δ	Δ
ROR (opr)	Rotate Right		EXT IND,X IND,Y	76 66 18 66	hh ll ff ff	6 6 7					Δ	Δ	Δ	Δ
RORA	Rotate Right A		A INH	46		2					Δ	Δ	Δ	Δ
RORB	Rotate Right B		B INH	56		2					Δ	Δ	Δ	Δ
RTI	Return from Interrupt	See Figure 3-2	INH	3B		12	Δ	↓	Δ	Δ	Δ	Δ	Δ	Δ
RTS	Return from Subroutine	See Figure 3-2	INH	39		5								

4.2 Introduction

This section presents the elements involved in configuring the M68HC11K/KS Family microcontrollers (MCUs), including:

- A list of the control registers, see 4.3 Control Registers
- Special registers that control system initialization, see 4.4 System Initialization
- Description of the four operating modes and how they're selected, see 4.5 Operating Modes
- Memory maps of the K Family, see 4.6 Memory Map
- Information on programming EPROM (erasable, programmable read-only memory) and EEPROM (electrically erasable, programmable read-only memory), see 4.7 EPROM/OTPROM (M68HC711K4 and M68HC711KS2) and 4.8 EEPROM and the CONFIG Register

4.3 Control Registers

The heart of the M68HC11 Family of MCUs is a special register block which controls the peripheral functions. In the K Family, this block is 128 bytes. The default location of this block is the first 128 bytes of memory, but software can map it to any 4-Kbyte boundary (see 4.6.1 Control Registers and RAM).

Certain bits and registers that control initialization and the basic operation of the MCU are protected against writes in normal operating modes except under special circumstances. Some bits cannot be written at all; others can be written only once and/or within the first 64 bus cycles after any reset. The special operating modes override these restrictions. These bits and registers are discussed in 4.4 System Initialization .

Normal and special operating modes are discussed in 4.5 Operating Modes . The write-restricted registers and bits are summarized in Table 4-1 .

Figure 4-1 lists the entire 128-byte register block in ascending order by address, using the default memory block assignment $0000–$007F.

LSBF — Least Significant Bit (LSB) First Enable Bit

For detailed information, refer to Section 8. Serial Peripheral Interface (SPI) .

1 = Data is transferred LSB first.

0 = Data is transferred MSB (most significant bit) first.

SPR2 — SPI Clock Rate Selected Bit

This bit adds a divide-by-four to the SPI clock chain. For detailed information, refer to Section 8. Serial Peripheral Interface (SPI) .

XDV[1:0] — XOUT Clock Divide Select Bits

These bits control the frequency of the clock driven out of the XOUT pin, if enabled by the CLKX bit on the CONFIG register. See Table 5-4

Table 5-4. XOUT Clock Divide Select

XDV [1:0]	XOUT = EXTAL Divided By	Frequency at EXTAL = 8 MHz	Frequency at EXTAL = 12 MHz	Frequency at EXTAL = 16 MHz
0 0	1	8 MHz	12 MHz	16 MHz
0 1	4	2 MHz	3 MHz	4 MHz
1 0	6	1.3 MHz	2 MHz	2.7 MHz
1 1	8	1 MHz	1.5 MHz	2 MHz

5.4 Effects of Reset

When the MCU recognizes a reset condition, it forces the CPU registers and control bits to established initial states. These in turn force the on-chip peripheral systems to known startup states, as described here.

- Central processor unit (CPU)
  - The stack pointer and other CPU registers are indeterminate immediately after reset, except for three bits in the condition code register (CCR).
  - The X and I interrupt mask bits are set to mask any interrupt requests, and the S bit in the CCR is set to inhibit the stop mode.
- Memory map
  - The INIT register is initialized to $00, putting the control registers at locations $0000–$007F.
  - The 1.5 Kbytes of RAM are at locations $0080–$067F except for the M68HC11KS Family, which has 1 Kbytes of RAM at locations $0080–$047F.
  - The INIT2 register is $00, locating the EEPROM at $0D80–$0FFF.
- Timer
  - The timing system is initialized to a count of $0000.
  - The prescaler bits are cleared, and all output compare registers are initialized to $FFFF.
  - All input capture registers are indeterminate after reset.
  - The output compare 1 mask (OC1M) register is cleared so that successful OC1 compares do not affect any input/output (I/O) pins. The other four output compares are configured so that they do not affect any I/O pins on successful compares.
  - All input capture edge-detector circuits are configured for capture disabled operation.
  - The timer overflow interrupt flag and all eight timer function interrupt flags are cleared.

to restart the system, a normal reset sequence results and all pins and registers are reinitialized.

To use the $\overline{\text{IRQ}}$ pin as a means of recovering from STOP, the I bit in the CCR must be clear ($\overline{\text{IRQ}}$ not masked). The $\overline{\text{XIRQ}}$ pin can be used to wake up the MCU from STOP regardless of the state of the X bit in the CCR, although the state of this bit does affect the recovery sequence. If X is clear ($\overline{\text{XIRQ}}$ not masked), the MCU executes a normal XIRQ service routine. If X is set ($\overline{\text{XIRQ}}$ masked or inhibited), then processing continues with the instruction that immediately follows the STOP instruction, and no $\overline{\text{XIRQ}}$ interrupt service is requested or pending.

Executing a STOP instruction requires special consideration when the clock monitor is enabled. Because the stop function halts all clocks, the clock monitor function will generate a reset sequence if it is enabled at the time the stop mode was initiated. To prevent this, clear the CME and FCME bits in the OPTION register before executing a STOP instruction to disable the clock monitor. After recovery from STOP, set the CME bit to enable the clock monitor.

Systems using the internal oscillator require a delay after restart upon leaving STOP to allow the oscillator to stabilize. If a stable external oscillator is used, the DLY control bit in the OPTION register can be used to bypass this startup delay (see Figure 5-11). Reset sets the DLY control bit; it can be cleared during initialization. Do not use reset to recover from STOP if the DLY is to be bypassed, since reset sets the DLY bit again, causing the restart delay. This same delay will follow a power-on reset, regardless of the state of the DLY control bit, but does not apply to a reset while the clocks are running.

Address: $0039

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ADPLE	DSEL	IRQE(1)	DLY(1)	CME	FCME(1)	CR1(1)	CR0(1)
Reset:	0	0	0	1	0	0	0	0

1. Can be written only once in first 64 cycles out of reset in normal modes or at any time in special modes

Figure 5-11. System Configuration Options Register (OPTION)

6.9 Port G

The state of port G pin 7 (PG7) at reset is mode dependent. In single-chip or bootstrap modes, it is a high-impedance input; its data direction can be changed through DDRG. In expanded and special test modes, PG7 functions as the R/$\overline{W}$ line to control the direction of data flow between the MCU and external memory devices.

Port G pins (PG[6:0]) reset to high-impedance inputs in any mode. Data direction can be changed through DDRG. Port G bits [5:0] can serve as memory expansion address lines (see 11.3 Memory Expansion) in expanded and special test modes. M68HC11KS devices do not contain these pins.

All eight port G pins have selectable internal pullup resistors (see 6.11 Internal Pullup Resistors).

Address: $007E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PG7	PG6(1)	PG5(1)	PG4(1)	PG3(1)	PG2(1)	PG1(1)	PG0(1)
Reset:	0	0	0	0	0	0	0	0
Alternate Pin Function:	R/$\overline{W}$	—	XA18	XA17	XA16	XA15	XA14	XA13

1. Not available on KS devices

Figure 6-13. Port G Data Register (PORTG)

Address: $007F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDG7	DDG6(1)	DDG5(1)	DDG4(1)	DDG3(1)	DDG2(1)	DDG1(1)	DDG0(1)
Reset:	0	0	0	0	0	0	0	0

1. Not available on KS devices

Figure 6-14. Port G Data Direction Register (DDRG)

DDG[7:0] Data Direction for Port G Bits
0 = Input
1 = Output

8.4.4 Slave Select ($\overline{SS}$)

The slave select ($\overline{SS}$) input is used to target specific devices in the SPI system. It must be pulled low on a targeted slave device prior to any communication with a master and must remain low for the duration of the transaction. $\overline{SS}$ must always be high on any device in master mode. Pulling $\overline{SS}$ low on a master mode device generates a mode fault error (see 8.5.1 Mode Fault Error).

8.4.5 SPI Timing

Four possible timing relationships are available through control bits CPOL (clock polarity) and CPHA (clock phase) in the SPCR. These bits must be the same in both master and slave devices. The master device always places data on the MOSI line approximately a half-cycle before the SCK clock edge. This enables the slave device to latch the data. See Figure 8-2 .

A write collision is normally a slave error because a slave has no control over when a master initiates a transfer. A master knows when a transfer is in progress, so there is no reason for a master to generate a write-collision error, although the SPI logic can detect write collisions in both master and slave devices.

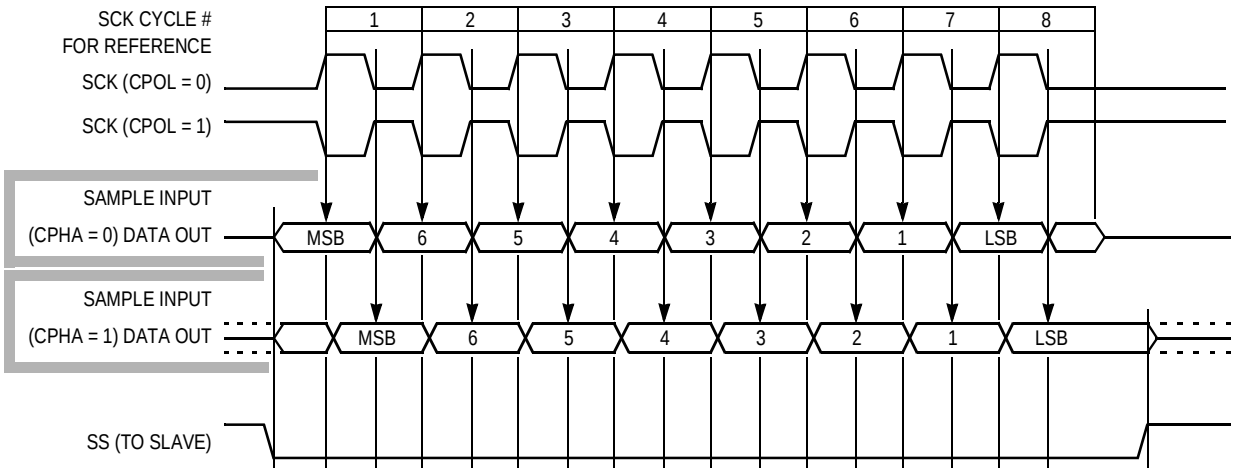


Figure 8-2. Data Clock Timing Diagram

NOTE: Throughout this manual, the registers are discussed by function. In the event that not all bits in a register are referenced, the bits that are not discussed are shaded.

8.6.1 Serial Peripheral Control Register

Address: $0028

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR2
Reset:	0	0	0	0	0	1	U	U

U = Undefined

Figure 8-3. Serial Peripheral Control Register (SPCR)

SPIE Serial Peripheral Interrupt Enable Bit

0 = SPI interrupt disabled

1 = SPI interrupt is enabled each time the SPIF or MODF status flag in SPSR is set.

SPE Serial Peripheral System Enable Bit

0 = SPI off

1 = SPI on PD[5:2] function as SPI signals

DWOM Port D Wired-OR Mode Bit

DWOM affects only the four SPI pins on port D, PD[5:2]. See also 7.9.2 Serial Communications Control Register 1 for a discussion of the WOMS (wired-OR Mode for SCI pins) bit in the serial communications control register 1 (SCCR1).

0 = Normal CMOS outputs

1 = Open-drain outputs

MSTR Master Mode Select Bit

0 = Slave mode

1 = Master mode

register is set after the fourth conversion in a sequence to signal the availability of data in the result registers.The result registers are written during a portion of the system clock cycle when reads do not occur, so there is no conflict. A conversion sequence can repeat continuously or stop after one iteration. Figure 10-2 shows the timing of a typical sequence. In this example, synchronization is referenced to the system E clock.

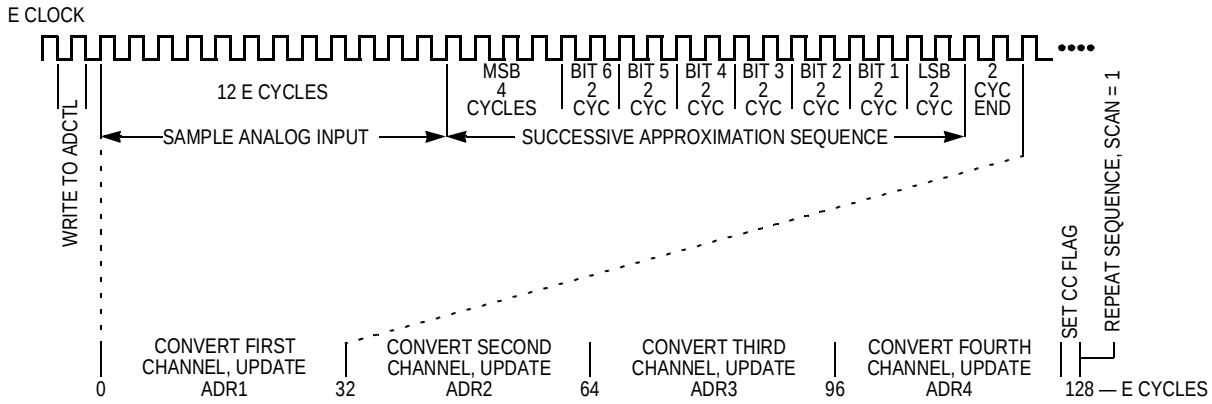


Figure 10-2. A/D Conversion Sequence

10.3.4 Digital Control

In addition to the conversion complete status flag, ADCTL bits select single or continuous conversions, whether conversions are performed on single or multiple channels, and the analog input(s) to be converted.

Single or continuous conversions are selected by the SCAN bit. Clearing the SCAN bit selects the single conversion option, in which results are written to each of the four result registers one time. The first result is stored in A/D result register 1 (ADR1), and the fourth result is stored in ADR4. All conversion activity is then halted until the ADCTL register is written again. In the continuous mode (SCAN =1), conversion activity does not stop. The fifth conversion is stored in register ADR1 (overwriting the first conversion result), the sixth conversion overwrites ADR2, and so on.

Address: $0039

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ADPU	CSEL	IRQE	DLY(1)	CME	FCME	CR1	CR0
Reset:	0	0	0	1	0	0	0	0

1. DLY can be written only once in the first 64 cycles out of reset in normal modes or at any time in special modes.

Figure 10-3. System Configuration Options Register (OPTION)

ADPU A/D Power-up
0 = A/D powered down
1 = A/D powered up

CSEL Clock Select
0 = A/D and EEPROM use system E clock.
1 = A/D and EEPROM use internal RC clock.

10.4.2 A/D Control/Status Register

All bits in this register can be read or written except bit 7, which is a read-only status indicator, and bit 6, which always reads as 0. Writing to ADCTL initiates a conversion, aborting any conversion in progress.

Address: $0030

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CCF		SCAN	MULT	CD	CC	CB	CA
Write:								
Reset:	0	0	U	U	U	U	U	U

= Unimplemented U = Unaffected by reset

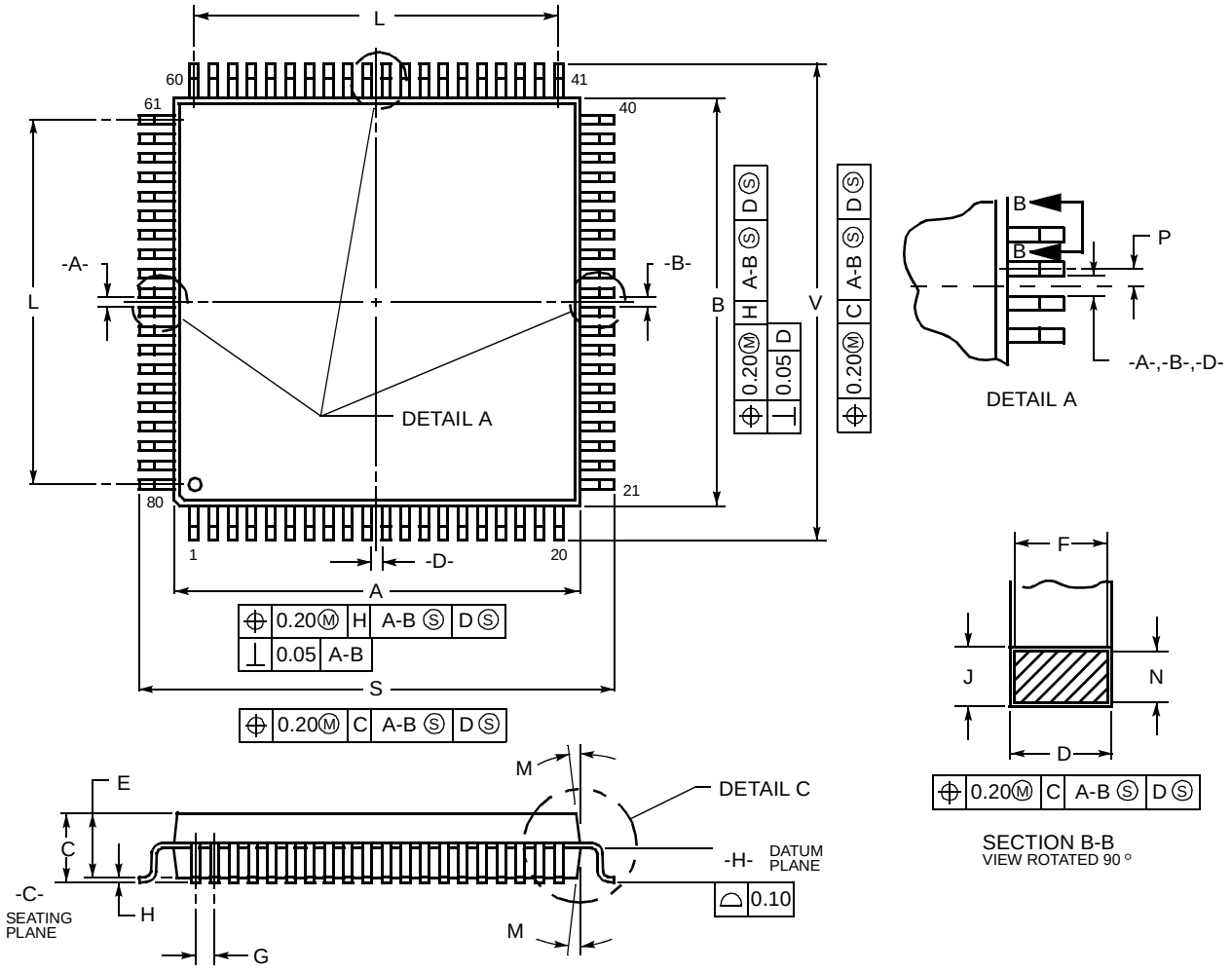
Figure 10-4. Analog-to-Digital Control/Status Register (ADCTL)

12.11 Expansion Bus Timing

Num	Characteristic (1)	Symbol	2.0 MHz		3.0 MHz		4.0 MHz		Unit
			Min	Max	Min	Max	Min	Max	
	Frequency of operation (E clock)(2)	f_o	dc	2.0	dc	3.0	dc	4.0	MHz
1	Cycle time, $t_{cyc} = 1/f_o$	t_{cyc}	500		333		250		ns
2	Pulse width, E low, $PW_{EL} = 1/2\ t_{cyc}$ 20 ns	PW_{EL}	230		147		105		ns
3	Pulse width, E high(3) $PW_{EH} = 1/2\ t_{cyc}$ 25 ns	PW_{EH}	225		142		100		ns
4A 4B	E clock Rise time Fall time	 t_r t_f		 20 20		 20 18		 20 15	ns
9	Address hold time, $t_{AH} = 1/8\ t_{cyc}$ 10 ns	t_{AH}	53		32		21		ns
11	Address delay time, $t_{AD} = 1/8\ t_{cyc} + 40$ ns	t_{AD}		103		82		71	ns
12	Address valid time to E rise $t_{AV} = PW_{EL}$ t_{AD}	t_{AV}	128		65		34		ns
17	Read data setup time	t_{DSR}	30		30		20		ns
18	Read data hold time	t_{DHR}	0		0		0		ns
19	Write data delay time	t_{DDW}		40		40		40	ns
21	Write data hold time, $t_{DHW} = 1/8\ t_{cyc}$	t_{DHW}	63		42		31		ns
29	MPU address access time(3) $t_{ACCA} = t_{cyc}$ t_f t_{DSR} t_{AD}	t_{ACCA}	348		203		144		ns
39	Write data setup time(3) $t_{DSW} = PW_{EH}$ t_{DDW}	t_{DSW}	185		102		60		ns
50	E valid chip-select delay time	t_{ECSD}		40		40		40	ns
51	E valid chip-select access time(3) $t_{ECSA} = PW_{EH}$ t_{ECSD} t_{DSR}	t_{ECSA}	155		72		40		ns
52	Chip select hold time	t_{CH}	0	20	0	20	0	20	ns
54	Address valid chip-select delay time $t_{ACSD} = 1/4\ t_{cyc} + 40$ ns	t_{ACSD}		165		123		103	ns
55	Address valid chip-select access time $t_{ACSA} = t_{cyc}$ t_f t_{DSR} t_{ACSD}(3)	t_{ACSA}	285		162		113		ns
56	Address valid to chip-select time	t_{AVCS}	10		10		10		ns
57	Address valid to data three-state time	t_{AVDZ}		10		10		10	ns

1. $V_{DD} = 5.0 \pm 10\%$, $V_{SS} = 0$ Vdc, $T_A = T_L$ to T_H, unless otherwise noted
   All timing measurements refer to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Input clocks with duty cycles other than 50% affect bus performance.
3. This parameter is affected by clock stretching. Add n(t_{cyc}) to parameter value, where n = 1, 2, or 3 depending on values written to CSCSTR register or n = 1 for STRCH = 1 on KS parts.

13.5 80-Pin Quad Flat Pack (Case 841B)



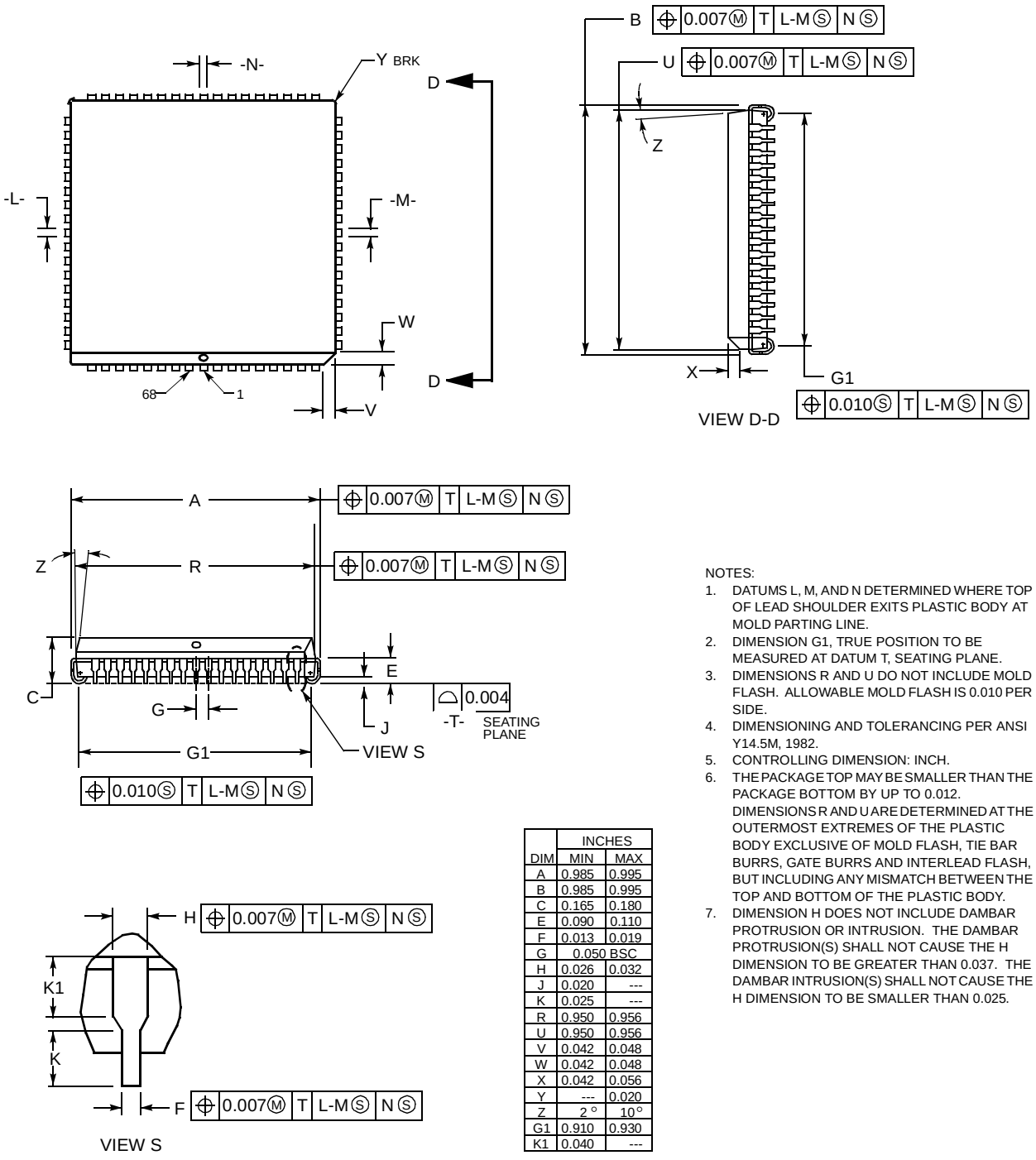
DETAIL A

DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS	
DIM	MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5 °	10 °
N	0.13	0.17
P	0.325 BSC	
Q	0 °	7 °
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0 °	---
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	

13.7 68-Pin Plastic Leaded Chip Carrier (Case 779)



DIM	INCHES MIN	INCHES MAX
A	0.985	0.995
B	0.985	0.995
C	0.165	0.180
E	0.090	0.110
F	0.013	0.019
G	0.050 BSC	
H	0.026	0.032
J	0.020	---
K	0.025	---
R	0.950	0.956
U	0.950	0.956
V	0.042	0.048
W	0.042	0.048
X	0.042	0.056
Y	---	0.020
Z	2 °	10 °
G1	0.910	0.930
K1	0.040	---

NOTES:
1. DATUMS L, M, AND N DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM T, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012. DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037. THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025.