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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	4MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	37
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	640 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc11k1cfue4

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Section 2. Pin Description

2.1 Contents

2.2 Introduction

The M68HC11K Family is available in a variety of packages, as shown in **Table 1-1. M68HC11K Family Devices**. Most pins on this MCU serve two or more functions, as described in this section. Pin assignments for the various package types are shown in **Figure 2-1**, **Figure 2-2**, **Figure 2-3**, and **Figure 2-4**.

Pin Description

3.3.5 Program Counter (PC)

The 16-bit program counter contains the address of the next instruction to be executed. Its initial value after reset is fetched from one of six possible vectors, depending on operating mode and the cause of reset, as described in **5.3 Sources of Resets**.

3.3.6 Condition Code Register (CCR)

This 8-bit register contains:

- Five condition code indicators (C, V, Z, N, and H)
- Two interrupt masking bits (IRQ and XIRQ)
- A stop disable bit (S)

Most instructions update condition codes automatically, as described in the following paragraphs. Certain instructions, such as pushes, pulls, add B to X (ABX), add B to Y (ABY), and transfer/exchange instructions do not affect the condition codes. **Table 3-1** shows which condition codes are affected by each instruction.

3.3.6.1 Carry/Borrow (C)

The C bit is set if the CPU performs a carry or borrow during an arithmetic operation. This bit also acts as an error flag for multiply and divide operations. Shift and rotate instructions operate with and through the carry bit to facilitate multiple-word shift operations.

3.3.6.2 Overflow (V)

The overflow bit is set if an operation results in a two’s complement overflow of the 8-bit signed range –128 to +127. Otherwise, the V bit is cleared.

3.3.6.3 Zero (Z)

The Z bit is set if the result of an arithmetic, logic, or data manipulation operation is 0. Otherwise, the Z bit is cleared. Compare instructions do

NOTE: *Throughout this manual, the registers are discussed by function. In the event that not all bits in a register are referenced, the bits that are not discussed are shaded.*

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PORTA) See page 138.	Read: Write:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Reset:	Undefined after reset							
$0001	Port A Data Direction Register (DDRA) See page 138.	Read: Write:	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0
		Reset:	0	0	0	0	0	0	0	0
$0002	Port B Data Direction Register (DDRB) See page 139.	Read: Write:	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
		Reset:	0	0	0	0	0	0	0	0
$0003	Port F Data Direction Register (DDRF) See page 144.	Read: Write:	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0
		Reset:	0	0	0	0	0	0	0	0
$0004	Port B Data Register (PORTB) See page 139.	Read: Write:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
		Reset:	Undefined after reset							
$0005	Port F Data Register (PORTF) See page 144.	Read: Write:	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
		Reset:	Undefined after reset							
$0006	Port C Data Register (PORTC) See page 140.	Read: Write:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Reset:	Undefined after reset							
$0007	Port C Data Direction Register (DDRC) See page 141.	Read: Write:	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
		Reset:	0	0	0	0	0	0	0	0
$0008	Port D Data Register (PORTD) See page 142.	Read: Write:	0	0	PD5	PD4	PD3	PD2	PD1	PD0
		Reset:	0	0	U	U	U	U	U	U
$0009	Port D Data Direction Register (DDRD) See page 142.	Read: Write:	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Undefined

Figure 4-1. Register and Control Bit Assignments (Sheet 1 of 11)

Address: $003F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ROMAD	1	CLKX	PAREN	NOSEC	NOCOP	ROMON	EEON
Reset:	—	1	—	—	—	—	—	—

Figure 4-6. System Configuration Register (CONFIG)

NOTE: *CONFIG is writable once in normal modes and writable at any time in special modes.*

ROMAD — ROM Address Mapping Control Bit

Set out of reset in single-chip mode

0 = (EP)ROM set at $2000–$7FFF;
$0000–$7FFF in [7]11KS2;
$0000–$BFFF in [7]11KS8
(expanded mode only)

1 = (EP)ROM set at $A000–$FFFF;
$8000–$FFFF in [7]11KS2;
$4000–$FFFF in [7]11KS8

ROMON — ROM/PROM Enable Bit

Set by reset in single-chip mode; cleared by reset in special test mode

0 = (EP)ROM removed from the memory map
1 = (EP)ROM present in the memory map

EEON — EEPROM Enable Bit

0 = 640-byte EEPROM disabled
1 = 640-byte EEPROM enabled

4.8.2.2 EEPROM Bulk Erase

```
BULKE   LDAB    #$06
        STAB    $003B   Set EELAT and ERASE.
        STAA    $0,X    Store any data to any EEPROM address
        LDAB    #$07
        STAB    $002B   Set EEPGM bit as well
                        to enable EEPROM programming voltage
        JSR     DLY10   Delay 10 ms
        CLR     $003B   Turn off programming voltage and set
                        to READ mode
```

4.8.2.3 EEPROM Row Erase

```
ROWE    LDAB    #$07
        STAB    $003B   Set EELAT, ERASE and ROW.
        STAA    $0,X    Store any data to any EEPROM address
                        in row
        LDAB    #$07
        STAB    $002B   Set EEPGM bit as well
                        to enable EEPROM programming voltage
        JSR     DLY10   Delay 10 ms
        CLR     $003B   Turn off programming voltage and set
                        to READ mode
```

4.8.2.4 EEPROM Byte Erase

```
BYTEE   LDAB    #$16
        STAB    $003B   Set EELAT, ERASE and BYTE.
        STAA    $0,X    Store any data to targeted EEPROM
                        address
        LDAB    #$17
        STAB    $002B   Set EEPGM bit as well
                        to enable EEPROM programming voltage
        JSR     DLY10   Delay 10 ms
        CLR     $003B   Turn off programming voltage and set
                        to READ mode
```

  - All nine timer interrupts are disabled because their mask bits have been cleared.
  - The I4/O5 bit in the PACTL register is cleared to configure the I4/O5 function as OC5; however, the OM5:OL5 control bits in the TCTL1 register are clear so OC5 does not control the PA3 pin.

- Real-time interrupt (RTI)
  - The RTI enable bit in TMSK2 is cleared, masking automatic hardware interrupts.
  - The rate control bits are cleared after reset and can be initialized by software before the RTI system is enabled.
- Pulse accumulator
  - The pulse accumulator system is disabled at reset.
  - The PAI input pin defaults to a general-purpose input pin (PA7).
- Computer operating properly (COP) watchdog system
  - The COP watchdog system is enabled if the NOCOP control bit in the CONFIG register is clear and disabled if NOCOP is set.
  - The OPTION register's CR[1:0] bits are cleared, setting the COP rate for the shortest duration timeout.
- Serial communications interface (SCI)
  - At reset, the SCI baud rate control register (**7.9.1 SCI Baud Rate Control Register**) is initialized to $0004.
  - All transmit and receive interrupts are masked and both the transmitter and receiver are disabled so the port pins default to being general-purpose I/O lines.
  - The SCI frame format is initialized to an 8-bit character size.
  - The send break and receiver wake-up functions are disabled.
  - The TDRE and TC status bits in the SCI status register are both set, indicating that there is no transmit data in either the transmit data register or the transmit serial shift register.

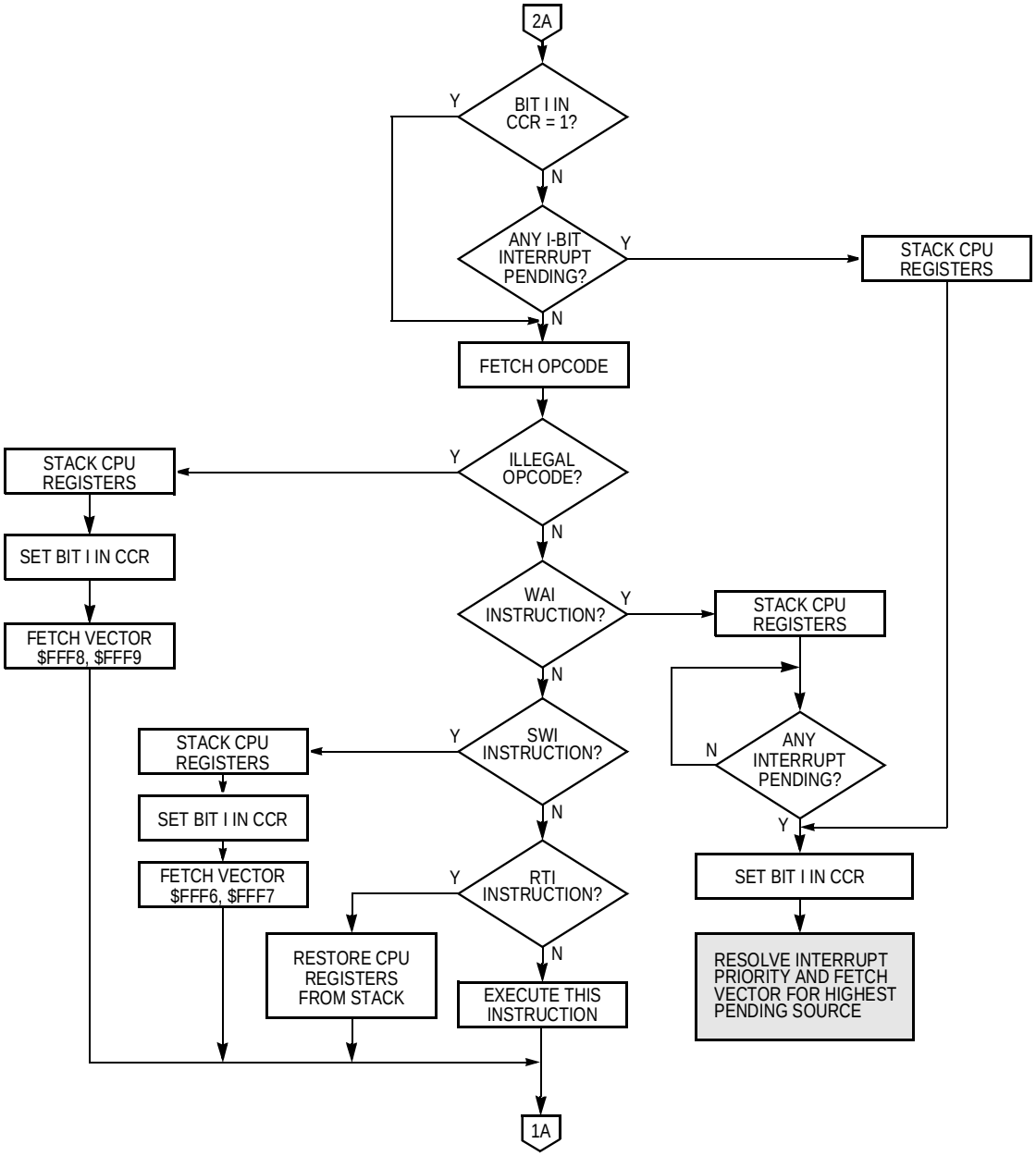

Figure 5-8. Processing Flow Out of Reset (Sheet 2 of 2)

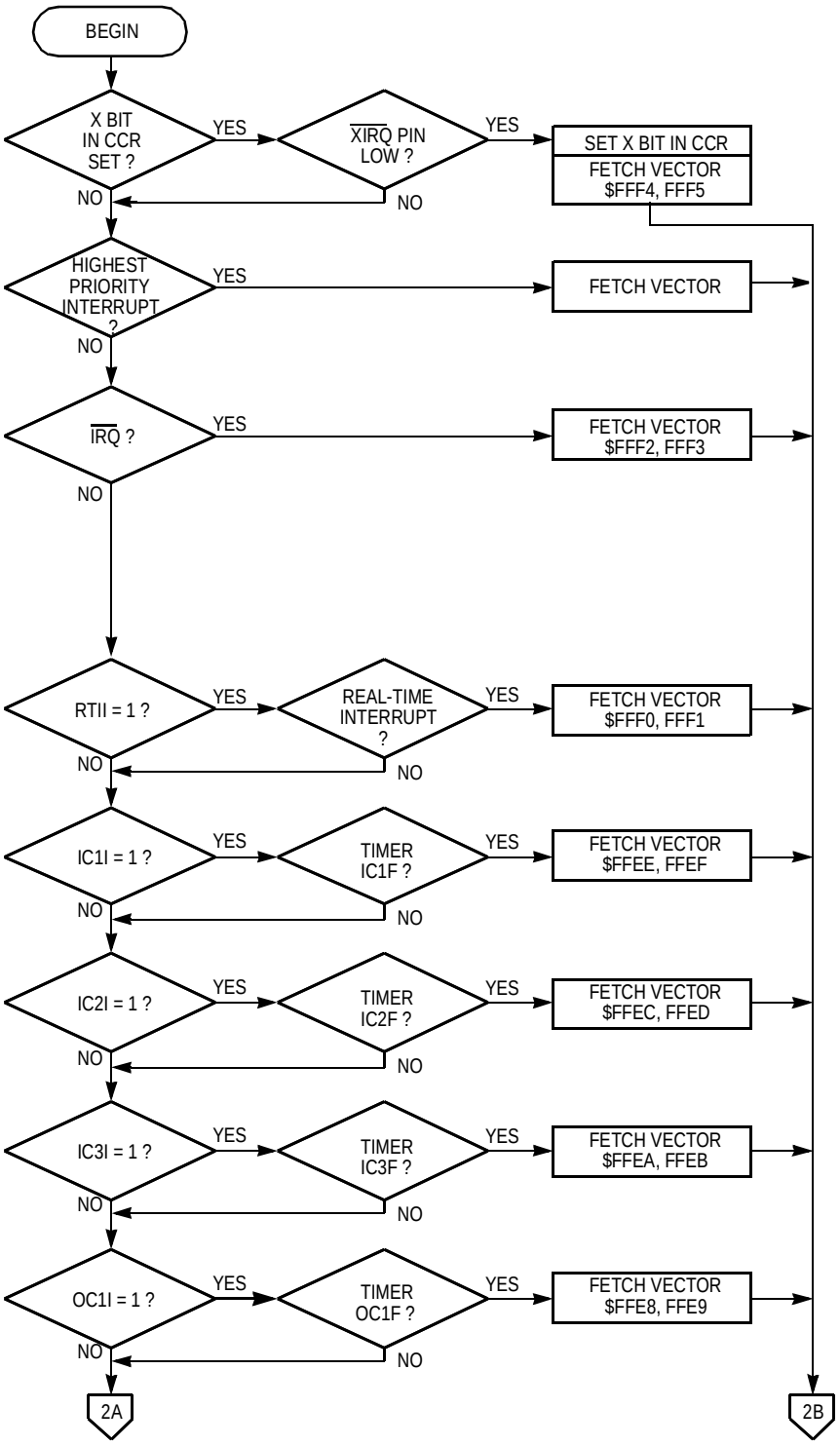

Figure 5-9. Interrupt Priority Resolution (Sheet 1 of 2)

The M68HC11K series offers several enhancements to the basic MC68HC11 SCI, including:

- 13-bit modulus prescaler in the baud generator
- Receiver-active flag
- Transmitter and receiver hardware parity
- Accelerated idle line detection

7.3 Data Format

The SCI uses the standard non-return to zero mark/space data format illustrated in **Figure 7-1**.

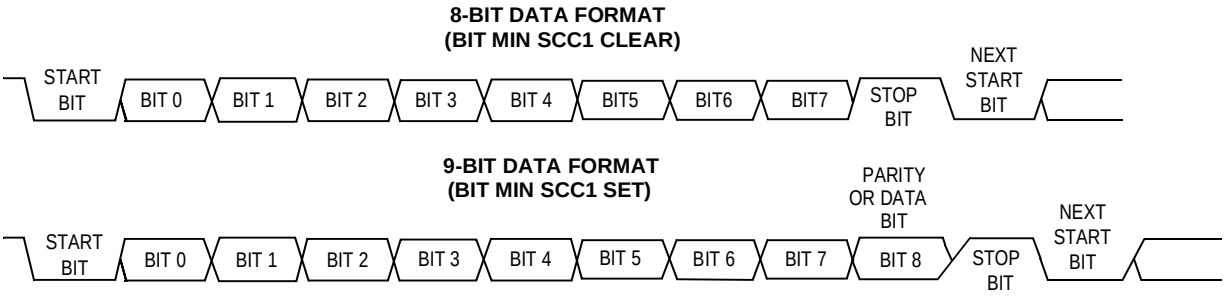

Figure 7-1. SCI Data Formats

Data is transmitted in frames consisting of a start bit, a word of eight or nine data bits, and a stop bit. The step-by-step transmission procedure is:

1. The transmission line is idle before a message is transmitted. This means that the line is in a logic 1 state for at least one frame time.
2. A start bit, logic 0, is transmitted, indicating the start of a frame.
3. An 8-bit or 9-bit word is transmitted, least significant bit (LSB) first.
4. A stop bit, logic 1, is transmitted to indicate the end of a frame.
5. An optional number of breaks can be transmitted. A break is the transmission of a logic low state for one frame time. After the last break character is sent, the line goes high for at least one bit time.

7.9.2 Serial Communications Control Register 1

Address $0072

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	LOOPS	WOMS	0	M	WAKE	ILT	PE	PT
Reset:	U	U	0	0	0	0	0	0

U = Undefined

Figure 7-7. SCI Control Register 1 (SCCR1)

LOOPS — SCI Loop Mode Enable Bit

Both the transmitter and receiver must be enabled to use the loop mode. When the loop mode is enabled, the TxD pin is driven high (idle line state) if the transmitter is enabled.

0 = SCI transmit and receive operate normally.
1 = SCI transmit and receive are disconnected from TxD and RxD pins, and transmitter output is fed back into the receiver input.

WOMS — Wired-OR Mode for SCI Pins PD[1:0] Bits

See also **8.6.1 Serial Peripheral Control Register** for a description of the DWOM (port D wired-OR mode) bit in the serial peripheral control register (SPCR).

0 = TxD and RxD operate normally.
1 = TxD and RxD are open drains if operating as outputs.

M — Mode (SCI Word Size) Bit

0 = Start bit, 8 data bits, 1 stop bit
1 = Start bit, 9 data bits, 1 stop bit

WAKE — Wakeup Mode Bit

0 = Wake up by idle line recognition
1 = Wake up by address mark (most significant data bit set)

ILT — Idle Line Type Bit

0 = Short (SCI counts consecutive 1s after start bit.)
1 = Long (SCI counts one only after stop bit.)

TDRE — Transmit Data Register Empty Flag

TDRE is set when the SCDR transfers its contents to the transmission shift register.

0 = SCDR is full.
1 = SCDR is empty.

TC — Transmit Complete Flag

TC is set when the final character in a message has been sent (no data, preamble, or break transmissions pending).

0 = Transmitter busy
1 = Transmitter idle

RDRF — Receive Data Register Full Flag

RDRF is set when the shift register has received a complete character and transferred it to the receive data register.

0 = RDR not full
1 = RDR full

IDLE — Idle Line Detected Flag

IDLE is set when a frame of all 1s is received after a message.

0 = RxD line is active.
1 = RxD line is idle.

OR — Overrun Error Flag

OR is set if a new character is received before a previously received character is read from SCDR.

0 = No overrun
1 = Overrun detected

NF — Noise Error Flag

NF is set after the last bit in a frame is received if the samples in the receiver's data recovery circuit are not unanimous for any of the bits, including start and stop bits.

0 = No noise detected
1 = Noise detected

Section 8. Serial Peripheral Interface (SPI)

8.1 Contents

8.2 Introduction

The serial peripheral interface (SPI) provides synchronous communication between the MCU and peripheral devices such as transistor-transistor logic (TTL) shift registers, liquid crystal display (LCD) drivers, analog-to-digital (A/D) converter subsystems, and other processors. Synchronous communication requires a clock and, in the M68HC11 series, a slave-select signal, but provides substantially faster communication than the asynchronous SCI, which does not require this

Section 9. Timing System

9.1 Contents

10.3 Functional Description

The A/D converter system consists of four functional blocks as shown in **Figure 10-1**:

- Multiplexer
- Analog converter
- Result storage
- Digital control

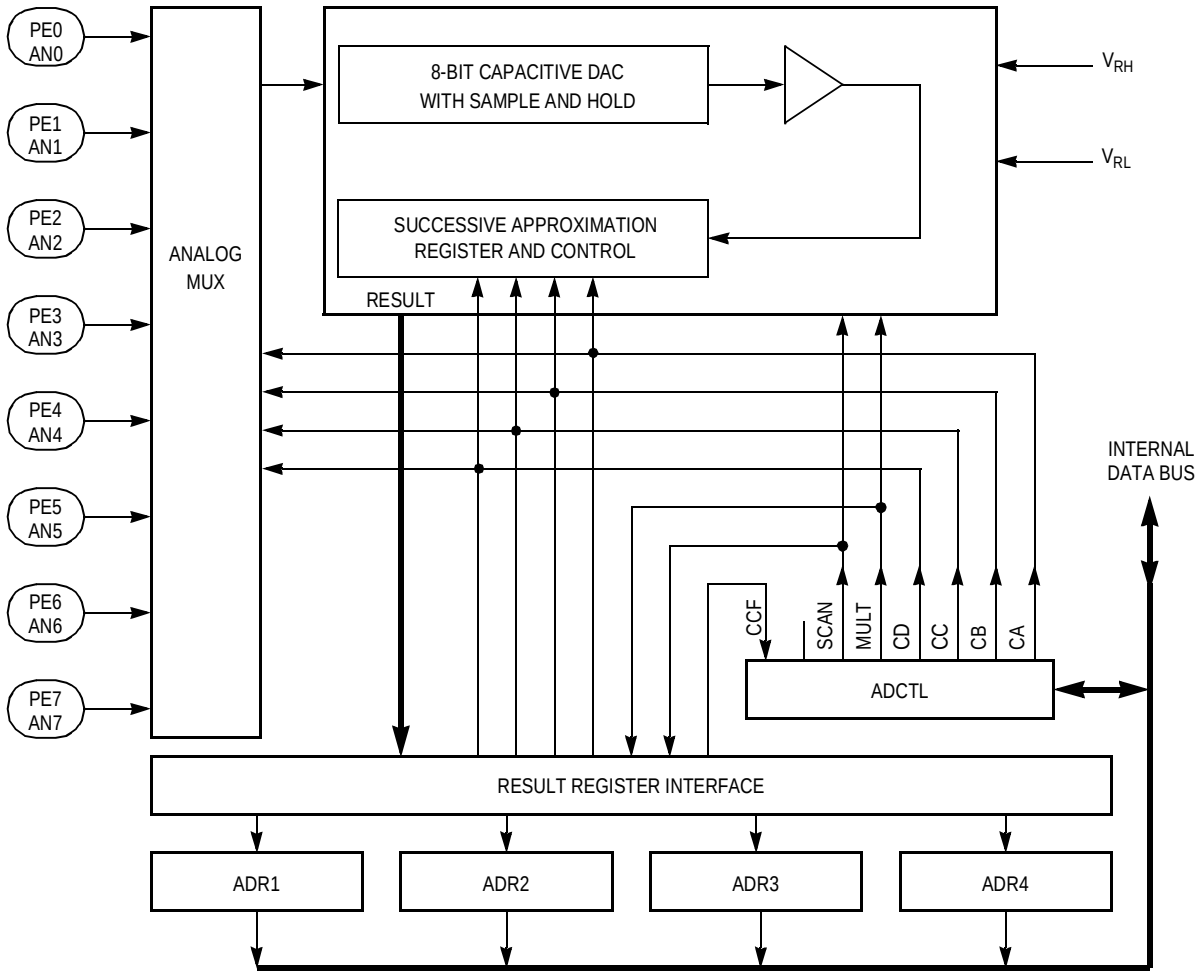

Figure 10-1. A/D Converter Block Diagram

Table 11-4. Chip Select Control Parameter Summary

CSIO	Enable	IOEN in CSCTL	1 = enabled, 0 = disabled(1)
	Valid	IOCSA in CSCTL	1 = address valid, 0(1) = E high
	Polarity	IOPL in CSCTL	1 = active high, 0 = active low(1)
	Size	IOSZ in CSCTL	1 = 4 K ($1000–$1FFF) 0 = 8 K ($0000–$1FFF)(1)
	Start address	Fixed (see size)	
	Stretch	IO1S[A:B] in CSCSTR	0(1), 1, 2, or 3 E clocks
CSPROG	Enable	PCSEN in CSCTL	1 = enabled(1), 0 = disabled
	Valid	Fixed (address valid)	
	Polarity	Fixed (active low)	
	Size	PCSZ[A:B] in CSCTL	0:0 = 64 K ($0000–$FFFF)(1) 0:1 = 32 K ($8000–$FFFF) 1:0 = 16 K ($C000–$FFFF) 1:1 = 8 K ($E000–$FFFF)
	Start address	Fixed (see size)	
	Stretch	PCS[A:B] in CSCSTR	0(1), 1, 2, or 3 E clocks
	Priority	GCSPR in CSCTL	1 = CSGPx above CSPROG 0(1) = CSPROG above CSGPx
CSGP1, CSGP2	Enable	Set size to 0K to disable	
	Valid	G1AV in GPCS1C G2AV in GPCS2C	1 = address valid, 0 = E high(1)
	Polarity	G1POL in GPS1C G2POL in GPS2C	1 = active high, 0 = active low(1)
	Size	G1SZ[A:D] in GPCS1C G1SZ[A:D] in GPCS2C	2 K to 512 K in nine steps 0K = disabled(1) can also follow memory expansion window 1 or window 2
	Start address	GPCS1A GPCS2A	
	Stretch	CSCSTR	0(1), 1, 2, or 3 E clocks
	Other	G1DG2 in GPCS1C	Allows CSGP1 and CSGP2 to be logically ORed and driven out the CSGP2 pin
		G1DPC in GPCS1C	Allows CSGP1 and CSPROG to be logically ORed and driven out the CSPROG pin
		G2DPC in GPCS2C	Allows CSGP2 and CSPROG to be logically ORed and driven out the CSPROG pin.
		MXGS2 in MMSIZ	Allows CSGP2 to follow either 64 K CPU addresses or 512K expansion addresses
		MXGS1 in MMSIZ	Allows CSGP1 to follow either 64 K CPU addresses or 512K expansion addresses

1. Configuration at reset

Address: $005A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	IOSA	IOSB	GP1SA	GP1SB	GP2SA	GP2SB	PCSA	PCSB
Reset:	0	0	0	0	0	0	0	0

Figure 11-14. Chip Select Clock Stretch Register (CSCSTR)

IOS[A:B] — CSIO Stretch Select Bits

GP1S[A:B] — CSGP1 Stretch Select Bits

GP2S[A:B] — CSGP2 Stretch Select Bits

PCS[A:B] — CSPROG Stretch Select Bits

Each of these pairs of bits contain the binary number of cycles of clock stretch, as shown in **Table 11-9**.

Table 11-9. CSCSTR Bits Versus Clock Cycles

Bit [A:B]	Clock Stretch
0 0	None
0 1	1 cycle
1 0	2 cycles
1 1	3 cycles

11.5 Memory Expansion Examples

The first example, shown in **Figure 11-15** contains a system with 64 Kbytes of external memory to be accessed through a single 8-Kbyte window. To access eight Kbytes, or 2^{13} address locations, the CPU will need 13 address lines, ADDR[12:0]. The number of memory banks needed is the total memory, 64 Kbytes divided by the window size, eight Kbytes. This yields eight memory banks, or 2^3. Thus, three expansion lines are required, so expansion address lines XA[15:13] replace CPU address lines ADDR[15:13]. **Figure 1-1** shows a memory map and schematic drawing of this system.

Mechanical Data

The diagrams included in this section show the latest package specifications available at the time of this publication. To make sure that you have the latest information, contact one of the following:

- Local Motorola Sales Office
- World Wide Web at http://www.motorola.com/semiconductors

Follow the World Wide Web on-line instructions to retrieve the current mechanical specifications.