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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	4MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	37
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	640 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.29x29.29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc11k1vfne4

Section 12. Electrical Characteristics

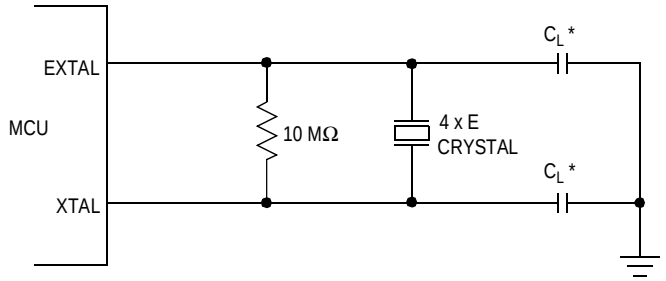
Figure	Title	Page

Section 2. Pin Description

2.1 Contents

2.2 Introduction

The M68HC11K Family is available in a variety of packages, as shown in **Table 1-1. M68HC11K Family Devices**. Most pins on this MCU serve two or more functions, as described in this section. Pin assignments for the various package types are shown in **Figure 2-1**, **Figure 2-2**, **Figure 2-3**, and **Figure 2-4**.



* This value includes all stray capacitances.

Figure 2-6. Common Crystal Connections

2.6 XOUT

The XOUT pin provides a buffered clock signal if enabled to synchronize external devices with the MCU. See **4.9 XOUT Pin Control**.

NOTE: *This signal is not present on the 80-pin M68HC(7)11K device QFP package.*

2.7 E-Clock Output (E)

The internally generated instruction cycle clock, or E clock, is available on the E pin as a timing reference. Its frequency is one fourth the input frequency at the XTAL and EXTAL pins. The E clock is low during the address portion of a bus cycle and high during the data access portion of the bus cycle. All clocks, including the E clock, are halted when the MCU is in stop mode. The E-pin driver can be turned off in single-chip modes to reduce radio frequency interference (RFI) and current consumption.

2.8 Interrupt Request ($\overline{\text{IRQ}}$) and Non-Maskable Interrupt ($\overline{\text{XIRQ}}$)

The MCU provides two pins for applying asynchronous interrupt requests. Interrupts applied to the $\overline{\text{IRQ}}$ pin can be masked by setting the I bit in the condition code register (CCR), which can be set or cleared by software at any time. Triggering is level sensitive by default, which is

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$003A	Arm/Reset COP Timer Circuitry Register (COPRST) See page 110.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$003B	EEPROM Programming Control Register (PPROG) See page 91.	Read:	ODD	EVEN	LVPI	BYTE	ROW	ERASE	EELAT	EEPGM
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$003C	Highest Priority I-Bit Interrupt and Misc. Register (HPRIO) See pages 80, 123	Read: Write:	RBOOT	SMOD	MDA	PSEL4	PSEL3	PSEL2	PSEL1	PSEL0
		Reset:	—	—	—	0	0	1	1	0
$003D	RAM and I/O Mapping Register (INIT)(1) See page 84.	Read: Write:	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0
		Reset:	0	0	0	0	0	0	0	0

1. Can only be written once in first 64 cycles out of reset in normal modes

$003E	Test 1 Register (TEST1)	Read: Write:	TILOP	0	OCCR	CBYP	DISR	FCM	FCOP	0
		Reset:	0	0	0	0	0	0	0	0
$003F	System Configuration Register (CONFIG) See pages 88, 101, 108, 147	Read: Write:	ROMAD	1	CLKX	PAREN	NOSEC	NOCOP	ROMON	EEON
		Reset:	—	1	—	—	1	—	—	—
$0040 to $0055	Reserved		R	R	R	R	R	R	R	R
$0056	Memory Mapping Size Register (MMSIZ)(2) See pages 235, 243	Read: Write:	MXGS2	MXGS1	W2SZ1	W2SZ0	0	0	W1SZ1	W1SZ0
		Reset:	0	0	0	0	0	0	0	0
$0057	Memory Mapping Window Base Register (MMWBR)(2) See page 236.	Read: Write:	W2A15	W2A14	W2A13	0	W1A15	W1A14	W1A13	0
		Reset:	0	0	0	0	0	0	0	0

2. Not available on M68HC11KS devices

= Unimplemented R = Reserved U = Undefined

Figure 4-1. Register and Control Bit Assignments (Sheet 7 of 11)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0077	SCI Data Register (SCDR) See page 165.	Read: Write:	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0
		Reset:	Undefined after reset							
$0078	Reserved		R	R	R	R	R	R	R	R
to										
$007B	Reserved		R	R	R	R	R	R	R	R
$007C	Port H Data Register (PORTH) See page 146.	Read: Write:	PH7(1)	PH6(1)	PH5(1)	PH4(1)	PH3	PH2	PH1	PH0
		Reset:	Undefined after reset							
$007D	Port H Data Direction Register (DDRH) See page 146.	Read: Write:	DDH7(1)	DDH6(1)	DDH5(1)	DDH4(1)	DDH3	DDH2	DDH1	DDH0
		Reset:	0	0	0	0	0	0	0	0
$007E	Port G Data Register (PORTG) See page 145.	Read: Write:	PG7	PG6(1)	PG5(1)	PG4(1)	PG3(1)	PG2(1)	PG1(1)	PG0(1)
		Reset:	Undefined after reset							
$007F	Port G Data Direction Register (DDRG) See page 145.	Read: Write:	DDG7	DDG6(1)	DDG5(1)	DDG4(1)	DDG3(1)	DDG2(1)	DDG1(1)	DDG0(1)
		Reset:	0	0	0	0	0	0	0	0

1. Not available on M68HC11KS devices

= Unimplemented R = Reserved U = Undefined

Figure 4-1. Register and Control Bit Assignments (Sheet 11 of 11)

Table 4-5. RAM Mapping

RAM[3:0]	Address(1)	Address(2)
0000	$0080–$037F(3)	$0000–$02FF
0001	$1080–$137F	$1000–$12FF
0010	$2080–$237F	$2000–$22FF
0011	$3080–$337F	$3000–$32FF
0100	$4080–$437F	$4000–$42FF
0101	$5080–$537F	$5000–$52FF
0110	$6080–$637F	$6000–$62FF
0111	$7080–$737F	$7000–$72FF
1000	$8080–$837F	$8000–$82FF
1001	$9080–$937F	$9000–$92FF
1010	$A080–$A37F	$A000–$A2FF
1011	$B080–$B37F	$B000–$B2FF
1100	$C080–$C37F	$C000–$C2FF
1101	$D080–$D37F	$D000–$D2FF
1110	$E080–$E37F	$E000–$E2FF
1111	$F080–$F37F	$F000–$F2FF

1. RAM[3:0] = REG[3:0]: On the [7]11KS2, RAM address range is $x080–$x47F.
2. RAM[3:0] ≠ REG[3:0]: On the [7]11KS2, RAM address range is $x000–$x37F.
3. Default locations out of reset

registers to default values, then receives data from an external host and programs it into the EPROM. The value in the X index register determines programming delay time. The value in the Y index register is a pointer to the first address in EPROM to be programmed. The default starting address is $8000 for the M68HC11KS2.

When the utility program is ready to receive programming data, it sends the host a $FF character and waits for a reply. When the host sees the $FF character, it sends the EPROM programming data, starting with the first location in the EPROM array. After the MCU receives the last byte to be programmed and returns the corresponding verification data, it terminates the programming operation by initiating a reset. Refer to the Motorola application note entitled *MC68HC11 Bootstrap Mode,* document order number AN1060/D.

4.7.2 Programming the EPROM from Memory

In this method, software programs the EPROM one byte at a time. Each byte is read from memory, then latched and programmed into the EPROM using the EPROM programming control register (EPROG). This procedure can be done in any operating mode.

Address: $002B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	R	0	ELAT	EXCOL	EXROW	0	0	EPGM
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 4-8. EPROM Programming Control Register (EPROG)

MBE — Multiple-Byte Program Enable Bit

MBE is for factory use only and is accessible only in special test mode. When MBE is set, the MCU ignores address bit 5, so that bytes with ADDR5 = 0 and ADDR5 = 1 both get programmed with the same data.

0 = Normal programming
1 = Multiple-byte programming enabled

The procedures for both writing and erasing involve these five steps:

1. **Set the EELAT bit in PPROG**. If erasing, also set the ERASE bit and the appropriate BYTE and ROW bits.
2. **Write data to the appropriate EEPROM address**. If erasing, any data will work. To erase a row, write to any location in the row. To erase the entire EEPROM, write to any location in the array. This step is done before applying the programming voltage because setting the EEPGM bit inhibits writes to EEPROM addresses.
3. **Set the EEPGM bit in PPROG,** keeping EELAT set. If erasing, also set the ERASE bit and the appropriate BYTE and ROW bits.
4. **Delay for 10 ms**.
5. **Clear the PPROG register** to turn off the high voltage and reconfigure the EEPROM address and data buses for normal operation.

The following examples demonstrate programming a single EEPROM byte, erasing the entire EEPROM, erasing a row (16 bytes), and erasing a single byte.

4.8.2.1 EEPROM Programming

On entry, accumulator A contains the data to be written and X points to the address to be programmed.

```
EEPROG   LDAB    #$02
         STAB    $003B    Set EELAT bit to enable EEPROM
                          latches.
         STAA    $0,X     Store data to EPROM address
         LDAB    #$03
         STAB    $002B    Set EPGM bit with ELAT=1
                          to enable EEPROM programming voltage
         JSR     DLY10    Delay 10 ms
         CLR     $003B    Turn off programming voltage and set
                          to READ mode
```

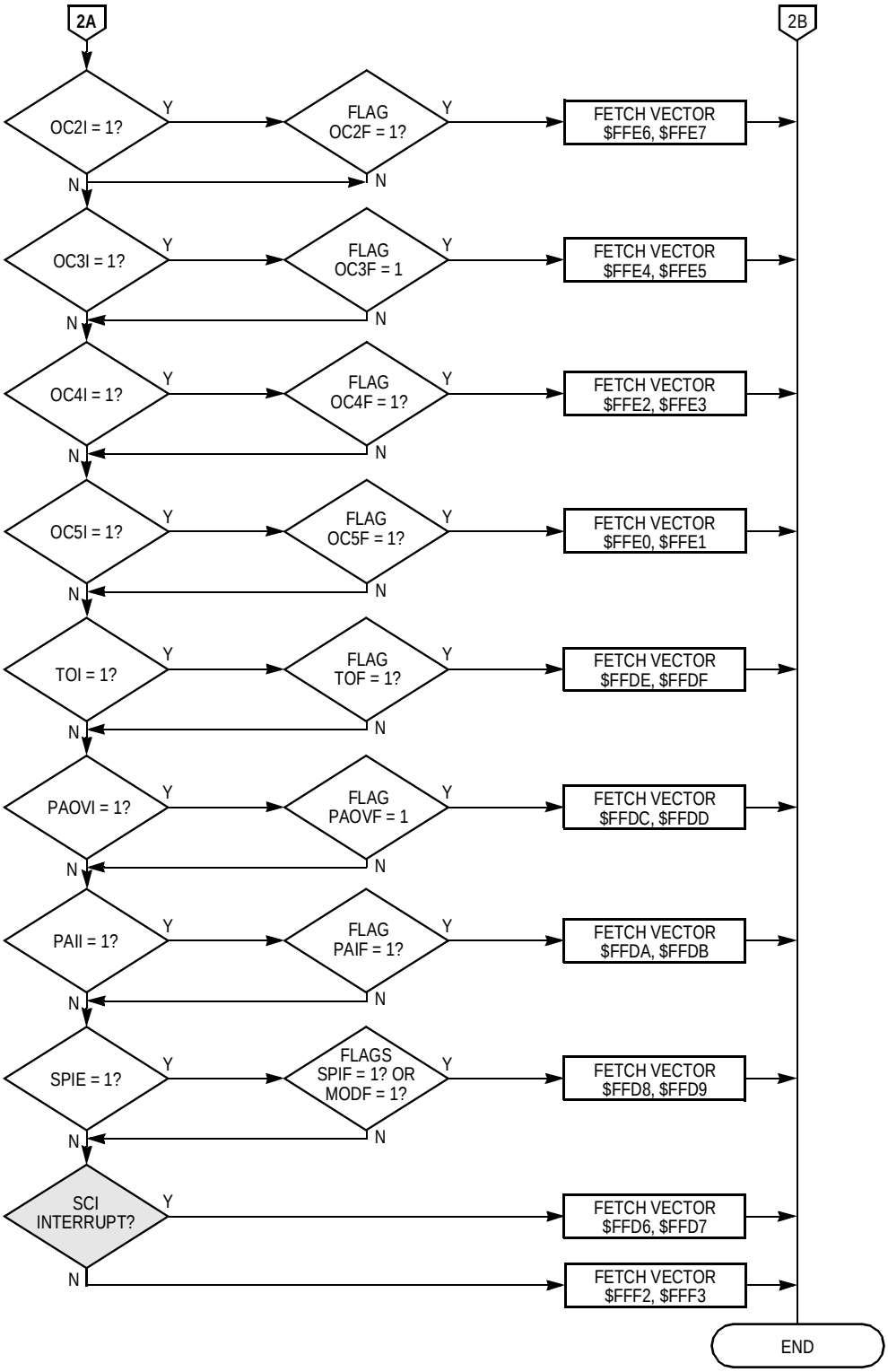


Figure 5-9. Interrupt Priority Resolution (Sheet 2 of 2)

6.3 Port A

Port A provides the I/O lines for the timer functions and pulse accumulator. The eight port A bits (PA[7:0]) are configured as high-impedance general-purpose inputs out of reset. Writes to DDRA can change any of the bits to outputs. Writes to timer registers enable the various timer functions (see **Section 9. Timing System**).

Address: $0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Reset:	Undefined after reset							
Alternate Pin Function:	PAI	OC2	OC3	OC4	IC4/OC5	IC1	IC2	IC3
And/or:	OC1	OC1	OC1	OC1	OC1	—	—	—

Figure 6-1. Port A Data Register (PORTA)

Address: $0001

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0
Reset:	0	0	0	0	0	0	0	0

Figure 6-2. Port A Data Direction Register (DDRA)

DDA[7:0] — Data Direction for Port A Bits

0 = Input

1 = Output

6.8 Port F

The state of port F (PF[7:0]) at reset is mode dependent. In single-chip or bootstrap modes, port F pins are high-impedance inputs with selectable internal pullup resistors (see **6.11 Internal Pullup Resistors**). Writes to DDRF can change any of the bits to outputs. In expanded or test modes, port F pins provide low-order address lines, ADDR[7:0], for external memory devices.

Address: $0005

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
Reset:	Undefined after reset							
Single-Chip/Boot:	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
Expanded/Test:	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

Figure 6-11. Port F Data Register (PORTF)

Address: $0003

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0
Reset:	0	0	0	0	0	0	0	0

Figure 6-12. Port F Data Direction Register (DDRF)

DDF[7:0] — Data Direction for Port F Bits

0 = Input

1 = Output

7.6 Wakeup Feature

The wakeup feature reduces SCI service overhead in multiple receiver systems. If a system generates address information at the beginning of every message, each receiver can determine whether or not it is the intended recipient of a message by evaluating the first character(s) through software.

If the message is intended for a different receiver, the SCI can be placed in a sleep mode so that the rest of the message will not generate requests for service. It does this by setting the RWU (receiver wakeup) bit in SCI control register 2 (SCCR2), which inhibits all receiver-related status flags (RDRF, IDLE, OR, NF, FE, PF, and RAF). A new message clears the receiver's RWU bit, enabling it to evaluate the new address information. Although RWU can be cleared by a software write to SCCR2, this is rarely done because hardware clears RWU automatically.

Two methods of wakeup are available:

- Idle line wakeup — A sleeping receiver wakes up as soon as the RxD line becomes idle (for example, in a logic 1 state for at least one frame time). A system using this type of wakeup must provide at least one character time of idle between messages to wake up sleeping receivers and must not allow any idle time between characters within a message.
- Address mark wakeup — Uses the most significant bit (MSB) to distinguish address characters (MSB = 1) from data characters (MSB = 0). A sleeping receiver wakes up whenever it receives an address character. Unlike the idle line method, address mark wakeup allows idle periods within messages and does not require idle time between messages. However, message processing is less efficient because the start bit of each character must be evaluated.

9.6.2 Timer Input Capture 4/Output Compare 5 Register

	Bit 7	6	5	4	3	2	1	Bit 0
Address:	$001E — TI4/O5 (High)							
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1
Address:	$001F — TI4/O5 (Low)							
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1

Figure 9-14. Timer Input Capture 4/Output Compare 5 Register (TI4/O5)

Functions as the output compare register for OC5 when PA3 is configured for output compare 5. This register is 16-bit read-write. It can be used as a storage location if it is not used for output compare or input capture.

9.6.3 Timer Interrupt Flag 1 Register

Address: $0023

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F
Reset:	0	0	0	0	0	0	0	0

Figure 9-15. Timer Interrupt Flag 1 Register (TFLG1)

Clear each flag by writing a 1 to the corresponding bit position.

OCxF — Output Compare x Flag

Set each time the counter matches output compare x value.

I4/O5F — Input Capture 4/Output Compare 5 Flag

Set each time the counter matches output compare 5 value if OC5 is enabled.

Section 10. Analog-to-Digital (A/D) Converter

10.1 Contents

10.2 Introduction

The analog-to-digital (A/D) system in M68HC11 microcontrollers is an 8-channel, 8-bit, multiplexed input converter. It employs a successive approximation technique with an all-capacitive charge redistribution system that does not require external sample-and-hold circuits. A/D converter timing can be synchronized either to the E clock or an internal resistor-capacitor (RC) oscillator. Separate power supply inputs, AV_{DD} and AV_{SS}, allow independent bypassing for noise immunity.

11.4.3.4 General-Purpose Chip Select 2 Address Register

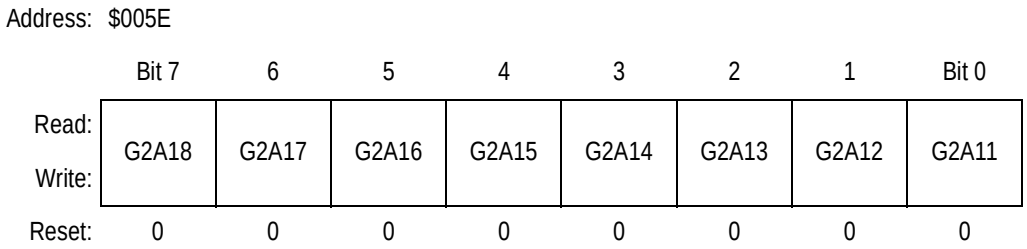


Figure 11-10. General-Purpose Chip Select 2 Address Register (GPCS2A)

G2A[18:11] — General-Purpose Chip Select 2 Address Bits

They select the starting address of GPCS2. Refer to **Table 11-7**.

11.4.3.5 General-Purpose Chip Select 2 Control Register

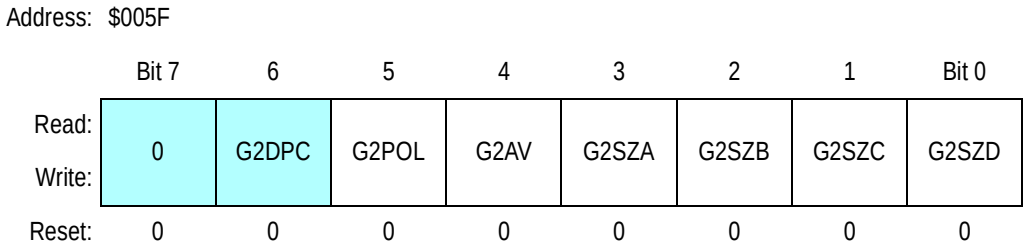


Figure 11-11. General-Purpose Chip Select 2 Control Register (GPCS2C)

G2POL — General-Purpose Chip Select 2 Polarity Select Bit

0 = CSGP2 active low
1 = CSGP2 active high

G2AV — General-Purpose Chip Select 2 Address Valid Select Bit

0 = CSGP2 is valid during E high time.
1 = CSGP2 is valid during address valid time.

G2SZ[A:D] — General-Purpose Chip Select 2 Size Bits

They select the range of GPCS2. Refer to **Table 11-7**.

11.4.4.1 General-Purpose Chip Select 1 Control Register

Address: $005D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	G1DG2	G1DPC	G1POL	G1AV	G1SZA	G1SZB	G1SCC	G1SZD
Reset:	0	0	0	0	0	0	0	0

Figure 11-12. General-Purpose Chip Select 1 Control Register (GPCS1C)

G1DG2 — GPCS 1 Drives GPCS 2 Bit
0 = CSGP1 does not affect CSGP2.
1 = CSGP1 and CSGP2 are ORed and driven out of the CSGP2.

G1DPC — General-Purpose Chip Select 1 Drives Program Chip Select Bit
0 = CSGP1 does not affect CSPROG.
1 = CSGP1 and CSPROG are ORed and driven out of the CSPROG.

11.4.4.2 General-Purpose Chip Select 2 Control Register

Address: $005F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	G2DPC	G2POL	G2AV	G2SZA	G2SZB	G2SZC	G2SZD
Reset:	0	0	0	0	0	0	0	0

Figure 11-13. General-Purpose Chip Select 2 Control Register (GPCS2C)

G2DPC — General-Purpose Chip Select 2 Drives Program Chip Select Bit
0 = Does not affect program chip select
1 = CSGP2 and CSPROG are ORed and driven out of the CSPROG pin.

Table 11-8. One Chip Select Driving Another

G1DG2	G1DPC	G2DPC	Program CS Pin is Asserted When Address is in:	General 2 CS Pin is Asserted When Address is in:	General 1 CS Pin is Asserted When Address is in:
0	0	0	A valid program area	A valid general 2 area	A valid general 1 area
0	0	1	A valid program or general 2 area	Never asserted	A valid general 1 area
0	1	0	A valid program or general 1 area	A valid general 2 area	Never asserted
0	1	1	A valid program or general 1 or 2 area	Never asserted	Never asserted
1	0	0	A valid program area	A valid general 2 or general 1 area	Never asserted
1	0	1	A valid program or general 2 area	Never asserted	A valid general 1 area
1	1	0	A valid program or general 1 area	A valid general 2 area	Never asserted
1	1	1	A valid program or general 1 or 2 area	Never asserted	Never asserted

11.4.5 Clock Stretching

Chip select and bus control signals are synchronized with the external E clock. To accommodate devices that are slower than the MCU, the E clock can be stretched when a chip select is asserted so that it remains high for one to three extra bus cycles. During this stretch, which can occur only during accesses to addresses in that chip select's address range, the other clocks continue running normally, maintaining the integrity of the timers and baud generators. Each chip select has two associated bits in the chip-select clock stretch (CSCSTR) register that set its clock stretching from zero (disabled) to three cycles.

12.12 Serial Peripheral Interface Timing

Num	Characteristic[1]	Symbol	Min	Max	Unit
	Operating frequency Master Slave	$f_{op(m)}$ $f_{op(s)}$	$f_o/128$ dc	$f_o/2$ f_o	MHz
1	Cycle time Master Slave	$t_{cyc(m)}$ $t_{cyc(s)}$	2 1	128 —	t_{cyc}
2	Enable lead time Slave	$t_{Lead(s)}$	1	—	t_{cyc}
3	Enable lag time Slave	$t_{Lag(s)}$	1	—	t_{cyc}
4	Clock (SCK) high time Master Slave	$t_{w(SCKH)m}$ $t_{w(SCKH)s}$	$t_{cyc} – 25$ $1/2\ t_{cyc} – 25$	$64\ t_{cyc}$ —	ns
5	Clock (SCK) low time Master Slave	$t_{w(SCKL)m}$ $t_{w(SCKL)s}$	$t_{cyc} – 25$ $1/2\ t_{cyc} – 25$	$64\ t_{cyc}$ —	ns
6	Data setup time (inputs) Master Slave	$t_{su(m)}$ $t_{su(s)}$	30 30	— —	ns
7	Data hold time (inputs) Master Slave	$t_{h(m)}$ $t_{h(s)}$	30 30	— —	ns
8	Slave access time (time to data active from high-impedance state)	t_a	0	40	ns
9	Slave disable time (hold time to high-impedance state)	t_{dis}	—	50	ns
10	Data valid (after enable edge)[2]	$t_{v(s)}$	—	50	ns
11	Data hold time (outputs) (after enable edge)	t_{ho}	0	—	ns

1. V_{DD} = 4.5 to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H. All timing measurements refer to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Capacitive load on all SPI pins is 200 pF.