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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | HC11 |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | SCI, SPI |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 62 |
| Program Memory Size | 24KB (24K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | 640 x 8 |
| RAM Size | 768 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 8x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-QFP |
| Supplier Device Package | 80-QFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc711k4cfu4 |

The MODB pin is grounded to select special modes, and has no function after reset. To select the normal operating modes (single-chip and expanded) the MODB pin is pulled to a logic high level. Connecting MODB to a voltage source other than $V_{DD}$ enables it to function as a battery backup input, $V_{STBY.}$ When $V_{DD}$ drops more than one MOS threshold (about 0.7 volts) below the voltage at $V_{STBY}$, the MCU's RAM and part of the reset logic are powered from $V_{STBY}$ rather than $V_{DD}$. Reset must be driven low before $V_{DD}$ is removed and must remain low until $V_{DD}$ has been restored to a valid level. The extra hardware required to utilize $V_{STBY}$ may be justified in certain applications where a significant amount of external circuitry operates from $V_{DD}$. **Figure 2-9** shows a suggested circuit employing the $V_{STBY}$ pin.

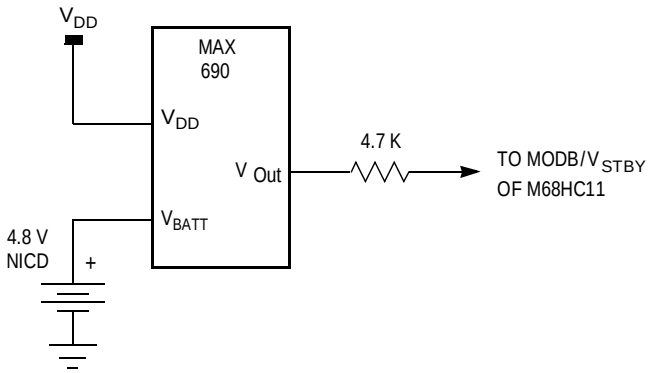



**Figure 2-9. MODB/$V_{STBY}$ Connection**

## 2.10 $V_{RH}$ and $V_{RL}$

These pins provide the reference voltage for the analog-to-digital converter.

## 2.11 Port Signals

The K series contains 62 input/output lines arranged in eight ports, A through H; all ports are eight bits except port D, which is six bits. The KS series drops seven lines from port G and four from port H, for a total of

| Addr. | Register Name | | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $0058 | Memory Mapping Window 1 Control Register (MM1CR)(1) See page 237. | Read: Write: | 0 | X1A18 | X1A17 | X1A16 | X1A15 | X1A14 | X1A13 | 0 |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $0059 | Memory Mapping Window 2 Control Register (MM2CR)(1) See page 237. | Read: Write: | 0 | X2A18 | X2A17 | X2A16 | X2A15 | X2A14 | X2A13 | 0 |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $005A | Chip Select Clock Stretch Register (CSCSTR)(1) See page 249. | Read: Write: | IOSA | IOSB | GP1SA | GP1SB | GP2SA | GP2SB | PCSA | PCSB |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $005B | Chip Select Control Register (CSCTL)(1) See pages 240, 241 | Read: Write: | IOEN | IOPL | IOCSA | IOSZ | GCSPR | PCSEN | PCSZA | PCSZB |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| $005C | General-Purpose Chip Select 1 Address Register (GPCS1A)(1) See page 243. | Read: Write: | G1A18 | G1A17 | G1A16 | G1A15 | G1A14 | G1A13 | G1A12 | G1A11 |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $005D | General-Purpose Chip Select 1 Control Register (GPCS1C)(1) See pages 244, 247 | Read: Write: | G1DG2 | G1DPC | G1POL | G1AV | G1SZA | G1SZB | G1SZC | G1SZD |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $005E | General-Purpose Chip Select 2 Address Register (GPCS2A)(1) See page 245. | Read: Write: | G2A18 | G2A17 | G2A16 | G2A15 | G2A14 | G2A13 | G2A12 | G2A11 |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $005F | General-Purpose Chip Select 2 Control Register (GPCS2C)(1) See pages 245, 247 | Read: Write: | 0 | G2DPC | G2POL | G2AV | G2SZA | G2SZB | G2SZC | G2SZD |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $0060 | Pulse Width Modulation Timer Clock Select Register (PWCLK) See page 213. | Read: Write: | CON34 | CON12 | PCKA2 | PCKA1 | 0 | PCKB3 | PCKB2 | PCKB1 |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $0061 | Pulse Width Modulation Timer Polarity Register (PWPOL) See page 215. | Read: Write: | PCLK4 | PCLK3 | PCLK2 | PCLK1 | PPOL4 | PPOL3 | PPOL2 | PPOL1 |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

1. Not available on M68HC11KS devices

= Unimplemented R = Reserved U = Undefined

**Figure 4-1. Register and Control Bit Assignments (Sheet 8 of 11)**

### 4.6.1 Control Registers and RAM

Out of reset, the 128-byte register block is mapped to $0000 and the 768-byte RAM (1 Kbyte on the [7]11KS2) is mapped to $0080. Both the register block and the RAM can be placed at any other 4-Kbyte boundary ($x000 and $x080, respectively) by writing the appropriate value to the INIT register.

Address: $003D

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read: Write: | RAM3 | RAM2 | RAM1 | RAM0 | REG3 | REG2 | REG1 | REG0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 4-5. RAM and I/O Mapping Register (INIT)**

***NOTE:*** *INIT is writable once in normal modes and writable at any time in special modes.*

RAM[3:0] — RAM Map Position Bits

These four bits determine the position of RAM in the memory map by specifying the upper hexadecimal digit of the RAM address. Refer to **Table 4-5**.

REG[3:0] — Register Block Position Bits

These four bits determine the position of the register block in memory by specifying the upper hexadecimal digit of the block address. Refer to **Table 4-6**.

### 4.6.4 Bootloader ROM

The bootloader program occupies 512 bytes of bootstrap ROM at addresses $BE00–$BFFF. It is active only in special modes when the RBOOT bit in the HPRIO register is set.

## 4.7 EPROM/OTPROM (M68HC711K4 and M68HC711KS2)

The M68HC711K4 devices include 24 Kbytes of on-chip EPROM (OTPROM in non-windowed packages). The M68HC711KS2 has 32 Kbytes of EPROM.

The two methods available to program the EPROM are:

- Downloading data through the serial communication interface (SCI) in bootstrap or special test mode
- Programming individual bytes from memory

Before proceeding with programming:

- Ensure that the CONFIG register ROMON bit is set.
- Ensure that the $\overline{\text{IRQ}}$ pin is pulled to a high level.
- Apply 12 volts to the $\overline{\text{XIRQ}}/V_{PP}$ pin.

Program the EPROM only at room temperature. Place an opaque label over the quartz window on windowed parts after programming.

### 4.7.1 Programming the EPROM with Downloaded Data

The MCU can download EPROM data through the SCI while in the special test or bootstrap modes. This can be done either with custom software, also downloaded through the SCI, or with a built-in utility program in bootstrap ROM. In either case, the 12-volt nominal programming voltage must be present on the $\overline{\text{XIRQ}}/V_{PP}$ pin.

To use the bootstrap ROM utility, download a 3-byte program consisting of a single jump instruction to $BF00, the starting address of the resident EPROM programming utility. The utility program sets the X and Y index

The procedures for both writing and erasing involve these five steps:

1. **Set the EELAT bit in PPROG**. If erasing, also set the ERASE bit and the appropriate BYTE and ROW bits.
2. **Write data to the appropriate EEPROM address**. If erasing, any data will work. To erase a row, write to any location in the row. To erase the entire EEPROM, write to any location in the array. This step is done before applying the programming voltage because setting the EEPGM bit inhibits writes to EEPROM addresses.
3. **Set the EEPGM bit in PPROG,** keeping EELAT set. If erasing, also set the ERASE bit and the appropriate BYTE and ROW bits.
4. **Delay for 10 ms**.
5. **Clear the PPROG register** to turn off the high voltage and reconfigure the EEPROM address and data buses for normal operation.

The following examples demonstrate programming a single EEPROM byte, erasing the entire EEPROM, erasing a row (16 bytes), and erasing a single byte.

#### *4.8.2.1 EEPROM Programming*

On entry, accumulator A contains the data to be written and X points to the address to be programmed.

```
EEPROG   LDAB    #$02
         STAB    $003B    Set EELAT bit to enable EEPROM
                          latches.
         STAA    $0,X     Store data to EPROM address
         LDAB    #$03
         STAB    $002B    Set EPGM bit with ELAT=1
                          to enable EEPROM programming voltage
         JSR     DLY10    Delay 10 ms
         CLR     $003B    Turn off programming voltage and set
                          to READ mode
```

### 5.3.4.2 System Configuration Options Register 2

Address: $0038

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read: Write: | LIRDV | CWOM | STRCH(1) | IRVNE | LSBF | SPR2 | XDV1 | XDV0 |
| Reset: | 0 | 0 | 0 | — | 0 | 0 | 0 | 0 |

1. Not available on M68HC11K devices

**Figure 5-5. System Configuration Options Register 2 (OPT2)**

LIRDV — LIR Driven Bit

This bit allows power savings in expanded modes by turning off the $\overline{\text{LIR}}$ output (it has no meaning in single-chip or bootstrap modes). The $\overline{\text{LIR}}$ pin is driven low to indicate that execution of an instruction has begun. To detect consecutive instructions in a high-speed application, this signal drives high for a quarter of a cycle to prevent false triggering. An external pullup is required in expanded modes, while a hardwired $V_{SS}$ connection is possible in single-chip modes. LIRDV is reset to 0 in single-chip modes and to 1 in expanded modes.

1 = Enable $\overline{\text{LIR}}$ push-pull drive
0 = $\overline{\text{LIR}}$ not driven high on MODA/$\overline{\text{LIR}}$ pin

CWOM — Port C Wired-OR Mode Bit

For detailed information, refer to **Section 6. Parallel Input/Output**.

1 = Port C outputs are open drain.
0 = Port C operates normally.

STRCH — Stretch External Accesses Bit

When this bit is set, off-chip accesses of selected addresses are extended by one E-clock cycle to allow access to slow peripherals. The E clock stretches externally, but the internal clocks are not affected, so that timers and serial systems are not corrupted. The state of the ROMAD bit in the CONFIG register determines which address range is affected.

1 = Off-chip accesses are selectively extended by one E-clock cycle.
0 = Normal operation

to restart the system, a normal reset sequence results and all pins and registers are reinitialized.

To use the $\overline{\text{IRQ}}$ pin as a means of recovering from STOP, the I bit in the CCR must be clear ($\overline{\text{IRQ}}$ not masked). The $\overline{\text{XIRQ}}$ pin can be used to wake up the MCU from STOP regardless of the state of the X bit in the CCR, although the state of this bit does affect the recovery sequence. If X is clear ($\overline{\text{XIRQ}}$ not masked), the MCU executes a normal XIRQ service routine. If X is set ($\overline{\text{XIRQ}}$ masked or inhibited), then processing continues with the instruction that immediately follows the STOP instruction, and no $\overline{\text{XIRQ}}$ interrupt service is requested or pending.

Executing a STOP instruction requires special consideration when the clock monitor is enabled. Because the stop function halts all clocks, the clock monitor function will generate a reset sequence if it is enabled at the time the stop mode was initiated. To prevent this, clear the CME and FCME bits in the OPTION register before executing a STOP instruction to disable the clock monitor. After recovery from STOP, set the CME bit to enable the clock monitor.

Systems using the internal oscillator require a delay after restart upon leaving STOP to allow the oscillator to stabilize. If a stable external oscillator is used, the DLY control bit in the OPTION register can be used to bypass this startup delay (see **Figure 5-11**). Reset sets the DLY control bit; it can be cleared during initialization. Do not use reset to recover from STOP if the DLY is to be bypassed, since reset sets the DLY bit again, causing the restart delay. This same delay will follow a power-on reset, regardless of the state of the DLY control bit, but does not apply to a reset while the clocks are running.

Address: $0039

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read:<br>Write: | ADPLE | DSEL | IRQE(1) | DLY(1) | CME | FCME(1) | CR1(1) | CR0(1) |
| Reset: | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

1. Can be written only once in first 64 cycles out of reset in normal modes or at any time in special modes

**Figure 5-11. System Configuration Options Register (OPTION)**

## 6.2 Introduction

The M68HC11K series MCUs contain eight input/output (I/O) ports, A through H. All ports can provide general-purpose I/O (GPIO) as well as their specialized functions, as explained in **2.11 Port Signals** and summarized in **Table 6-1**.

**Table 6-1. Port Configuration**

| Port | Input Pins | Output Pins | Bidirectional Pins | Shared Functions |
|---|---|---|---|---|
| Port A | — | — | 8 | Timer |
| Port B | — | — | 8 | High-order address |
| Port C | — | — | 8 | Data bus |
| Port D | — | — | 6 | SCI and SPI |
| Port E | 8 | — | — | A/D converter |
| Port F | — | — | 8 | Low-order address |
| Port G | — | — | 8(1) | Memory expansion |
| Port H | — | — | 8(2) | Chip selects and PWM |

1. KS devices do not contain port G[6:0], so they have only one bidirectional pin on this port.
2. KS devices do not contain port H[7:4], so they have only four bidirectional pins on this port.

Each of the ports has an associated data register (PORTx). Each port, except port E, also has an associated data direction register (DDRx). When a port is configured for GPIO, its DDR determines whether port pins function as inputs or outputs. A port's special functions override the DDR when they are enabled.

Writes to any port, except port E, are stored in internal latches. The latches drive the port pins only when they are configured as general-purpose outputs.

When software reads a port pin configured for GPIO, the MCU returns the physical pin level, not the port register value. This applies to both inputs and outputs. The only exception applies to ports C and D in wired-OR mode. When they are configured as outputs, a read returns the pin driver levels.

## 6.9 Port G

The state of port G pin 7 (PG7) at reset is mode dependent. In single-chip or bootstrap modes, it is a high-impedance input; its data direction can be changed through DDRG. In expanded and special test modes, PG7 functions as the R/$\overline{W}$ line to control the direction of data flow between the MCU and external memory devices.

Port G pins (PG[6:0]) reset to high-impedance inputs in any mode. Data direction can be changed through DDRG. Port G bits [5:0] can serve as memory expansion address lines (see **11.3 Memory Expansion**) in expanded and special test modes. M68HC11KS devices do not contain these pins.

All eight port G pins have selectable internal pullup resistors (see **6.11 Internal Pullup Resistors**).

Address: $007E

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read:<br>Write: | PG7 | PG6(1) | PG5(1) | PG4(1) | PG3(1) | PG2(1) | PG1(1) | PG0(1) |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Alternate Pin Function: | R/$\overline{W}$ | — | XA18 | XA17 | XA16 | XA15 | XA14 | XA13 |

1. Not available on KS devices

**Figure 6-13. Port G Data Register (PORTG)**

Address: $007F

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read:<br>Write: | DDG7 | DDG6(1) | DDG5(1) | DDG4(1) | DDG3(1) | DDG2(1) | DDG1(1) | DDG0(1) |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

1. Not available on KS devices

**Figure 6-14. Port G Data Direction Register (DDRG)**

DDG[7:0] — Data Direction for Port G Bits
0 = Input
1 = Output

## 7.7 Short Mode Idle Line Detection

This feature can increase system communication speed by reducing the amount of time between messages. Setting the ILT bit in SCCR1 allows the SCI receiver to detect the consecutive 1s of an idle period before the stop bit of an incoming character is received. If the last few bits of the character are 1s, they are counted as the first high bits in the frame of 1s comprising the idle period following the character.

***NOTE:*** *Extra care may be needed to prevent premature detection of an idle line condition.*

## 7.8 Baud Rate Selection

The baud rate generator for the SCI includes a 13-bit modulus prescaler driven by the system crystal clock (EXTAL). Writing to the SCI baud rate register (SCBDH/L) selects the prescaler value. See **Figure 7-4**.

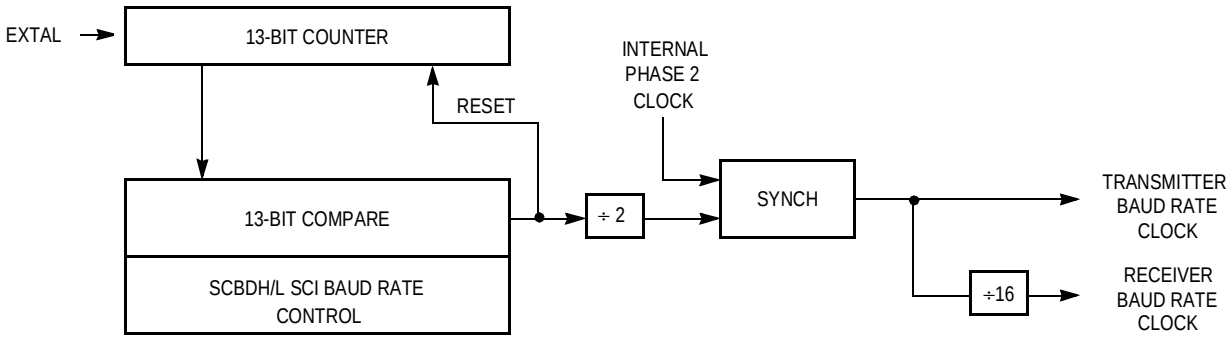



**Figure 7-4. SCI Baud Generator Circuit Diagram**

### 7.9.2 Serial Communications Control Register 1

Address $0072

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read:<br>Write: | LOOPS | WOMS | 0 | M | WAKE | ILT | PE | PT |
| Reset: | U | U | 0 | 0 | 0 | 0 | 0 | 0 |

U = Undefined

**Figure 7-7. SCI Control Register 1 (SCCR1)**

LOOPS — SCI Loop Mode Enable Bit

Both the transmitter and receiver must be enabled to use the loop mode. When the loop mode is enabled, the TxD pin is driven high (idle line state) if the transmitter is enabled.

0 = SCI transmit and receive operate normally.
1 = SCI transmit and receive are disconnected from TxD and RxD pins, and transmitter output is fed back into the receiver input.

WOMS — Wired-OR Mode for SCI Pins PD[1:0] Bits

See also **8.6.1 Serial Peripheral Control Register** for a description of the DWOM (port D wired-OR mode) bit in the serial peripheral control register (SPCR).

0 = TxD and RxD operate normally.
1 = TxD and RxD are open drains if operating as outputs.

M — Mode (SCI Word Size) Bit

0 = Start bit, 8 data bits, 1 stop bit
1 = Start bit, 9 data bits, 1 stop bit

WAKE — Wakeup Mode Bit

0 = Wake up by idle line recognition
1 = Wake up by address mark (most significant data bit set)

ILT — Idle Line Type Bit

0 = Short (SCI counts consecutive 1s after start bit.)
1 = Long (SCI counts one only after stop bit.)

### 9.7.1 Port A Data Direction Register

Address: $0001

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read: Write: | DDA7 | DDA6 | DDA5 | DDA4 | DDA3 | DDA2 | DDA1 | DDA0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 9-22. Port A Data Direction Register (DDRA)**

The pulse accumulator uses port A, bit 7 as the PAI input, but the pin can also be used as general-purpose I/O or as an output compare.

***NOTE:*** *Even when port A, bit 7 is configured as an output, the pin still drives the input to the pulse accumulator.*

DDA7 — Data Direction Control for Port A, Bit 7
0 = PA7 configured as an input
1 = PA7 configured as an output

### 9.7.2 Pulse Accumulator Control Register

Address: $0026

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read: Write: | 0 | PAEN | PAMOD | PEDGE | 0 | I4/O5 | RTR1 | RTR0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 9-23. Pulse Accumulator Control Register (PACTL)**

PAEN — Pulse Accumulator System Enable Bit
0 = Pulse accumulator disabled
1 = Pulse accumulator enabled

### 9.7.5 Pulse Accumulator Count Register

Address: $0027

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read: Write: | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 9-26. Pulse Accumulator Count Register (PACNT)**

In event counting mode, PACNT contains the count of external input events at the PAI input. In gated accumulation mode, PACNT is incremented by the pulse accumulator's E ÷ 64 clock when the PAI input is at the selected level. Counting is synchronized to the internal PH2 clock so that incrementing and reading occur during opposite half cycles. The counter is not affected by reset and can be read or written to at any time.

## 9.8 Real-Time Interrupt (RTI)

The real-time interrupt (RTI) feature generates hardware interrupts at a fixed periodic rate. The rate is determined by bits RTR[1:0] in the PACTL register, which further divide a clock running at E ÷ $2^{13}$ by 1, 2, 4 or 8. The resulting periods for various common crystal frequencies are shown in **Table 9-7**.

Every cycle of the RTI clock sets the RTIF bit in timer interrupt flag 2 (TFLG2) register. This flag can be polled to determine when RTI timeouts occur, or an interrupt can be generated if the RTII bit in the timer interrupt mask 2 (TMSK2) register is set. After reset, one entire real-time interrupt period elapses before the RTIF flag is set for the first time.

The clock source for the RTI function is a free-running clock that cannot be stopped or interrupted except by reset. The time between successive RTI timeouts is a constant that is independent of software latencies

### 11.4.3 General-Purpose Chip Selects

The general-purpose chip selects are the most flexible and programmable of the chip-select signals. They can access any memory in the expanded 1-Mbyte address space. Polarity of active state, E valid or address valid, size, and starting address are all programmable. Clock stretching can be set from zero to three cycles. Both signals can be programmed to drive $\overline{\text{CSPROG}}$, and GPCS1 can be configured to drive GPCS2. In addition, each signal can follow a window; for instance, be asserted whenever the CPU address falls within a selected memory expansion window regardless of the state of the expanded address lines.

There are two registers for each of the general-purpose chip select signals:

- The control register, GPS1C or GPS2C, determines the GPCS's active signal polarity, its valid time, which of the other chip-select signals it can drive, and either the size of the memory it enables or which window it follows.
- The address register, GPS1A or GPS2A, programs the chip-select's starting address; valid bits in this register are determined by the size of the address range selected by the control register.

In addition, the MMSIZ register contains a bit for each GPCS which determines whether it is driven by the CPU's 64-Kbyte address lines or the expansion address lines.

### 11.4.3.4 General-Purpose Chip Select 2 Address Register

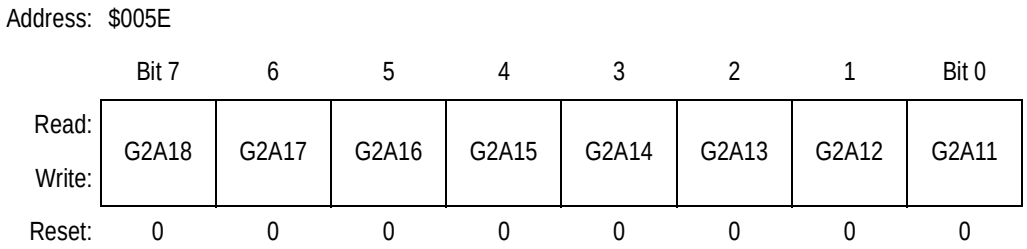



**Figure 11-10. General-Purpose Chip Select 2 Address Register (GPCS2A)**

G2A[18:11] — General-Purpose Chip Select 2 Address Bits

They select the starting address of GPCS2. Refer to **Table 11-7**.

### 11.4.3.5 General-Purpose Chip Select 2 Control Register

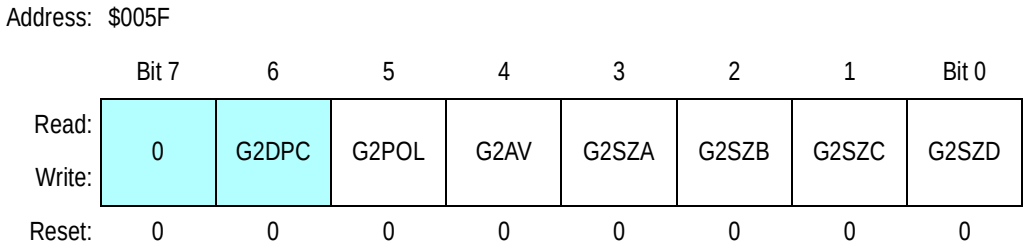



**Figure 11-11. General-Purpose Chip Select 2 Control Register (GPCS2C)**

G2POL — General-Purpose Chip Select 2 Polarity Select Bit

0 = CSGP2 active low
1 = CSGP2 active high

G2AV — General-Purpose Chip Select 2 Address Valid Select Bit

0 = CSGP2 is valid during E high time.
1 = CSGP2 is valid during address valid time.

G2SZ[A:D] — General-Purpose Chip Select 2 Size Bits

They select the range of GPCS2. Refer to **Table 11-7**.

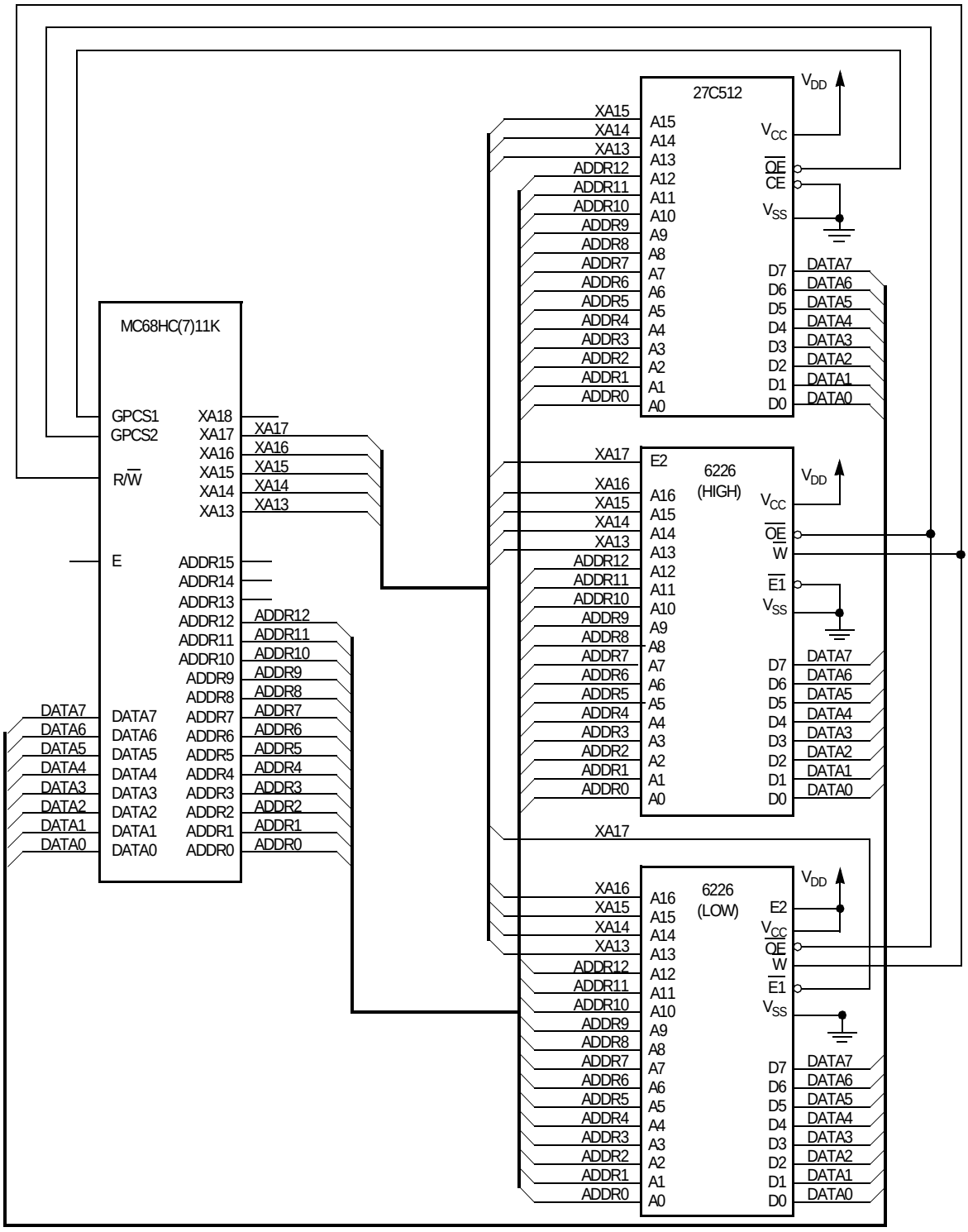
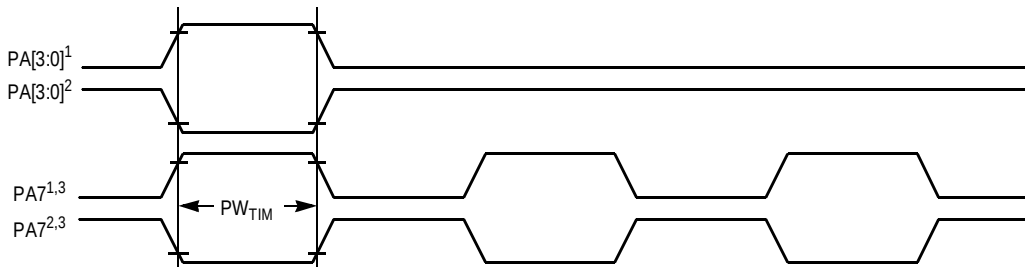



**Figure 11-16. Memory Expansion Example 2 (Sheet 2 of 2)**
**Memory Map for One 8-Kbyte Window with Eight Banks and One 16-Kbyte Window with 16 Banks of External Memory**

## 12.8 Control Timing

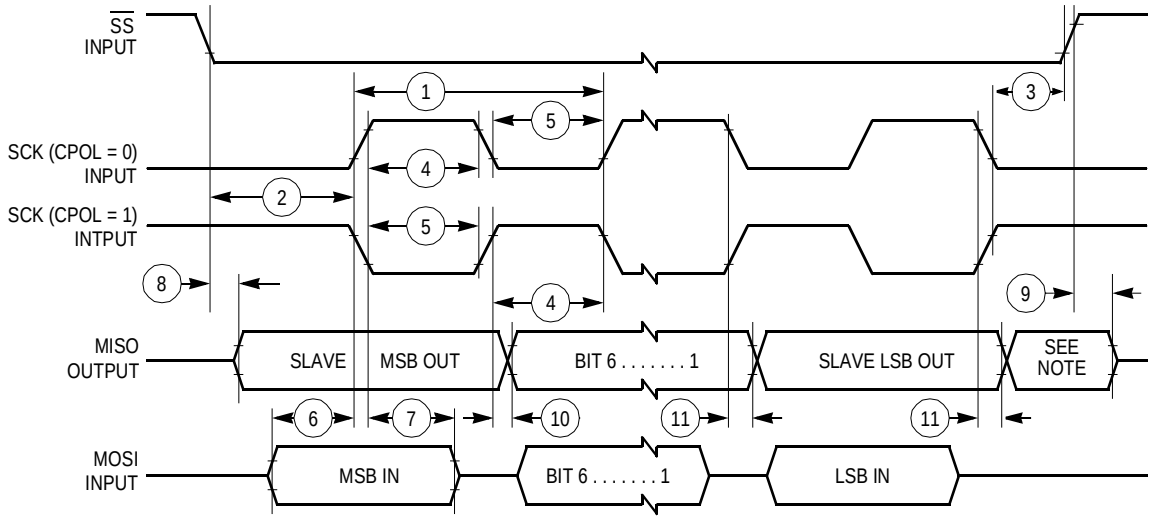
| Characteristic[1] | Symbol | 1.0 MHz | | 2.0 MHz | | 3.0 MHz | | 4.0 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Frequency of operation | $f_o$ | dc | 1.0 | dc | 2.0 | dc | 3.0 | dc | 4.0 | MHz |
| E-clock period | $t_{cyc}$ | 1000 | — | 500 | — | 333 | — | 250 | — | ns |
| Crystal frequency | $f_{XTAL}$ | — | 4.0 | — | 8.0 | — | 12.0 | — | 16.0 | MHz |
| External oscillator frequency | 4 $f_o$ | dc | 4.0 | dc | 8.0 | dc | 12.0 | dc | 16.0 | MHz |
| Processor control setup time<br>$t_{PCSU}$ = 1/4 $t_{cyc}$ + 50 ns<br>$t_{PCSU}$ = 1/4 $t_{cyc}$ + 75 ns<br>(extended voltage devices) | $t_{PCSU}$ | 300<br><br>325 | —<br><br>— | 175<br><br>200 | —<br><br>— | 133<br><br>158 | —<br><br>— | 112<br><br>— | —<br><br>— | ns |
| Reset input pulse width[2]<br>To guarantee external reset vector<br>Minimum input time[3] | $PW_{RSTL}$ | <br>16<br>1 | <br>—<br>— | <br>16<br>1 | <br>—<br>— | <br>16<br>1 | <br>—<br>— | <br>16<br>1 | <br>—<br>— | $t_{cyc}$ |
| Mode programming setup time | $t_{MPS}$ | 2 | — | 2 | — | 2 | — | 2 | — | $t_{cyc}$ |
| Mode programming hold time | $t_{MPH}$ | 10 | — | 10 | — | 10 | — | 10 | — | ns |
| Interrupt pulse width,<br>$\overline{IRQ}$ edge-sensitive mode<br>$PW_{IRQ}$ = $t_{cyc}$ + 20 ns | $PW_{IRQ}$ | 1020 | — | 520 | — | 353 | — | 270 | — | ns |
| Wait recovery startup time | $t_{WRS}$ | — | 4 | — | 4 | — | 4 | — | 4 | $t_{cyc}$ |
| Timer pulse width<br>$PW_{TIM}$ = $t_{cyc}$ + 20 ns<br>Input capture, pulse accumulator | $PW_{TIM}$ | 1020 | — | 520 | — | 353 | — | 270 | — | ns |

1. $V_{DD}$ = 4.5 to 5.5 Vdc for standard devices, $V_{SS}$ = 0 Vdc, $T_A$ = $T_L$ to $T_H$
   All timing measurements refer to 20% $V_{DD}$ and 70% $V_{DD}$, unless otherwise noted.
2. Reset is recognized during the first clock cycle it is held low. Internal circuitry then drives the pin low for eight clock cycles, releases the pin, and samples the pin level two cycles later to determine the source of the interrupt.
3. Can be pre-empted by internal reset



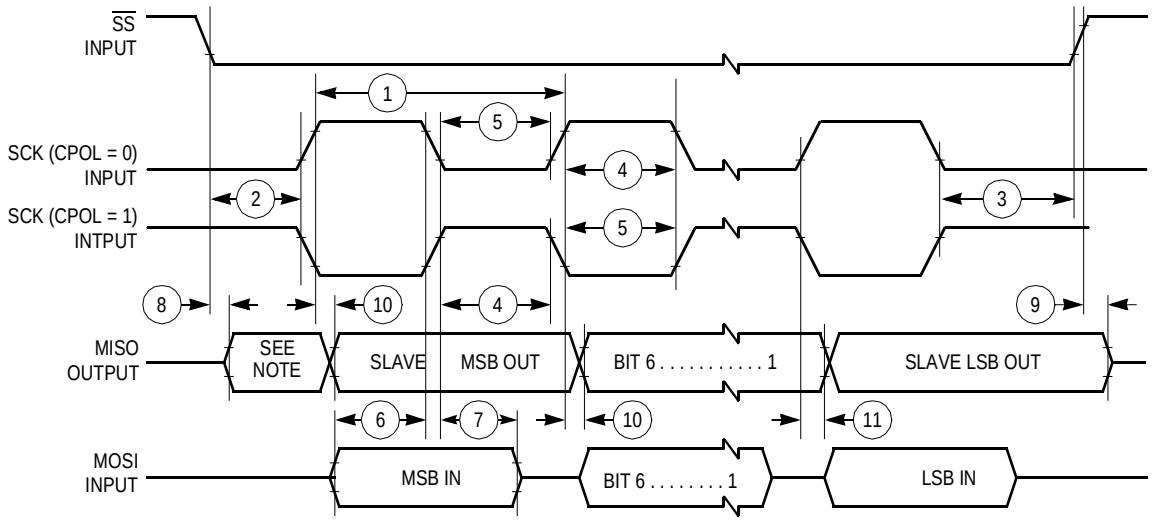

Notes:
1. Rising edge sensitive input
2. Falling edge sensitive input
3. Maximum pulse accumulator clocking rate is E-clock frequency divided by 2.

**Figure 12-2. Timer Inputs**




Note: Not defined, but normally MSB of character just received

**a) SPI Slave Timing (CPHA = 0)**




Note: Not defined, but normally LSB of character previously transmitted

**b) SPI Slave Timing (CPHA = 1)**

**Figure 12-10. SPI Timing Diagram (Sheet 2 of 2)**

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