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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	2MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	37
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	640 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68l11k1fue2

2.3 Power Supply (V_{DD}, V_{SS}, AV_{DD}, and AV_{SS})

The MCU operates from a single 5-volt (nominal) power supply. V_{DD} is the positive power input and V_{SS} is ground. There are three V_{DD}/V_{SS} pairs of pins on the K series devices and two sets on the KS devices. All devices contain a separate pair of power inputs, AV_{DD} and AV_{SS}, for the analog-to-digital (A/D) converter, so that the A/D circuitry can be bypassed independently.

Very fast signal transitions occur on the MCU pins. The short rise and fall times place high, short duration current demands on the power supply. To prevent noise problems, provide good power supply bypassing at the MCU. Also, use bypass capacitors that have good high-frequency characteristics and situate them as close to the MCU as possible. Bypass requirements vary, depending on how heavily the MCU pins are loaded.

2.4 Reset ($\overline{\text{RESET}}$)

This active-low, bidirectional control signal acts as an input to initialize the MCU to a known start-up state. It also serves as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or computer operating properly (COP) watchdog circuit.

The CPU distinguishes between internal and external reset conditions by counting the number of E-clock cycles that occur between the start of reset and the presence of a logic 1 voltage level on the reset pin. Less than two cycles indicates an internal reset; greater than two, an external reset. To prevent the device from misinterpreting the kind of reset that occurs, do not connect an external resistor-capacitor (RC) power-up delay circuit directly to the reset pin.

3.6.5 Inherent

In the inherent addressing mode, the opcode contains all required information. The operands (if any) are registers, so no memory access is required. This mode includes:

- Control instructions with no arguments
- Operations that only involve the index registers or accumulators

These instructions are one or two bytes.

3.6.6 Relative

Only branch instructions use the relative addressing mode. If the branch condition is true, the CPU adds the 8-bit signed offset following the opcode to the contents of the program counter to form the effective branch address. Otherwise, control proceeds to the next instruction. These are usually 2-byte instructions.

3.7 Instruction Set

Table 3-1 presents a detailed listing of all the M68HC11 instructions in all possible addressing modes.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$000A	Port E Data Register (PORTE) See page 143.	Read: Write:	PE7	PE6	PE5	PE4	PE3	PE2	PD1	PD0
		Reset:	Undefined after reset							
$000B	Timer Compare Force Register (CFORC) See page 201.	Read: Write:	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0
		Reset:	0	0	0	0	0	0	0	0
$000C	Output Compare 1 Mask Register (OC1M) See page 202.	Read: Write:	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0
		Reset:	0	0	0	0	0	0	0	0
$000D	Output Compare 1 Data Register (OC1D) See page 202.	Read: Write:	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0
		Reset:	0	0	0	0	0	0	0	0
$000E	Timer Counter Register High (TCNTH) See page 188.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$000F	Timer Counter Register Low (TCNTL) See page 188.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0010	Timer Input Capture 1 Register High (TIC1H) See page 192.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	Undefined after reset							
$0011	Timer Input Capture 1 Register Low (TIC1L) See page 192.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	Undefined after reset							
$0012	Timer Input Capture 2 Register High (TIC2H) See page 192.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	Undefined after reset							
$0013	Timer Input Capture 2 Register Low (TIC2L) See page 192.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	Undefined after reset							
$0014	Timer Input Capture 3 Register High (TIC3H) See page 192.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	Undefined after reset							

= Unimplemented R = Reserved U = Undefined

Figure 4-1. Register and Control Bit Assignments (Sheet 2 of 11)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001E	Timer Input Capture 4/ Output Compare 5 Reg. High (TI4H/O5H) See page 199.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	1	1	1	1	1	1	1	1
$001F	Timer Input Capture 4/ Output Compare 5 Reg. Low (TI4L/O5L) See page 199.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	1	1	1	1	1	1	1	1
$0020	Timer Control 1 Register (TCTL1) See page 200.	Read: Write:	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
		Reset:	0	0	0	0	0	0	0	0
$0021	Timer Control 2 Register (TCTL2) See page 195.	Read: Write:	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A
		Reset:	0	0	0	0	0	0	0	0
$0022	Timer Interrupt Mask 1 Register (TMSK1) See page 200.	Read: Write:	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I
		Reset:	0	0	0	0	0	0	0	0
$0023	Timer Interrupt Flag 1 Register (TFLG1) See page 199.	Read: Write:	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F
		Reset:	0	0	0	0	0	0	0	0
$0024	Timer Interrupt Mask 2 Register (TMSK2) See page 209.	Read: Write:	TOI	RTII	PAOVI	PAII	0	0	PR1(1)	PR0(1)
		Reset:	0	0	0	0	0	0	0	0

1. Can be written only once in first 64 cycles out of reset in normal modes

$0025	Timer Interrupt Flag 2 (TFLG2) See page 209.	Read: Write:	TOF	RTIF	PAOVF	PAIF	0	0	0	0
		Reset:	0	0	0	0	0	0	0	0
$0026	Pulse Accumulator Control Register (PACTL) See page 210.	Read: Write:	0	PAEN	PAMOD	PEDGE	0	I4/O5	RTR1	RTR0
		Reset:	0	0	0	0	0	0	0	0
$0027	Pulse Accumulator Count Register (PACNT) See page 208.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	Undefined after reset							

= Unimplemented R = Reserved U = Undefined

Figure 4-1. Register and Control Bit Assignments (Sheet 4 of 11)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0028	Serial Peripheral Control Register (SPCR) See page 174.	Read: Write:	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
		Reset:	0	0	0	0	0	1	U	U
$0029	Serial Peripheral Status Register (SPSR) See page 176.	Read: Write:	SPIF	WCOL	0	MODF	0	0	0	0
		Reset:	0	0	0	0	0	0	0	0
$002A	Serial Peripheral Data Register (SPDR) See page 177.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	Undefined after reset							
$002B	EPROM Programming Control Register (EPROG)(1) See page 91.	Read: Write:	R	0	ELAT	EXCOL	EXROW	0	0	EPGM
		Reset:	0	0	0	0	0	0	0	0

1. Present only in EPROM (711) devices

$002C	Port Pullup Assignment Register (PPAR) See page 147.	Read: Write:	0	0	0	0	HPPUE	GPPUE	FPPUE	BPPUE
		Reset:	0	0	0	0	1	1	1	1
$002D	Port G Assignment Register (PGAR) See page 235.	Read: Write:	0	0	PGAR5	PGAR4	PGAR3	PGAR2	PGAR1	PGAR0
		Reset:	0	0	0	0	0	0	0	0
$002E	System Configuration Options 3 Register (OPT3)(2) See page 132.	Read: Write:		SM						
		Reset:	0	0	0	0	0	0	0	0

2. Not available on M68HC11K4 devices

$002F	Reserved		R	R	R	R	R	R	R	R
$0030	Analog-to-Digital Control/Status Register (ADCTL) See page 227.	Read: Write:	CCF	0	SCAN	MULT	CD	CC	CB	CA
		Reset:	0	0	U	U	U	U	U	U
$0031	Analog-to-Digital Results Register 1 (ADR1) See page 229.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Undefined after reset							

= Unimplemented R = Reserved U = Undefined

Figure 4-1. Register and Control Bit Assignments (Sheet 5 of 11)

4.4 System Initialization

Registers and bits that control initialization and the basic operation of the MCU are protected against writes except under special circumstances. Table 4-1 lists registers that can be written only once after reset or that must be written within the first 64 cycles after reset.

Table 4-1. Registers with Limited Write Access

Operating Mode	Register Address	Register Name	Must be Written in First 64 Cycles	Write Anytime
SMOD = 0	$x024	Timer interrupt mask 2 (TMSK2)	Bits [1:0], once only	Bits [7:2]
	$x035	Block protect register (BPROT)	Clear bits, once only	Set bits only
	$x037	EEPROM mapping register (INIT2)	No, bits [7:4], once only	—
	$x038	System configuration options 2 register (OPT2)	No, bit 4, once only	See OPT2 description
	$x039	System configuration options (OPTION)	Bits [5:4], bits [2:0], once only	Bits [7:6], bit 3
	$x03C	Highest priority I-bit interrupt and miscellaneous (HPRIO)	—	See HPRIO description
	$x03D	RAM and I/O map register (INIT)	Yes, once only	—
SMOD = 1	$x024	Timer interrupt mask 2 (TMSK2)	—	All, set or clear
	$x035	Block protect register (BPROT)	—	All, set or clear
	$x037	EEPROM mapping register (INIT2)	—	Bits [7:4]
	$x038	System configuration options 2 register (OPT2)	—	See OPT2 description
	$x039	System configuration options (OPTION)	—	All, set or clear
	$x03C	Highest priority I-bit interrupt and miscellaneous (HPRIO)	—	See HPRIO description
	$x03D	RAM and I/O map register (INIT)	—	All, set or clear
	$x03F	System configuration register (CONFIG)	—	See CONFIG description

Table 4-6. Register Mapping

REG[3:0]	Address
0000	$0000–$007F(1)
0001	$1000–$107F
0010	$2000–$207F
0011	$3000–$307F
0100	$4000–$407F
0101	$5000–$507F
0110	$6000–$607F
0111	$7000–$707F
1000	$8000–$807F
1001	$9000–$907F
1010	$A000–$A07F
1011	$B000–$B07F
1100	$C000–$C07F
1101	$D000–$D07F
1110	$E000–$E07F
1111	$F000–$F07F

1. Default locations out of reset.

Since the direct addressing mode accesses RAM more quickly and efficiently than other addressing modes, many applications will find the default locations of registers and on-board RAM at the bottom of memory to be the most advantageous.

When RAM and the registers are both mapped to different 4-K boundaries, the registers are mapped at $x000–$x07F, and RAM is moved to $x000–$x2FF ($x000–x3FF for the [7]11KS2).

LSBF — Least Significant Bit (LSB) First Enable Bit

For detailed information, refer to **Section 8. Serial Peripheral Interface (SPI)**.

1 = Data is transferred LSB first.
0 = Data is transferred MSB (most significant bit) first.

SPR2 — SPI Clock Rate Selected Bit

This bit adds a divide-by-four to the SPI clock chain. For detailed information, refer to **Section 8. Serial Peripheral Interface (SPI)**.

XDV[1:0] — XOUT Clock Divide Select Bits

These bits control the frequency of the clock driven out of the XOUT pin, if enabled by the CLKX bit on the CONFIG register. See **Table 5-4**

Table 5-4. XOUT Clock Divide Select

XDV [1:0]	XOUT = EXTAL Divided By	Frequency at EXTAL = 8 MHz	Frequency at EXTAL = 12 MHz	Frequency at EXTAL = 16 MHz
0 0	1	8 MHz	12 MHz	16 MHz
0 1	4	2 MHz	3 MHz	4 MHz
1 0	6	1.3 MHz	2 MHz	2.7 MHz
1 1	8	1 MHz	1.5 MHz	2 MHz

  - All nine timer interrupts are disabled because their mask bits have been cleared.
  - The I4/O5 bit in the PACTL register is cleared to configure the I4/O5 function as OC5; however, the OM5:OL5 control bits in the TCTL1 register are clear so OC5 does not control the PA3 pin.

- Real-time interrupt (RTI)
  - The RTI enable bit in TMSK2 is cleared, masking automatic hardware interrupts.
  - The rate control bits are cleared after reset and can be initialized by software before the RTI system is enabled.
- Pulse accumulator
  - The pulse accumulator system is disabled at reset.
  - The PAI input pin defaults to a general-purpose input pin (PA7).
- Computer operating properly (COP) watchdog system
  - The COP watchdog system is enabled if the NOCOP control bit in the CONFIG register is clear and disabled if NOCOP is set.
  - The OPTION register's CR[1:0] bits are cleared, setting the COP rate for the shortest duration timeout.
- Serial communications interface (SCI)
  - At reset, the SCI baud rate control register (**7.9.1 SCI Baud Rate Control Register**) is initialized to $0004.
  - All transmit and receive interrupts are masked and both the transmitter and receiver are disabled so the port pins default to being general-purpose I/O lines.
  - The SCI frame format is initialized to an 8-bit character size.
  - The send break and receiver wake-up functions are disabled.
  - The TDRE and TC status bits in the SCI status register are both set, indicating that there is no transmit data in either the transmit data register or the transmit serial shift register.

Any single maskable interrupt can be given priority over other maskable interrupts by writing the appropriate value to the PSEL bits in the HPRIO register (see **Figure 5-7**). An interrupt that is assigned highest priority is still subject to global masking by the I bit in the CCR or by any associated local bits. Interrupt vectors are not affected by priority assignment.

Address: $003C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RBOOT	SMOD	MDA	PSEL4	PSEL3	PSEL2	PSEL1	PSEL0
Reset:	0	0	0	0	0	1	1	0

Figure 5-7. Highest Priority I-Bit Interrupt and Miscellaneous Register (HPRIO)

NOTE: *To avoid race conditions, HPRIO is designed so that bits PSEL[4:0] can be written only while the I-bit is set (interrupts are inhibited).*

PSEL[4:0] — Priority Select Bits

These bits select one interrupt source to have the highest priority, as explained in **Table 5-7**.

5.7 Reset and Interrupt Processing

This section presents flow diagrams of the reset and interrupt processes. **Figure 5-8** illustrates how the CPU begins from a reset and how interrupt detection relates to normal opcode fetches. **Figure 5-9** is an expansion of a block in **Figure 5-8** and illustrates interrupt priorities. **Figure 5-10** shows the resolution of interrupt sources within the SCI subsystem.

Ports B, F, G, and H contain on-chip pullup devices which are enabled by the port pullup assignment register (PPAR) described in **6.11 Internal Pullup Resistors**.

At reset, the ports are configured as high-impedance GPIO inputs (except for ports B, C, F, and port G pin 7 in expanded modes). The contents of the data latches is undefined. If any of the bidirectional pins are changed to outputs before writing to the associated data registers, the undefined contents will be driven on the pins. This is indicated by the letter U in the register descriptions that follow.

NOTE: *Throughout this manual, the registers are discussed by function. In the event that not all bits in a register are referenced, the bits that are not discussed are shaded.*

8.6.2 Serial Peripheral Status Register

Address: $0029

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	SPIF	WCOL	0	MODF	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 8-4. Serial Peripheral Status Register (SPSR)

SPIF — SPI Transfer Complete Flag

SPIF is set upon completion of data transfer between the processor and the external device. If SPIF goes high, and if SPIE is set, a serial peripheral interrupt is generated. To clear the SPIF bit, read the SPSR with SPIF set, then access the SPDR. Unless SPSR is read (with SPIF set) first, attempts to write SPDR are inhibited.

WCOL — Write Collision Bit

Clearing the WCOL bit is accomplished by reading the SPSR (with WCOL set) followed by an access of SPDR.

0 = No write collision
1 = Write collision

MODF — Mode Fault Bit

To clear the MODF bit, read the SPSR (with MODF set), then write to the SPCR.

0 = No mode fault
1 = Mode fault

8.6.3 Serial Peripheral Data Register

The SPDR is used when transmitting or receiving data on the serial bus. Only a write to this register initiates transmission or reception of a byte, and this only occurs in the master device. At the completion of transferring a byte of data, the SPIF status bit is set in both the master and slave devices.

A read of the SPDR is actually a read of a buffer. To prevent an overrun and the loss of the byte that caused the overrun, the first SPIF must be cleared by the time a second transfer of data from the shift register to the read buffer is initiated.

Address: $002A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	0	0	0	0	0	0	0	0

Figure 8-5. Serial Peripheral Data Register (SPDR)

A write to SPDR goes directly to the transmission shift register.

A read of the SPDR retrieves data from the read data buffer.

9.6.4 Timer Interrupt Mask 1 Register

Address: $0022

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I
Reset:	0	0	0	0	0	0	0	0

Figure 9-16. Timer Interrupt Mask 1 Register (TMSK1)

Bits in TMSK1 correspond bit for bit with flag bits in TFLG1.

OC1I–OC4I — Output Compare x Interrupt Enable Bits

If the OCxI enable bit is set when the OCxF flag bit is set, a hardware interrupt sequence is requested.

I4/O5I — Input Capture 4 or Output Compare 5 Interrupt Enable Bit

If I4/O5I is set when OC5 is enabled and the I4/O5F flag bit is set, a hardware interrupt sequence is requested.

9.6.5 Timer Control 1 Register

Address: $0020

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
Reset:	0	0	0	0	0	0	0	0

Figure 9-17. Timer Control Register 1 (TCTL1)

OM[2:5] and OL[2:5] — Output Mode and Output Level Bits

Use these bit pairs as indicated in **Table 9-4** to specify the action taken after a successful OCx compare.

register is set after the fourth conversion in a sequence to signal the availability of data in the result registers.The result registers are written during a portion of the system clock cycle when reads do not occur, so there is no conflict. A conversion sequence can repeat continuously or stop after one iteration. **Figure 10-2** shows the timing of a typical sequence. In this example, synchronization is referenced to the system E clock.

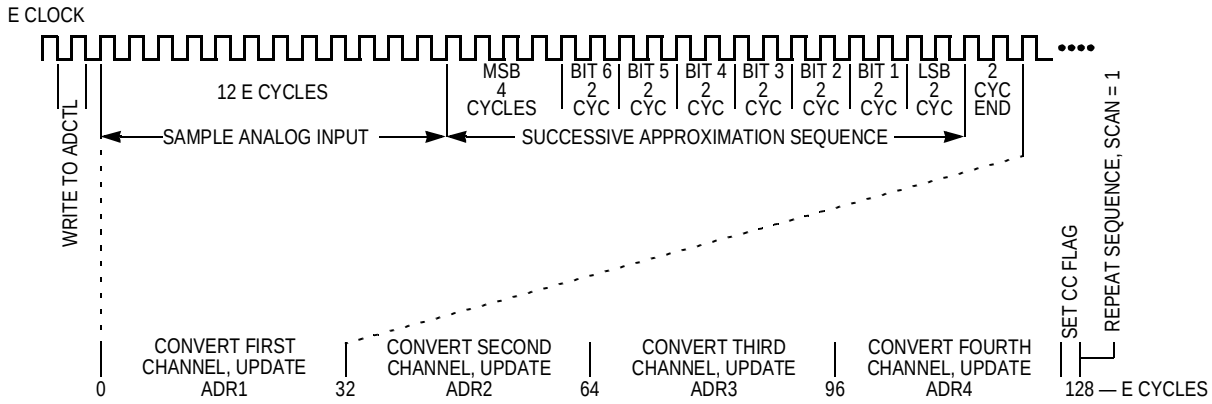


Figure 10-2. A/D Conversion Sequence

10.3.4 Digital Control

In addition to the conversion complete status flag, ADCTL bits select single or continuous conversions, whether conversions are performed on single or multiple channels, and the analog input(s) to be converted.

Single or continuous conversions are selected by the SCAN bit. Clearing the SCAN bit selects the single conversion option, in which results are written to each of the four result registers one time. The first result is stored in A/D result register 1 (ADR1), and the fourth result is stored in ADR4. All conversion activity is then halted until the ADCTL register is written again. In the continuous mode (SCAN =1), conversion activity does not stop. The fifth conversion is stored in register ADR1 (overwriting the first conversion result), the sixth conversion overwrites ADR2, and so on.

Section 11. Memory Expansion and Chip Selects

11.1 Contents

11.2 Introduction

This section provides descriptions of the expanded memory and the chip selects.

Address: $005A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	IOSA	IOSB	GP1SA	GP1SB	GP2SA	GP2SB	PCSA	PCSB
Reset:	0	0	0	0	0	0	0	0

Figure 11-14. Chip Select Clock Stretch Register (CSCSTR)

IOS[A:B] — CSIO Stretch Select Bits

GP1S[A:B] — CSGP1 Stretch Select Bits

GP2S[A:B] — CSGP2 Stretch Select Bits

PCS[A:B] — CSPROG Stretch Select Bits

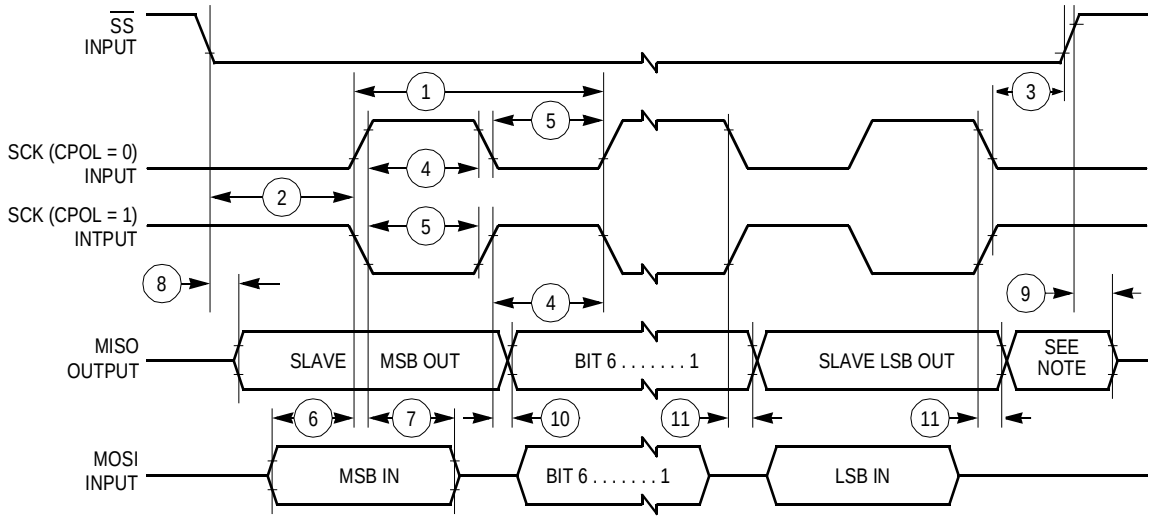
Each of these pairs of bits contain the binary number of cycles of clock stretch, as shown in **Table 11-9**.

Table 11-9. CSCSTR Bits Versus Clock Cycles

Bit [A:B]	Clock Stretch
0 0	None
0 1	1 cycle
1 0	2 cycles
1 1	3 cycles

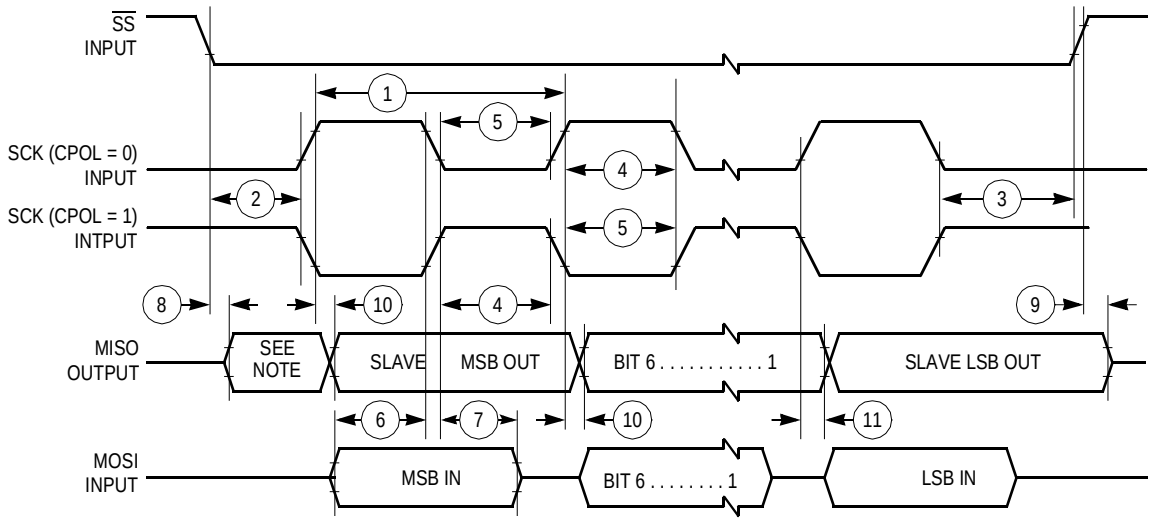
11.5 Memory Expansion Examples

The first example, shown in **Figure 11-15** contains a system with 64 Kbytes of external memory to be accessed through a single 8-Kbyte window. To access eight Kbytes, or 2^{13} address locations, the CPU will need 13 address lines, ADDR[12:0]. The number of memory banks needed is the total memory, 64 Kbytes divided by the window size, eight Kbytes. This yields eight memory banks, or 2^3. Thus, three expansion lines are required, so expansion address lines XA[15:13] replace CPU address lines ADDR[15:13]. **Figure 1-1** shows a memory map and schematic drawing of this system.



Note: Not defined, but normally MSB of character just received

a) SPI Slave Timing (CPHA = 0)



Note: Not defined, but normally LSB of character previously transmitted

b) SPI Slave Timing (CPHA = 1)

Figure 12-10. SPI Timing Diagram (Sheet 2 of 2)