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Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	3MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	62
Program Memory Size	24KB (24K x 8)
Program Memory Type	OTP
EEPROM Size	640 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.29x29.29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc711k4cfne3

MC68HC11K Family

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Section 1. General Description

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1.2 Introduction

The M68HC11K Family of high-performance microcontroller units (MCUs) offers a non-multiplexed expanded bus, high speed and low power consumption. The fully static design allows operation at frequencies from dc to 4 MHz.

This manual contains information concerning standard and custom-ROM (read-only memory) devices. Standard devices include those replacing the ROM with:

- Disabled ROM
- Disabled EEPROM (electrically erasable, programmable read-only memory)
- EPROM (erasable, programmable read-only memory)
- OTPROM (one-time progammable read-only memory)

Custom-ROM devices have a ROM array that is programmed at the factory to customer specifications.

NOTE: *Throughout this manual, the registers are discussed by function. In the event that not all bits in a register are referenced, the bits that are not discussed are shaded.*

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PORTA) See page 138.	Read: Write:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Reset:	Undefined after reset							
$0001	Port A Data Direction Register (DDRA) See page 138.	Read: Write:	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0
		Reset:	0	0	0	0	0	0	0	0
$0002	Port B Data Direction Register (DDRB) See page 139.	Read: Write:	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
		Reset:	0	0	0	0	0	0	0	0
$0003	Port F Data Direction Register (DDRF) See page 144.	Read: Write:	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0
		Reset:	0	0	0	0	0	0	0	0
$0004	Port B Data Register (PORTB) See page 139.	Read: Write:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
		Reset:	Undefined after reset							
$0005	Port F Data Register (PORTF) See page 144.	Read: Write:	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
		Reset:	Undefined after reset							
$0006	Port C Data Register (PORTC) See page 140.	Read: Write:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Reset:	Undefined after reset							
$0007	Port C Data Direction Register (DDRC) See page 141.	Read: Write:	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
		Reset:	0	0	0	0	0	0	0	0
$0008	Port D Data Register (PORTD) See page 142.	Read: Write:	0	0	PD5	PD4	PD3	PD2	PD1	PD0
		Reset:	0	0	U	U	U	U	U	U
$0009	Port D Data Direction Register (DDRD) See page 142.	Read: Write:	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Undefined

Figure 4-1. Register and Control Bit Assignments (Sheet 1 of 11)

4.6.2 ROM or EPROM

The presence and location of the 24-Kbyte (EP)ROM on the [7]11K4 is determined by two bits in the system configuration register (CONFIG). The CONFIG register is a special EEPROM register (see **Figure 4-6**).

(EP)ROM is present in the memory map when the ROMON bit is set and removed from the memory map when the bit is cleared. The default location of this memory is $A000–$FFFF, but it can be moved to $2000–$7FFF in expanded mode by clearing the ROMAD bit. Both bits are set out of reset in single-chip mode.

- On the [7]11KS2, (EP)ROM is 32 K, mapped to $8000–$FFFF by default, and moved to $0000–$7FFF by clearing the ROMAD bit.

In special test mode, the ROMON bit is forced to 0, removing (EP)ROM from the memory map.

4.6.3 EEPROM

The M68HC11K Family devices contain 640 bytes of EEPROM. It is initially located at $0D80 after reset if it is enabled by the EEON bit in the CONFIG register (see **Figure 4-6**). It can be relocated to any 4-K boundary ($xD80) by writing to the EEPROM mapping register (INIT2) (see **Figure 4-7**).

NOTE: *On the M68HC11K devices, the EEPROM can be mapped to where it will contain the vector space.*

Address: $0037

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EE3	EE2	EE1	EE0	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

Figure 4-7. EEPROM Mapping Register (INIT2)

NOTE: *INIT2 is writable once in normal modes and writable at any time in special modes.*

EE[3:0] — EEPROM Map Position Bits

These four bits determine the most-significant hexadecimal digit in the address range of the EEPROM, as shown in **Table 4-7**.

Table 4-7. EEPROM Map

EE[3:0]	Location
0000	$0D80–$0FFF
0001	$1D80–$1FFF
0010	$2D80–$2FFF
0011	$3D80–$3FFF
0100	$4D80–$4FFF
0101	$5D80–$5FFF
0110	$6D80–$6FFF
0111	$7D80–$7FFF
1000	$8D80–$8FFF
1001	$9D80–$9FFF
1010	$AD80–$AFFF
1011	$BD80–$BFFF
1100	$CD80–$CFFF
1101	$DD80–$DFFF
1110	$ED80–$EFFF
1111	$FD80–$FFFF

5.3.1 Power-On Reset (POR)

A positive transition on V_{DD} generates a POR, which is used only for power-up conditions. POR cannot be used to detect drops in power supply voltages. The CPU delays 4064 internal clock cycles after the oscillator becomes active to allow the clock generator to stabilize, then checks the $\overline{\text{RESET}}$ pin. If $\overline{\text{RESET}}$ is at logical 0, the CPU remains in the reset condition until the $\overline{\text{RESET}}$ pin goes to logical 1.

5.3.2 External Reset ($\overline{\text{RESET}}$)

The CPU distinguishes between internal and external reset conditions by sensing whether the reset pin rises to a logic 1 in less than two E-clock cycles after an internal device releases reset. When a reset condition is sensed, the $\overline{\text{RESET}}$ pin is driven low by an internal device for four E-clock cycles, then released. Two E-clock cycles later, it is sampled. If the pin is still held low, the CPU assumes that an external reset has occurred. If the pin is high, it indicates that the reset was initiated internally by either the COP system or the clock monitor.

NOTE: *It is not advisable to connect an external resistor capacitor (RC) power-up delay circuit to the reset pin of M68HC11 devices because the circuit charge time constant can cause the device to misinterpret the type of reset that occurred.*

5.3.3 Computer Operating Properly (COP) System

The MCU includes a COP system to help protect against software failures. When the COP is enabled, software periodically reinitializes a free-running watchdog timer before it times out and resets the system. Such a system reset indicates that a software error has occurred.

Table 5-5. Interrupt and Reset Vector Assignments

Vector Address	Interrupt Source	CC Register Mask	Local Mask
FFC0, C1 — FFD4, D5	Reserved	—	—
FFD6, D7	SCI serial system: • SCI transmit complete • SCI transmit data register empty • SCI idle line detect • SCI receiver overrun • SCI receive data register full	I bit	 TCIE TIE ILIE RIE RIE
FFD8, D9	SPI serial transfer complete	I bit	SPIE
FFDA, DB	Pulse accumulator input edge	I bit	PAII
FFDC, DD	Pulse accumulator overflow	I bit	PAOVI
FFDE, DF	Timer overflow	I bit	TOI
FFE0, E1	Timer input capture 4/output compare 5	I bit	I4/O5I
FFE2, E3	Timer output compare 4	I bit	OC4I
FFE4, E5	Timer output compare 3	I bit	OC3I
FFE6, E7	Timer output compare 2	I bit	OC2I
FFE8, E9	Timer output compare 1	I bit	OC1I
FFEA, EB	Timer input capture 3	I bit	IC3I
FFEC, ED	Timer input capture 2	I bit	IC2I
FFEE, EF	Timer input capture 1	I bit	IC1I
FFF0, F1	Real-time interrupt	I bit	RTII
FFF2, F3	$\overline{\text{IRQ}}$ (external pin)	I bit	None
FFF4, F5	$\overline{\text{XIRQ}}$ pin	X bit	None
FFF6, F7	Software interrupt	None	None
FFF8, F9	Illegal opcode trap	None	None
FFFA, FB	COP failure	None	NOCOP
FFFC, FD	Clock monitor fail	None	CME
FFFE, FF	RESET	None	None

6.9 Port G

The state of port G pin 7 (PG7) at reset is mode dependent. In single-chip or bootstrap modes, it is a high-impedance input; its data direction can be changed through DDRG. In expanded and special test modes, PG7 functions as the R/$\overline{W}$ line to control the direction of data flow between the MCU and external memory devices.

Port G pins (PG[6:0]) reset to high-impedance inputs in any mode. Data direction can be changed through DDRG. Port G bits [5:0] can serve as memory expansion address lines (see **11.3 Memory Expansion**) in expanded and special test modes. M68HC11KS devices do not contain these pins.

All eight port G pins have selectable internal pullup resistors (see **6.11 Internal Pullup Resistors**).

Address: $007E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PG7	PG6(1)	PG5(1)	PG4(1)	PG3(1)	PG2(1)	PG1(1)	PG0(1)
Reset:	0	0	0	0	0	0	0	0
Alternate Pin Function:	R/$\overline{W}$	—	XA18	XA17	XA16	XA15	XA14	XA13

1. Not available on KS devices

Figure 6-13. Port G Data Register (PORTG)

Address: $007F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDG7	DDG6(1)	DDG5(1)	DDG4(1)	DDG3(1)	DDG2(1)	DDG1(1)	DDG0(1)
Reset:	0	0	0	0	0	0	0	0

1. Not available on KS devices

Figure 6-14. Port G Data Direction Register (DDRG)

DDG[7:0] — Data Direction for Port G Bits
0 = Input
1 = Output

extra hardware. The SPI system can send data at up to one half of the E-clock rate when configured as master and the full E-clock rate when configured as a slave.

8.3 SPI Functional Description

The SPI is a 4-wire, full-duplex communication system. Characters are eight bits, transmitted most significant bit (MSB) first. One master device exchanges data with one or more slave devices. Each device selects its mode by writing either a 1 (master) or 0 (slave) to the MSTR bit in the serial peripheral control register (SPCR). As a master device transmits data to a slave device via the MOSI (master out slave in) line, the slave transmits data to the master via the MISO (master in slave out) line. The master produces a common synchronization clock signal and drives it on its SCK (serial clock) pin, which is configured as an output. The slave SCK pin is configured as an input to receive the clock. An external logic low signal is applied to the slave select pin ($\overline{SS}$) of each slave device for which a particular message is intended. Devices not selected ($\overline{SS}$ high) ignore the transmission.

Received characters are double-buffered. Serial input bits are fed into a shift register; when the last bit is received, the completed character is parallel-loaded to a read data buffer. This allows the next message to be received while the current message is being read. As long as the buffer is read before the next received character is ready to be transferred to the buffer, no overrun condition occurs.

Transmitted characters are not double-buffered, they are written directly to the output shift register. This means that new data for transmission cannot be written to the shift register until the previous transmission is complete. An attempt to write during data transmission will not go through; the transmission in progress will proceed undisturbed, and the MCU will set the write collision (WCOL) status bit in the serial peripheral status register (SPSR). After the last bit of a character is shifted out, the SPI transfer complete flag (SPIF) of the SPSR is set. This will also generate an interrupt if the SPIE (SPI interrupt enable) bit in the SPCR is set.

8.6.2 Serial Peripheral Status Register

Address: $0029

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	SPIF	WCOL	0	MODF	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 8-4. Serial Peripheral Status Register (SPSR)

SPIF — SPI Transfer Complete Flag

SPIF is set upon completion of data transfer between the processor and the external device. If SPIF goes high, and if SPIE is set, a serial peripheral interrupt is generated. To clear the SPIF bit, read the SPSR with SPIF set, then access the SPDR. Unless SPSR is read (with SPIF set) first, attempts to write SPDR are inhibited.

WCOL — Write Collision Bit

Clearing the WCOL bit is accomplished by reading the SPSR (with WCOL set) followed by an access of SPDR.

0 = No write collision
1 = Write collision

MODF — Mode Fault Bit

To clear the MODF bit, read the SPSR (with MODF set), then write to the SPCR.

0 = No mode fault
1 = Mode fault

Section 9. Timing System

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9.3 Timer Structure

As Figure 9-1 shows, the primary system clocks, including the E clock and the internal PH2 bus clock, are derived from the oscillator output divided by four.

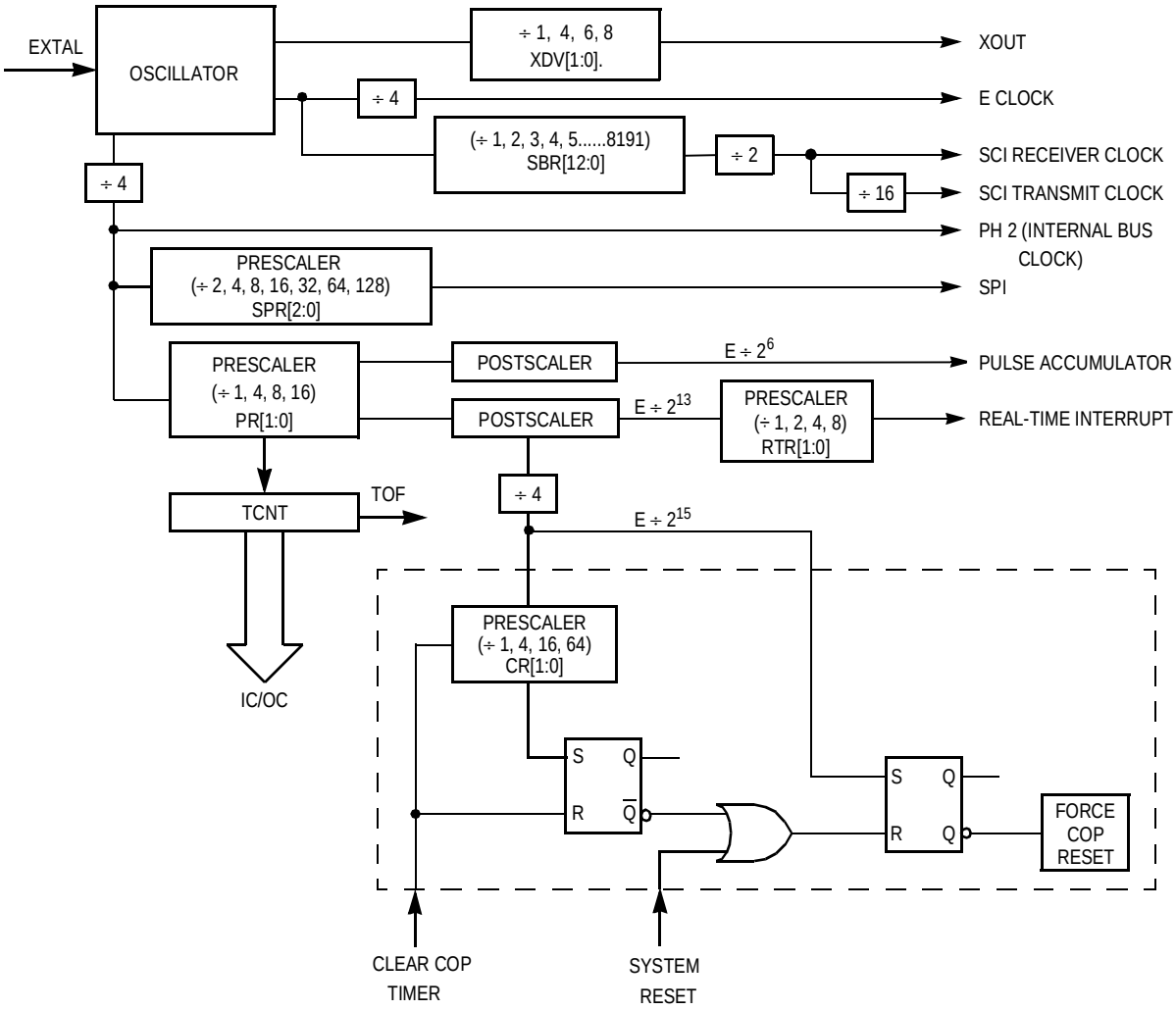


Figure 9-1. Timer Clock Divider Chains

9.7.4 Timer Interrupt Mask 2 Register

Address: $0024

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
Reset:	0	0	0	0	0	0	0	0

Figure 9-25. Timer Interrupt Mask 2 (TMSK2)

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2.

PAOVF — Pulse Accumulator Overflow Flag

The PAOVF status bit is set each time the pulse accumulator count rolls over from $FF to $00.

PAOVI — Interrupt Enable Bit

If PAOVI is set, an interrupt request is also generated. If PAOVI is cleared, pulse accumulator overflow interrupts are inhibited, and PAOVF must be polled by user software to determine when an overflow has occurred. In either case, software must clear PAOVF by writing a 1 to bit 5 in the TFLG2 register.

PAIF — Pulse Accumulator Input Edge Flag

The PAIF status bit is automatically set each time a selected edge is detected at the PA7 pin.

PAII — Interrupt Enable Bit

If PAII is set, an interrupt request is also generated. If PAII is cleared, pulse accumulator input interrupts are inhibited, and PAIF must be polled by user software to determine when an input edge has been detected. In either case, software must clear PAIF by writing a 1 to bit 5 in the TFLG2 register.

9.9.2.4 Pulse-Width Modulation Timer Enable Register

Address: $0063

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TPWSL	DISCP	0	0	PWEN4	PWEN3	PWEN2	PWEN1
Reset:	0	0	0	0	0	0	0	0

Figure 9-34. Pulse-Width Modulation Timer Enable Register (PWEN)

TPWSL — PWM Scaled Clock Test Bit — factory use only; only accessible in special test mode

0 = Normal operation

1 = Clock S is output to PWSCAL register (test only)

DISCP — Disable Compare Scaled E-Clock Bit — factory use only; only accessible in special test mode

0 = Normal operation

1 = Match of period does not reset associated count register (test only)

PWEN[4:1] — Pulse-Width Enable for Channels [4:1] Bits

0 = Channel disabled

1 = Channel enabled at port H bits [3:0]

register is set after the fourth conversion in a sequence to signal the availability of data in the result registers.The result registers are written during a portion of the system clock cycle when reads do not occur, so there is no conflict. A conversion sequence can repeat continuously or stop after one iteration. **Figure 10-2** shows the timing of a typical sequence. In this example, synchronization is referenced to the system E clock.

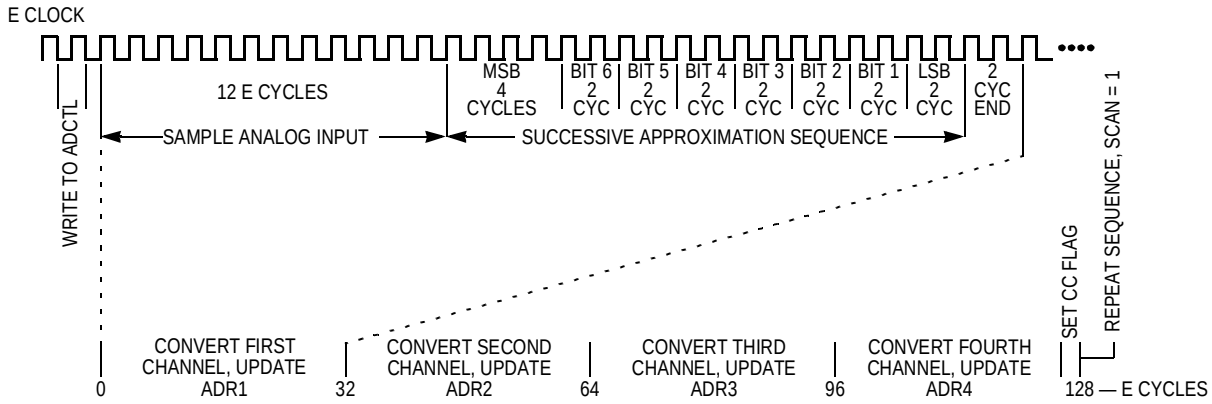


Figure 10-2. A/D Conversion Sequence

10.3.4 Digital Control

In addition to the conversion complete status flag, ADCTL bits select single or continuous conversions, whether conversions are performed on single or multiple channels, and the analog input(s) to be converted.

Single or continuous conversions are selected by the SCAN bit. Clearing the SCAN bit selects the single conversion option, in which results are written to each of the four result registers one time. The first result is stored in A/D result register 1 (ADR1), and the fourth result is stored in ADR4. All conversion activity is then halted until the ADCTL register is written again. In the continuous mode (SCAN =1), conversion activity does not stop. The fifth conversion is stored in register ADR1 (overwriting the first conversion result), the sixth conversion overwrites ADR2, and so on.

10.4 A/D Control/Status Registers

The registers involved in A/D operation include OPTION, ADCTL, and the four result registers ADR[1:4].

NOTE: *Throughout this manual, the registers are discussed by function. In the event that not all bits in a register are referenced, the bits that are not discussed are shaded.*

10.4.1 System Configuration Options Register

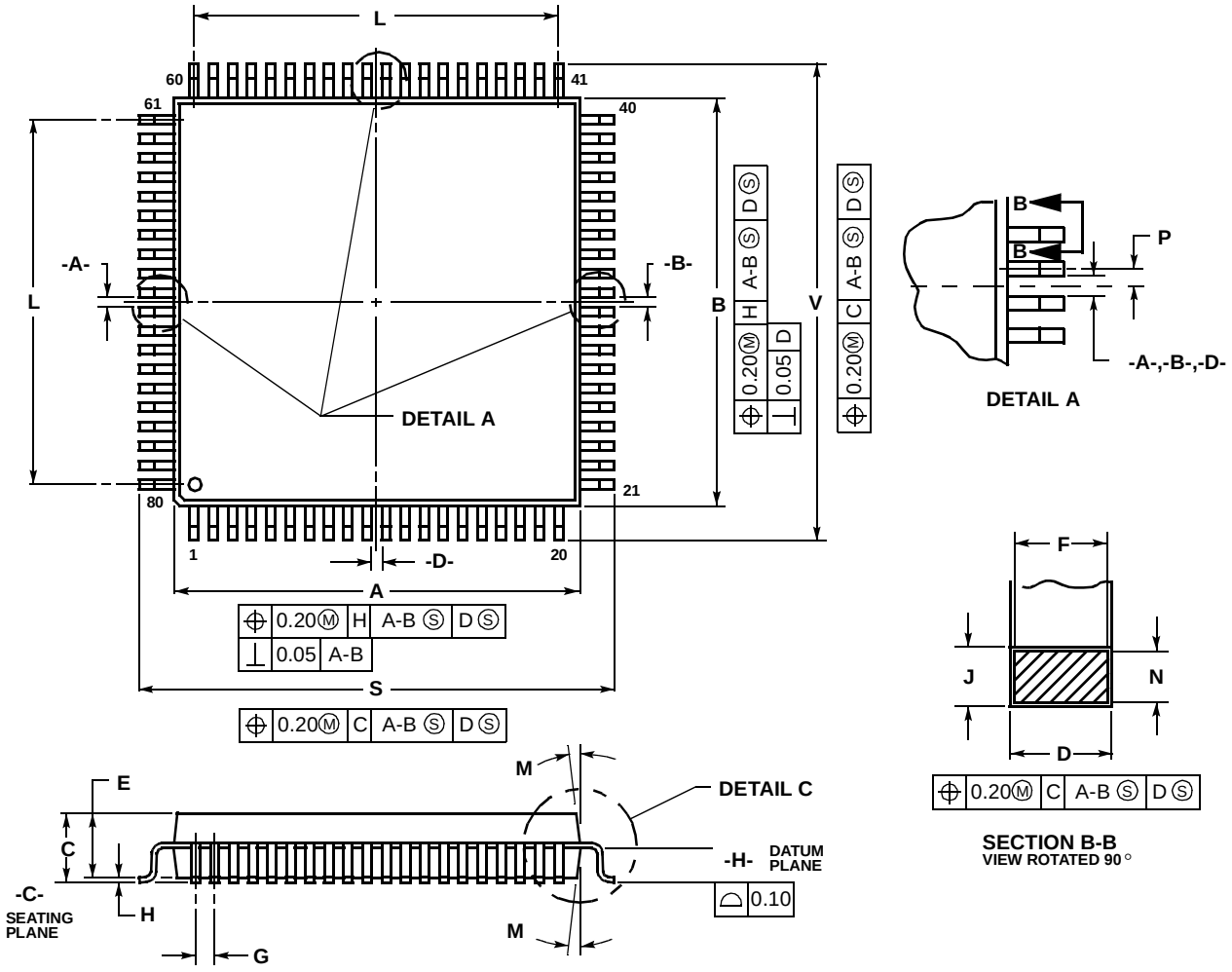
Bit 7 in the system configuration options register (OPTION), ADPU, enables the A/D converter system. Setting ADPU applies power to the A/D circuitry, including the charge pump that drives the analog switches. Clearing ADPU removes power from the A/D system.

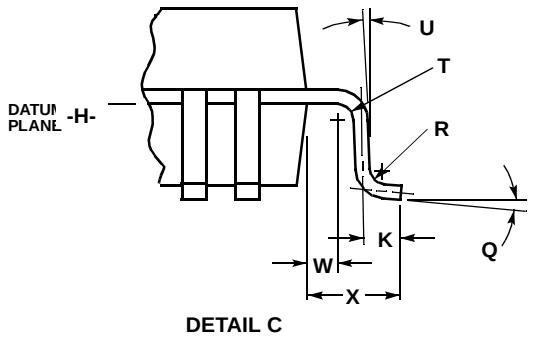
The gates of analog switches in the multiplexer are driven by a charge pump that develops between seven and eight volts. The high gate voltage assures low source-to-drain impedance for the analog signals. Both the charge pump and the comparator circuits require up to 100 µs to stabilize after setting the ADPU bit.

The CSEL bit (bit 6) determines whether the A/D converter uses the system E clock or an internal RC oscillator for synchronization. It is cleared out of reset, selecting the E clock. This is the preferred setting at normal operating frequencies because all switching and comparator operations are synchronized to the main MCU clocks. This allows the comparator output to be sampled at relatively quiet portions of the MCU clock cycles.

When the E clock frequency is less than 750 kHz, charge leakage in the capacitor array can cause errors. In this case, set the CSEL bit to select the internal oscillator, which usually runs at about 2 MHz. The additional error introduced by the asynchronous oscillator is about ± 1/2 LSB (least significant bit), which is usually less than that incurred by a slow clock.

13.5 80-Pin Quad Flat Pack (Case 841B)





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS	
DIM	MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5°	10°
N	0.13	0.17
P	0.325 BSC	
Q	0°	7°
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0°	---
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	