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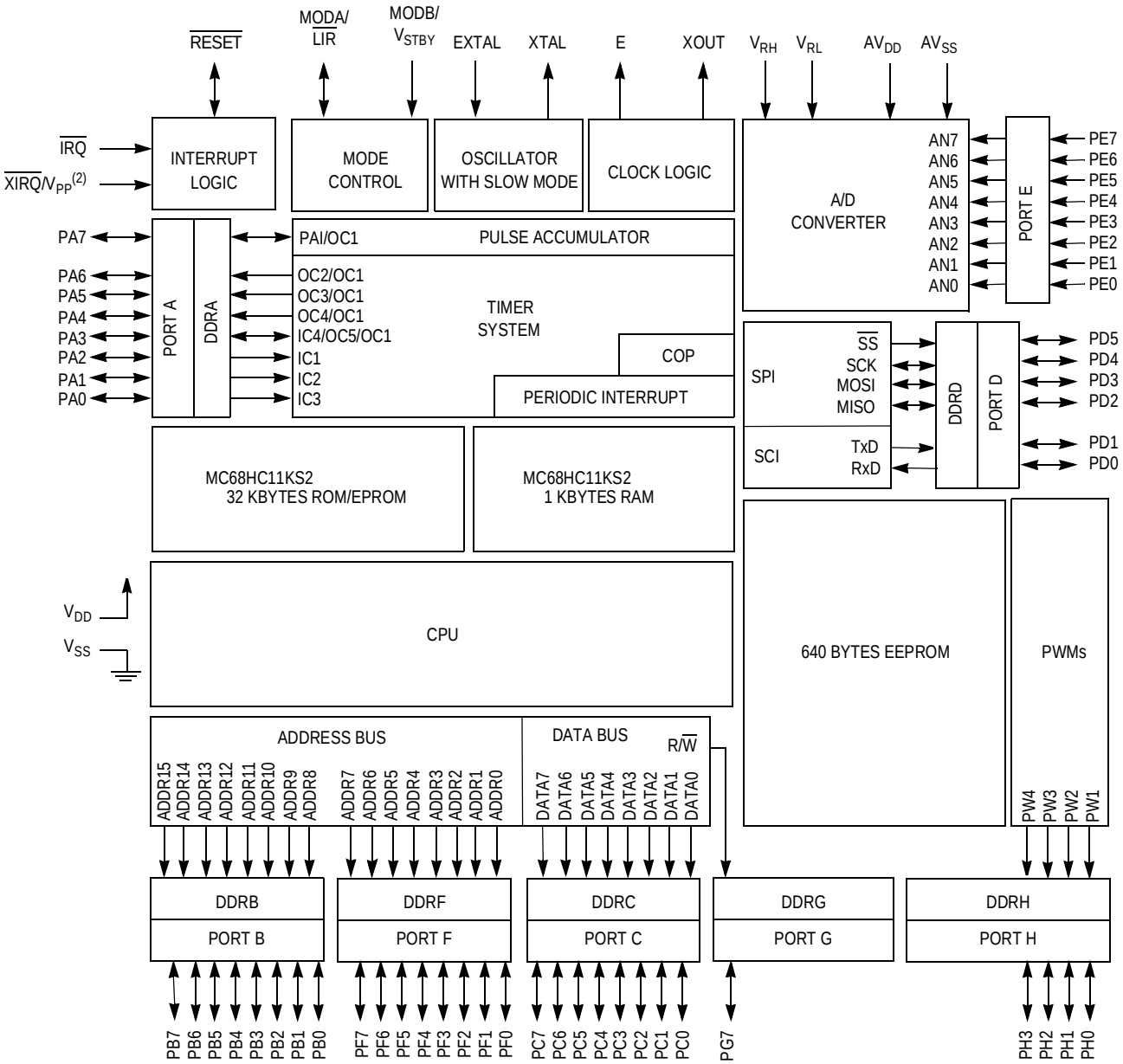
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	4MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	62
Program Memory Size	24KB (24K x 8)
Program Memory Type	OTP
EEPROM Size	640 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc711k4cfue4



Notes:
1. The configuration shown in this diagram is the MC68HC11KS2.
2. V_{PP} applies only to EPROM devices.

Figure 1-2. M68HC11KS Family Block Diagram

required for wire-OR configuration. Software can change the triggering to edge sensitive.

$\overline{\text{XIRQ}}$ interrupts can be non-maskable after reset initialization. Out of reset, the X bit in the CCR is set, masking $\overline{\text{XIRQ}}$ interrupts. Once software clears the X bit, it cannot be reset, and the $\overline{\text{XIRQ}}$ interrupts become non-maskable. The $\overline{\text{XIRQ}}$ input is level sensitive only. $\overline{\text{XIRQ}}$ is often used as a power-loss detect interrupt.

Whenever $\overline{\text{IRQ}}$ or $\overline{\text{XIRQ}}$ is used with multiple interrupt sources, each source must drive the interrupt input with an open-drain type of driver to avoid contention between outputs. There should be a single pullup resistor near the MCU interrupt pin (typically 4.7 kΩ). There must also be an interlock mechanism at each interrupt source which holds the interrupt line low until the MCU recognizes and acknowledges the interrupt request. If any interrupt sources are still pending after the MCU services a request, the interrupt line will remain low, interrupting the MCU again as soon as the I bit in the MCU is cleared (normally upon return from an interrupt). Interrupt mechanisms are explained further in **Section 5. Resets and Interrupts**.

On EPROM devices, the $\overline{\text{XIRQ}}$ pin also functions as the high-voltage supply, V_{PP}, during EPROM or OTPROM programming.

CAUTION: *Ensure that the voltage level at this pin is equal to V_{DD} during normal operation to avoid programming accidents.*

2.9 Mode Selection, Instruction Cycle Reference, and Standby Power (MODA/$\overline{\text{LIR}}$ and MODB/V_{STBY})

During reset, MODA and MODB select one of four operating modes:

1. Single-chip
2. Expanded
3. Bootstrap
4. Special test

For full descriptions of these modes, refer to **4.5 Operating Modes**.

3.3.5 Program Counter (PC)

The 16-bit program counter contains the address of the next instruction to be executed. Its initial value after reset is fetched from one of six possible vectors, depending on operating mode and the cause of reset, as described in **5.3 Sources of Resets**.

3.3.6 Condition Code Register (CCR)

This 8-bit register contains:

- Five condition code indicators (C, V, Z, N, and H)
- Two interrupt masking bits (IRQ and XIRQ)
- A stop disable bit (S)

Most instructions update condition codes automatically, as described in the following paragraphs. Certain instructions, such as pushes, pulls, add B to X (ABX), add B to Y (ABY), and transfer/exchange instructions do not affect the condition codes. **Table 3-1** shows which condition codes are affected by each instruction.

3.3.6.1 Carry/Borrow (C)

The C bit is set if the CPU performs a carry or borrow during an arithmetic operation. This bit also acts as an error flag for multiply and divide operations. Shift and rotate instructions operate with and through the carry bit to facilitate multiple-word shift operations.

3.3.6.2 Overflow (V)

The overflow bit is set if an operation results in a two’s complement overflow of the 8-bit signed range –128 to +127. Otherwise, the V bit is cleared.

3.3.6.3 Zero (Z)

The Z bit is set if the result of an arithmetic, logic, or data manipulation operation is 0. Otherwise, the Z bit is cleared. Compare instructions do

Address: $003F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ROMAD	1	CLKX	PAREN	NOSEC	NOCOP	ROMON	EEON
Reset:	—	1	—	—	—	—	—	—

Figure 4-6. System Configuration Register (CONFIG)

NOTE: *CONFIG is writable once in normal modes and writable at any time in special modes.*

ROMAD — ROM Address Mapping Control Bit

Set out of reset in single-chip mode

0 = (EP)ROM set at $2000–$7FFF;
$0000–$7FFF in [7]11KS2;
$0000–$BFFF in [7]11KS8
(expanded mode only)

1 = (EP)ROM set at $A000–$FFFF;
$8000–$FFFF in [7]11KS2;
$4000–$FFFF in [7]11KS8

ROMON — ROM/PROM Enable Bit

Set by reset in single-chip mode; cleared by reset in special test mode

0 = (EP)ROM removed from the memory map
1 = (EP)ROM present in the memory map

EEON — EEPROM Enable Bit

0 = 640-byte EEPROM disabled
1 = 640-byte EEPROM enabled

Address: $003F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ROMAD	1	CLKX	PAREN	NOSEC	NOCOP	ROMON	EEON
Reset:	—	1	—	—	1	—	—	—

Figure 4-13. System Configuration Register (CONFIG)

NOTE: *CONFIG is writable once in normal modes and writable at any time in special modes.*

NOSEC — RAM and EPROM Security Disabled Bit
0 = Enable security
1 = Disable security

M68HC11K Family devices are normally manufactured with NOSEC set and the security option unavailable. However, on special request, a mask option is selected during fabrication that enables the security mode. The secure mode can be invoked on these parts by clearing NOSEC. Contact a Motorola representative for information on the availability of this feature.

The bootstrap program performs this sequence when the security feature is present, enabled, and bootstrap mode is selected:

1. Output $FF, all 1s, on the SCI.
2. Clear the BPROT register by turning block protect off.
3. If the EEPROM is enabled, erase the EEPROM.
4. Verify that the EEPROM is erased. If EEPROM is not erased, begin sequence again.
5. Write $FF, all 1s, to the entire block of RAM.
6. Erase the CONFIG register.

If all of the operations are successful, the bootload process continues as if the device was never secured.

Table 5-5. Interrupt and Reset Vector Assignments

Vector Address	Interrupt Source	CC Register Mask	Local Mask
FFC0, C1 — FFD4, D5	Reserved	—	—
FFD6, D7	SCI serial system: • SCI transmit complete • SCI transmit data register empty • SCI idle line detect • SCI receiver overrun • SCI receive data register full	I bit	 TCIE TIE ILIE RIE RIE
FFD8, D9	SPI serial transfer complete	I bit	SPIE
FFDA, DB	Pulse accumulator input edge	I bit	PAII
FFDC, DD	Pulse accumulator overflow	I bit	PAOVI
FFDE, DF	Timer overflow	I bit	TOI
FFE0, E1	Timer input capture 4/output compare 5	I bit	I4/O5I
FFE2, E3	Timer output compare 4	I bit	OC4I
FFE4, E5	Timer output compare 3	I bit	OC3I
FFE6, E7	Timer output compare 2	I bit	OC2I
FFE8, E9	Timer output compare 1	I bit	OC1I
FFEA, EB	Timer input capture 3	I bit	IC3I
FFEC, ED	Timer input capture 2	I bit	IC2I
FFEE, EF	Timer input capture 1	I bit	IC1I
FFF0, F1	Real-time interrupt	I bit	RTII
FFF2, F3	$\overline{\text{IRQ}}$ (external pin)	I bit	None
FFF4, F5	$\overline{\text{XIRQ}}$ pin	X bit	None
FFF6, F7	Software interrupt	None	None
FFF8, F9	Illegal opcode trap	None	None
FFFA, FB	COP failure	None	NOCOP
FFFC, FD	Clock monitor fail	None	CME
FFFE, FF	RESET	None	None

5.5.1 Non-Maskable Interrupts

Non-maskable interrupts can interrupt CPU operations at any time. The most common use for such an interrupt is for serious system problems, such as program runaway or power failure. The three sources of non-maskable interrupt are:

- $\overline{\text{XIRQ}}$ pin
- Illegal opcode trap
- Software interrupt instruction (SWI)

5.5.1.1 Non-Maskable Interrupt Request ($\overline{XIRQ}$)

The $\overline{\text{XIRQ}}$ input is an updated version of the non-maskable $\overline{\text{NMI}}$ input of earlier MCUs. Upon reset, both the X bit and I bit of the CCR are set to inhibit all maskable interrupts and $\overline{\text{XIRQ}}$. After minimum system initialization, software can clear the X bit by a transfer from accumulator A to condition code register (TAP) instruction, enabling $\overline{\text{XIRQ}}$ interrupts. Thereafter, software cannot set the X bit and the $\overline{\text{XIRQ}}$ interrupt becomes non-maskable.

I bit-related interrupts do not affect the X bit, which has a higher priority than they do in the interrupt priority logic. When an I bit-related interrupt occurs, the CPU sets the I bit after stacking the CCR byte, but the X bit remains unaffected. When an X bit-related interrupt occurs, the CPU sets both the X and I bits after stacking the CCR. The RTI instruction restores the X and I bits to their pre-interrupt request state when it pulls the CCR from the stack.

5.5.1.2 Illegal Opcode Trap

The MCU includes an illegal opcode detection circuit to avoid attempting to process undefined opcodes or opcode sequences. This mechanism works for all unimplemented opcodes on all four opcode map pages. When the circuit detects an illegal opcode, it generates an interrupt. The CPU responds by pushing the current value of the program counter, which is actually the address of the first byte of the illegal opcode, on the stack. The illegal opcode service routine can use this stacked address as a pointer to the illegal opcode to correct it. To avoid repeated

6.7 Port E

Port E, PE[7:0], is the only port that functions as input only, and its pins are configured as high-impedance inputs out of reset. It also serves as the analog input for the analog-to-digital converter when this function is enabled by software (see **Section 10. Analog-to-Digital (A/D) Converter**).

NOTE: *PORT E should not be read during the sample portion of an A/D conversion.*

Address: $000A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	PE7	PE6	PE5	PE4	PE3	PE2	PD1	PD0
Reset:	Undefined after reset							
Alternate Pin Function:	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

Figure 6-10. Port E Data Register (PORTE)

- The overrun error (OR) flag is set instead of the RDRF bit when the next byte is ready to be transferred from the receive shift register to the RDR and the RDR is already full. The data in the shift register is lost and the data that was already in RDR is not disturbed.
- The noise flag (NF) is set if there is noise on any of the received bits, including the start and stop bits. The data recovery circuit takes three samples of each bit and indicates noise if any set of three samples is not unanimous. NF is not set until the entire character is received and transferred to the RDR, when RDRF is set.
- The framing error (FE) flag is set when no stop bit is detected in the received data character. FE is set at the same time as RDRF. If the byte received causes both framing and overrun errors, the processor only recognizes the overrun error. The framing error flag inhibits further data transfer into the RDR until the flag is cleared.
- The parity error (PE) flag indicates that the parity bit of a received character does not match the parity calculated by hardware.
- The receiver active flag (RAF) is a read-only bit that is set during data reception and cleared when the line goes idle. This is the only flag cleared by hardware.

Figure 7-3 is a block diagram of the SCI receiver.

7.6 Wakeup Feature

The wakeup feature reduces SCI service overhead in multiple receiver systems. If a system generates address information at the beginning of every message, each receiver can determine whether or not it is the intended recipient of a message by evaluating the first character(s) through software.

If the message is intended for a different receiver, the SCI can be placed in a sleep mode so that the rest of the message will not generate requests for service. It does this by setting the RWU (receiver wakeup) bit in SCI control register 2 (SCCR2), which inhibits all receiver-related status flags (RDRF, IDLE, OR, NF, FE, PF, and RAF). A new message clears the receiver's RWU bit, enabling it to evaluate the new address information. Although RWU can be cleared by a software write to SCCR2, this is rarely done because hardware clears RWU automatically.

Two methods of wakeup are available:

- Idle line wakeup — A sleeping receiver wakes up as soon as the RxD line becomes idle (for example, in a logic 1 state for at least one frame time). A system using this type of wakeup must provide at least one character time of idle between messages to wake up sleeping receivers and must not allow any idle time between characters within a message.
- Address mark wakeup — Uses the most significant bit (MSB) to distinguish address characters (MSB = 1) from data characters (MSB = 0). A sleeping receiver wakes up whenever it receives an address character. Unlike the idle line method, address mark wakeup allows idle periods within messages and does not require idle time between messages. However, message processing is less efficient because the start bit of each character must be evaluated.

7.9.2 Serial Communications Control Register 1

Address $0072

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	LOOPS	WOMS	0	M	WAKE	ILT	PE	PT
Reset:	U	U	0	0	0	0	0	0

U = Undefined

Figure 7-7. SCI Control Register 1 (SCCR1)

LOOPS — SCI Loop Mode Enable Bit

Both the transmitter and receiver must be enabled to use the loop mode. When the loop mode is enabled, the TxD pin is driven high (idle line state) if the transmitter is enabled.

0 = SCI transmit and receive operate normally.
1 = SCI transmit and receive are disconnected from TxD and RxD pins, and transmitter output is fed back into the receiver input.

WOMS — Wired-OR Mode for SCI Pins PD[1:0] Bits

See also **8.6.1 Serial Peripheral Control Register** for a description of the DWOM (port D wired-OR mode) bit in the serial peripheral control register (SPCR).

0 = TxD and RxD operate normally.
1 = TxD and RxD are open drains if operating as outputs.

M — Mode (SCI Word Size) Bit

0 = Start bit, 8 data bits, 1 stop bit
1 = Start bit, 9 data bits, 1 stop bit

WAKE — Wakeup Mode Bit

0 = Wake up by idle line recognition
1 = Wake up by address mark (most significant data bit set)

ILT — Idle Line Type Bit

0 = Short (SCI counts consecutive 1s after start bit.)
1 = Long (SCI counts one only after stop bit.)

8.4 SPI Signal Descriptions

The four basic SPI signals (MISO, MOSI, SCK, and $\overline{SS}$) are discussed for both the master and slave modes in the following paragraphs.

Every SPI output line must have its corresponding port D data direction register (DDRD) bit set. If this bit is clear, the line is disconnected from the SPI logic and becomes a general-purpose input line. SPI input lines are not affected by the data direction register.

8.4.1 Master In Slave Out (MISO)

The MISO is one of two unidirectional serial data lines in the SPI. It functions as an input in a master device and as an output in a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave is not selected.

8.4.2 Master Out Slave In (MOSI)

This unidirectional serial data line is an output in a master device and an input in a slave device.

8.4.3 Serial Clock (SCK)

The serial clock (SCK) synchronizes data movement both in and out of all devices. Master and slave devices exchange a byte of information simultaneously during a sequence of eight clock cycles. SCK is generated by the master device so its SCK pin functions as an output. Slave devices receive this signal through their SCK pins, which are configured as inputs.

The SPI clock rate select bits in the master device determine the SCK clock rate. These bits are SPR[1:0] in the serial peripheral control register (SPCR) and SPR2 in the system configuration options 2 register (OPT2). These bits have no effect in a slave device.

CPOL — Clock Polarity Bit

When the clock polarity bit is cleared and data is not being transferred, the SCK pin of the master device has a steady state low value. When CPOL is set, SCK idles high.

CPHA — Clock Phase Bit

The clock phase bit, in conjunction with the CPOL bit, controls the clock-data relationship between master and slave. The CPHA bit selects one of two different clocking protocols.

SPR[1:0] — SPI Clock Rate Select Bits

On a master device, these two bits in conjunction with SPR2 in the OPT2 register select the baud rate to be used as SCK. See **Table 8-1**. These bits have no effect in slave mode.

Table 8-1. SPI+ Baud Rates

EXTAL Frequencies						
EXTAL Freq.	**8.0 MHz**	**12.0 MHz**	**16.0 MHz**	**20.0 MHz**	**24.0 MHz**	**Other EXTAL**
E Clock Freq.	**2.0 MHz**	**3.0 MHz**	**4.0 MHz**	**5.0 MHz**	**6.0 MHz**	**EXTAL ÷ 4**
Control Bits SPR[2:0]	**SPI Baud Rate**					**E Clock Divide by**
0 0 0	1.0 MHz	1.5 MHz	2.0 MHz	2.5 MHz	3.0 MHz	2
0 0 1	500 kHz	750 kHz	1.0 MHz	1.3 kHz	1.5 MHz	4
0 1 0	125 kHz	187.5 kHz	250 kHz	312.5 kHz	375.0 kHz	16
0 1 1	62.5 kHz	93.8 kHz	125 kHz	156.3 kHz	187.5 kHz	32
1 0 0	250 kHz	375 kHz	500 kHz	625 kHz	750.0 kHz	8
1 0 1	125 kHz	187.5 kHz	250 kHz	312.5 kHz	375.0 kHz	16
1 1 0	31.3 kHz	46.9 kHz	62.5 kHz	78.1 kHz	93.8 kHz	64
1 1 1	15.6 kHz	23.4 kHz	31.3 kHz	39.1 kHz	46.9 kHz	128

8.6.2 Serial Peripheral Status Register

Address: $0029

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	SPIF	WCOL	0	MODF	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 8-4. Serial Peripheral Status Register (SPSR)

SPIF — SPI Transfer Complete Flag

SPIF is set upon completion of data transfer between the processor and the external device. If SPIF goes high, and if SPIE is set, a serial peripheral interrupt is generated. To clear the SPIF bit, read the SPSR with SPIF set, then access the SPDR. Unless SPSR is read (with SPIF set) first, attempts to write SPDR are inhibited.

WCOL — Write Collision Bit

Clearing the WCOL bit is accomplished by reading the SPSR (with WCOL set) followed by an access of SPDR.

0 = No write collision
1 = Write collision

MODF — Mode Fault Bit

To clear the MODF bit, read the SPSR (with MODF set), then write to the SPCR.

0 = No mode fault
1 = Mode fault

9.4.5 Pulse Accumulator Control Register

Address: $0026

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	PAEN	PAMOD	PEDGE	0	I4/O5	RTR1	RTR0
Reset:	0	0	0	0	0	0	0	0

Figure 9-7. Pulse Accumulator Control Register (PACTL)

I4/O5 — Input Capture 4/Output Compare 5 Bit
0 = Configure PA3 as OC5
1 = Configure PA3 as IC4

To configure PA3 as input compare 4, clear DDA3 and set I4/05. To configure PA3 as output compare 5, set DDA3 and clear I4/05. If the DDA3 bit is set (configuring PA3 as an output) and IC4 is enabled, writing a one to TI4/O5 causes an input capture. Writing to TI4/O5 has no effect when DDA3 is cleared and/or OC5 is enabled.

9.5 Input Capture (IC)

The input capture function records the time an external event occurs by latching the value of the free-running counter into one of the timer input capture (TIC) registers when a selected edge is detected at its associated timer input pin. Software can store latched values and use them to compute the period and duration of events. For example, by storing the times of successive edges of an incoming signal, software can determine the period and pulse width of a signal. To measure the period, two successive edges of the same polarity are captured. To measure pulse width, two alternate polarity edges are captured.

Capture requests are latched on the opposite half cycle of PH2 from when the timer counter is being incremented. This synchronization process introduces a delay between edge occurrence and counter value detection. Because these delays offset each other when the time between two edges is measured, they can be ignored. There is a similar delay for output compare between the actual compare point and when the output pin changes state.

	Bit 7	6	5	4	3	2	1	Bit 0
Address:	$001A— TOC3 (High)							
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1
Address:	$001B — TOC3 (Low)							
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1
Address:	$001C— TOC4 (High)							
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1
Address:	$001D — TOC4 (Low)							
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1

Figure 9-13. Timer Output Compare Registers (TOC1–TOC4) (Continued)

All output compare registers are 16-bit read-write. Any of these registers can be used as a storage location if it is not used for output compare or input capture.

12.7 Power Dissipation Characteristics

Characteristic	Symbol	2 MHz	3 MHz	4 MHz	Unit
Maximum total supply current(1) **RUN:** Single-chip mode Expanded mode Slow mode	I_{DD}	 27 35 6.5	 33 42 7.0	 40 50 7.5	mA
WAIT: (All peripheral functions shut down) Single-chip mode Expanded mode Slow mode	WI_{DD}	 10 12 3.5	 15 17 4.5	 20 22 5.5	mA
STOP: (No clocks) Single-chip mode	SI_{DD}	 50	 50	 50	µA
Maximum power dissipation Single-chip mode Expanded mode	P_D	 149 193	 149 193	 220 275	mW

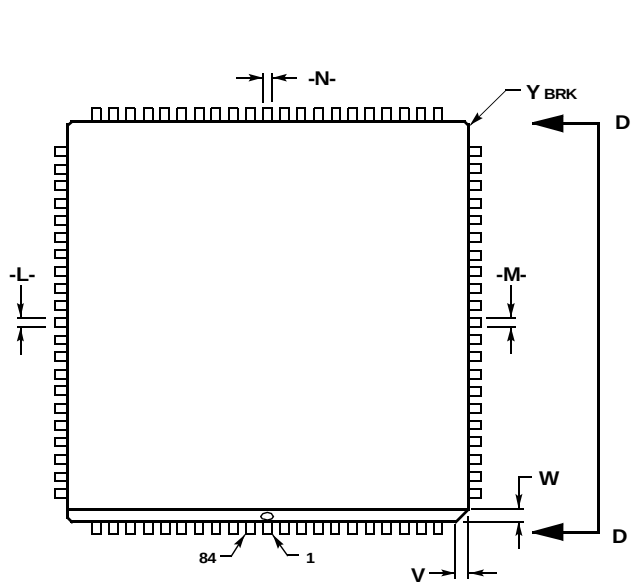
1. EXTAL is driven with a square wave; t_{cyc} = 500 ns for 2 MHz rating; t_{cyc} = 250 ns for 4 MHz rating; $V_{IL} \le 0.2$ V; $V_{IH} \ge V_{DD} - 0.2$ V; no dc loads

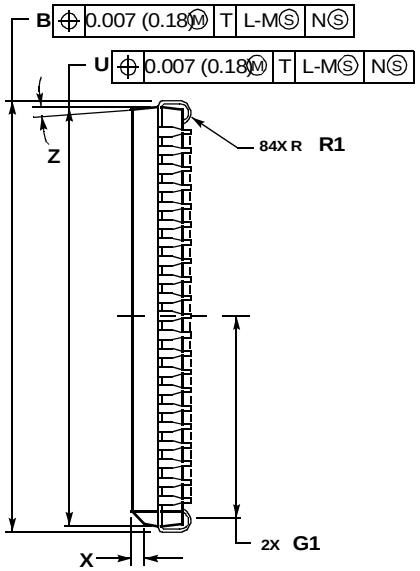
12.11 Expansion Bus Timing

Num	Characteristic[1]	Symbol	2.0 MHz		3.0 MHz		4.0 MHz		Unit
			Min	Max	Min	Max	Min	Max	
	Frequency of operation (E clock)[2]	f_o	dc	2.0	dc	3.0	dc	4.0	MHz
1	Cycle time, $t_{cyc} = 1/f_o$	t_{cyc}	500	—	333	—	250	—	ns
2	Pulse width, E low, $PW_{EL} = 1/2\ t_{cyc} - 20$ ns	PW_{EL}	230	—	147	—	105	—	ns
3	Pulse width, E high[3] $PW_{EH} = 1/2\ t_{cyc} - 25$ ns	PW_{EH}	225	—	142	—	100	—	ns
4A 4B	E clock Rise time Fall time	 t_r t_f	 — —	 20 20	 — —	 20 18	 — —	 20 15	ns
9	Address hold time, $t_{AH} = 1/8\ t_{cyc} - 10$ ns	t_{AH}	53	—	32	—	21	—	ns
11	Address delay time, $t_{AD} = 1/8\ t_{cyc} + 40$ ns	t_{AD}	—	103	—	82	—	71	ns
12	Address valid time to E rise $t_{AV} = PW_{EL} - t_{AD}$	t_{AV}	128	—	65	—	34	—	ns
17	Read data setup time	t_{DSR}	30	—	30	—	20	—	ns
18	Read data hold time	t_{DHR}	0	—	0	—	0	—	ns
19	Write data delay time	t_{DDW}	—	40	—	40	—	40	ns
21	Write data hold time, $t_{DHW} = 1/8\ t_{cyc}$	t_{DHW}	63	—	42	—	31	—	ns
29	MPU address access time[3] $t_{ACCA} = t_{cyc} - t_f - t_{DSR} - t_{AD}$	t_{ACCA}	348	—	203	—	144	—	ns
39	Write data setup time[3] $t_{DSW} = PW_{EH} - t_{DDW}$	t_{DSW}	185	—	102	—	60	—	ns
50	E valid chip-select delay time	t_{ECSD}	—	40	—	40	—	40	ns
51	E valid chip-select access time[3] $t_{ECSA} = PW_{EH} - t_{ECSD} - t_{DSR}$	t_{ECSA}	155	—	72	—	40	—	ns
52	Chip select hold time	t_{CH}	0	20	0	20	0	20	ns
54	Address valid chip-select delay time $t_{ACSD} = 1/4\ t_{cyc} + 40$ ns	t_{ACSD}	—	165	—	123	—	103	ns
55	Address valid chip-select access time $t_{ACSA} = t_{cyc} - t_f - t_{DSR} - t_{ACSD}$[3]	t_{ACSA}	285	—	162	—	113	—	ns
56	Address valid to chip-select time	t_{AVCS}	10	—	10	—	10	—	ns
57	Address valid to data three-state time	t_{AVDZ}	—	10	—	10	—	10	ns

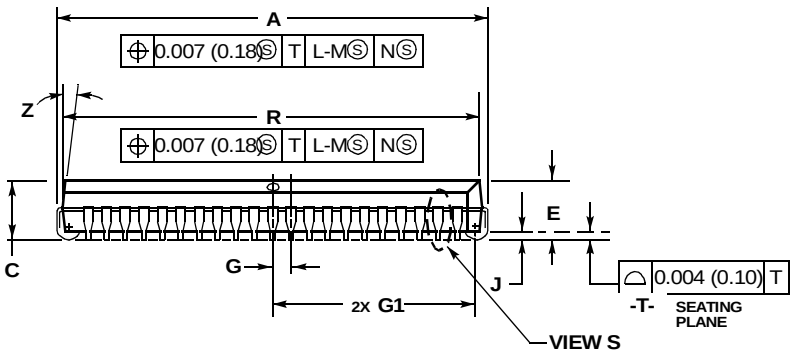
1. $V_{DD} = 5.0 \pm 10\%$, $V_{SS} = 0$ Vdc, $T_A = T_L$ to T_H, unless otherwise noted
   All timing measurements refer to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Input clocks with duty cycles other than 50% affect bus performance.
3. This parameter is affected by clock stretching. Add n(t_{cyc}) to parameter value, where n = 1, 2, or 3 depending on values written to CSCSTR register or n = 1 for STRCH = 1 on KS parts.

13.3 84-Pin Plastic-Leaded Chip Carrier (Case 780)

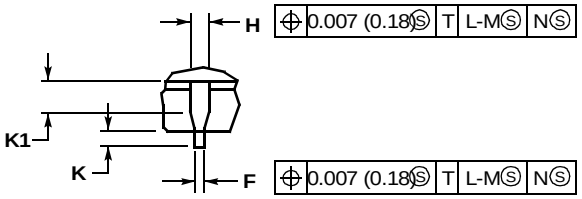




VIEW D-D



NOTES:
1. DATUMS L, M, AND N DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PACKAGE BODY AT MOLD PARTING LINE.
2. DIMENSION G1 TO BE MEASURED AT CLOSEST APPROACH OF LEAD TO DATUM T, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.25) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.94). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).



VIEW S

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.185	1.195	30.10	30.35
B	1.185	1.195	30.10	30.35
C	0.165	0.180	4.20	4.57
E	0.090	0.120	2.29	3.05
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	1.150	1.156	29.21	29.36
U	1.150	1.156	29.21	29.36
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.545	0.565	13.84	14.35
K1	0.060	---	1.52	---
R1	0.025	0.045	0.64	1.14

Section 15. Development Support

Motorola has developed tools for use in debugging and evaluating M68HC11 equipment. Specific development tools for use with the M68HC11K series include:

- M68HC11KEVS evaluation system
- M68HC711KPGMR programmer board
- M68HC711KEVB evaluation board

For more information about Motorola and third party development system hardware and software, contact one of the following:

- Local Motorola Sales Office
- World Wide Web at http://www.motorola.com/semiconductors