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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	3MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	62
Program Memory Size	24KB (24K x 8)
Program Memory Type	OTP
EEPROM Size	640 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.29x29.29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc711k4vfne3

List of Figures

Table 2-2. Port Signal Summary

Port/Bit	Single-Chip and Bootstrap Modes	Expanded and Special Test Modes
PA0	PA0/IC3	
PA1	PA1/IC2	
PA2	PA2/IC1	
PA3	PA3/OC5/IC4/and-or OC1	
PA4	PA4/OC4/and-or OC1	
PA5	PA5/OC3/and-or OC1	
PA6	PA6/OC2/and-or OC1	
PA7	PA7/PAI/and-or OC1	
PB[7:0]	PB[7:0]	ADDR[15:8]
PC[7:0]	PC[7:0]	DATA[7:0]
PD0	PD0/RxD	
PD1	PD1/TxD	
PD2	PD2/MISO	
PD3	PD3/MOSI	
PD4	PD4/SCK	
PD5	PD5/$\overline{SS}$	
PE[7:0]	PE[7:0]/AN[7:0]	
PF[7:0]	PF[7:0]	ADDR[7:0]
PG0	PG0	PG0/XA13
PG1	PG1	PG1/XA14
PG2	PG2	PG2/XA15
PG3	PG3	PG3/XA16
PG4	PG4	PG4/XA17
PG5	PG5	PG5/XA18
PG6	PG6	PG6
PG7	PG7	PG7/R/$\overline{W}$
PH0	PH0/PW1	
PH1	PH1/PW2	
PH2	PH2/PW3	
PH3	PH3/PW4	
PH4	PH4	PH4/CSIO
PH5	PH5	PH5/CSGP1
PH6	PH6	PH6/CSGP2
PH7	PH7	PH7/CSPROG

3.3.6.7 Non-Maskable Interrupt (X)

Setting the XIRQ mask (X) bit disables non-maskable interrupts from the XIRQ pin. Every reset sets the X bit by default and only a software instruction can clear it. When the processor recognizes a non-maskable interrupt, it stacks the registers, sets the X and I bits, and then fetches the interrupt vector. An interrupt service routine usually ends with a return from interrupt (RTI), which restores the registers to the values that were present before the interrupt occurred and clears the X bit. Only hardware or an acknowledge can set the X bit. Only software can clear the X bit (for example, the TAP instruction which transfers data from accumulator A to the condition code register). There is no hardware action for clearing X.

3.3.6.8 Stop Disable (S)

Setting the STOP disable (S) bit prevents the STOP instruction from putting the M68HC11 into a low-power stop condition. If the S bit is set, the CPU treats a STOP instruction as if it were a no-operation (NOP) instruction and continues to the next instruction.

NOTE: *S is set by reset and STOP is disabled by default.*

The STOP instruction can be cleared by using the TAP instruction which transfers data from accumulator A to the condition code register.

3.4 Data Types

The MC68HC11 CPU supports these data types:

- Bit data
- 8-bit and 16-bit signed and unsigned integers
- 16-bit unsigned fractions
- 16-bit addresses

A byte is eight bits wide and can be accessed at any byte location. A word is composed of two consecutive bytes with the most significant byte at the lower value address. Because the M68HC11 is an 8-bit CPU,

Three registers are involved in COP operation:

- The CONFIG register contains a bit which determines whether the COP system is enabled or disabled.
- The OPTION register contains two bits which determine the COP timeout period.
- The COPRST register must be written by software to reset the watchdog timer.

NOTE: *Throughout this manual, the registers are discussed by function. In the event that not all bits in a register are referenced, the bits that are not discussed are shaded.*

5.3.3.1 System Configuration Register

In normal modes, COP is enabled out of reset and does not depend on software action. To disable the COP system, set the NOCOP bit in the CONFIG register (see **Figure 5-1**). In special test and bootstrap operating modes, the COP system is initially inhibited by the disable resets (DISR) control bit in the TEST1 register. The DISR bit can subsequently be written to 0 to enable COP resets.

Address: $003F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ROMAD	1	CLKX	PAREN	NOSEC	NOCOP	ROMON	EEON
Reset:	—	1	—	—	1	—	—	—

Figure 5-1. System Configuration Register (CONFIG)

NOTE: *CONFIG is writable once in normal modes and writable at any time in special modes.*

NOCOP — COP System Disable Bit
0 = COP enabled
1 = COP disabled

Table 5-5. Interrupt and Reset Vector Assignments

Vector Address	Interrupt Source	CC Register Mask	Local Mask
FFC0, C1 — FFD4, D5	Reserved	—	—
FFD6, D7	SCI serial system: • SCI transmit complete • SCI transmit data register empty • SCI idle line detect • SCI receiver overrun • SCI receive data register full	I bit	 TCIE TIE ILIE RIE RIE
FFD8, D9	SPI serial transfer complete	I bit	SPIE
FFDA, DB	Pulse accumulator input edge	I bit	PAII
FFDC, DD	Pulse accumulator overflow	I bit	PAOVI
FFDE, DF	Timer overflow	I bit	TOI
FFE0, E1	Timer input capture 4/output compare 5	I bit	I4/O5I
FFE2, E3	Timer output compare 4	I bit	OC4I
FFE4, E5	Timer output compare 3	I bit	OC3I
FFE6, E7	Timer output compare 2	I bit	OC2I
FFE8, E9	Timer output compare 1	I bit	OC1I
FFEA, EB	Timer input capture 3	I bit	IC3I
FFEC, ED	Timer input capture 2	I bit	IC2I
FFEE, EF	Timer input capture 1	I bit	IC1I
FFF0, F1	Real-time interrupt	I bit	RTII
FFF2, F3	$\overline{\text{IRQ}}$ (external pin)	I bit	None
FFF4, F5	$\overline{\text{XIRQ}}$ pin	X bit	None
FFF6, F7	Software interrupt	None	None
FFF8, F9	Illegal opcode trap	None	None
FFFA, FB	COP failure	None	NOCOP
FFFC, FD	Clock monitor fail	None	CME
FFFE, FF	RESET	None	None

Many interrupt sources set associated flag bits when interrupts occur. These flags are usually cleared during the course of normal interrupt service. For example, the normal response to an RDRF interrupt request in the SCI is to read the SCI status register to check for receive errors, then read the received data from the SCI data register. It is precisely these two steps which clear RDRF, so no extra steps are required.

An interrupt can be recognized at any time after it is enabled by its local mask, if any, and by the global mask bit in the CCR. The CPU responds to an interrupt at the completion of the instruction being executed. Since the number of clock cycles in the instruction varies, so does interrupt latency. The CPU pushes the contents of its registers onto the stack in the order shown in **Table 5-6**. After the CCR value is stacked, the I bit is set (and the X bit as well if $\overline{\text{XIRQ}}$ is pending) to inhibit further interrupts. The CPU fetches the interrupt vector for the highest priority pending source, and execution continues at the address specified by the vector. The interrupt service routine ends with the return-from-interrupt (RTI) instruction, which tells the CPU to pull the saved registers from the stack in reverse order so that normal program execution can resume.

Table 5-6. Stacking Order on Entry to Interrupts

Memory Location	CPU Registers
SP	PCL
SP – 1	PCH
SP –2	IYL
SP – 3	IYH
SP – 4	IXL
SP – 5	IXH
SP – 6	ACCA
SP – 7	ACCB
SP – 8	CCR

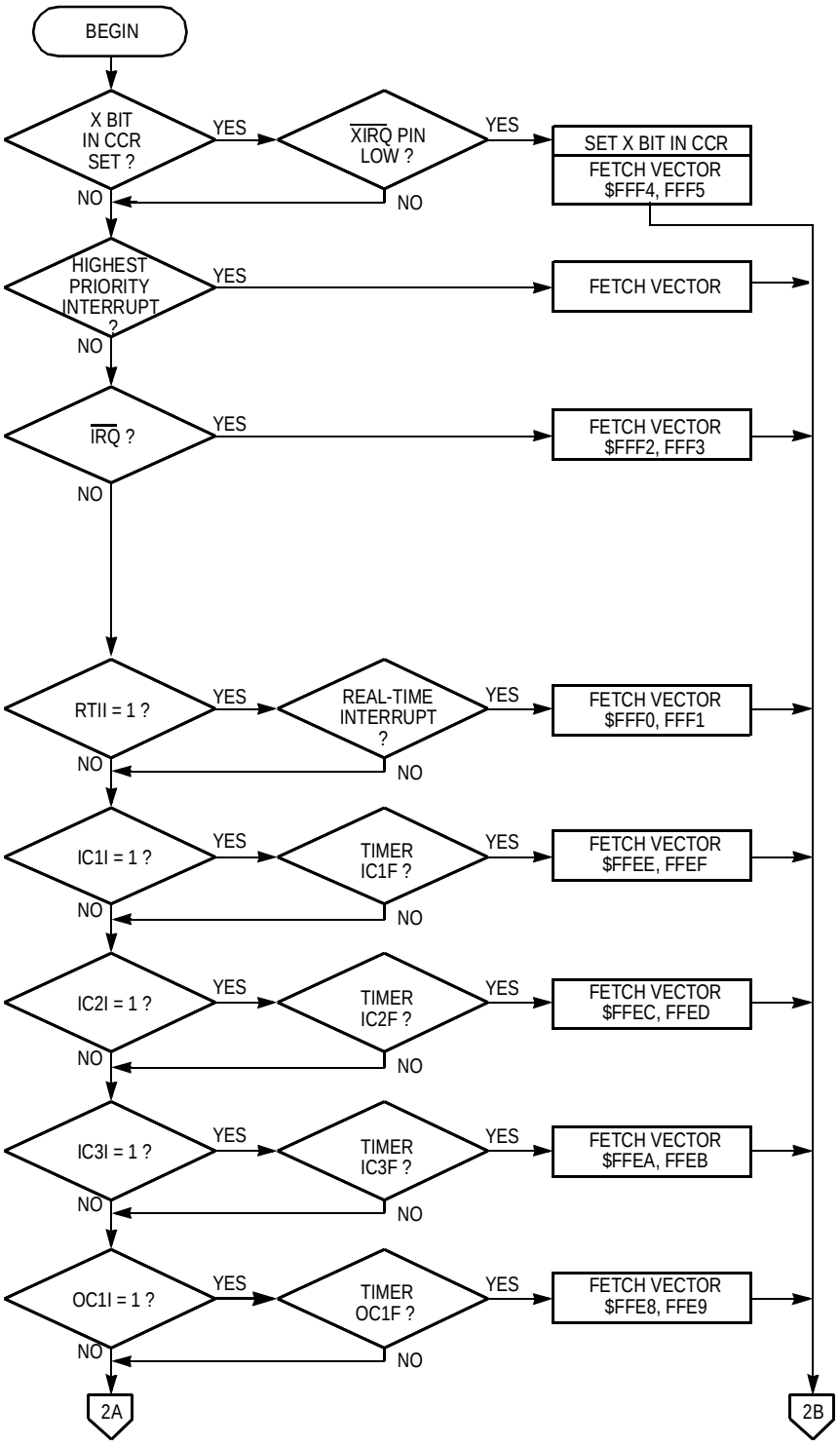


Figure 5-9. Interrupt Priority Resolution (Sheet 1 of 2)

6.7 Port E

Port E, PE[7:0], is the only port that functions as input only, and its pins are configured as high-impedance inputs out of reset. It also serves as the analog input for the analog-to-digital converter when this function is enabled by software (see **Section 10. Analog-to-Digital (A/D) Converter**).

NOTE: *PORT E should not be read during the sample portion of an A/D conversion.*

Address: $000A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	PE7	PE6	PE5	PE4	PE3	PE2	PD1	PD0
Reset:	Undefined after reset							
Alternate Pin Function:	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

Figure 6-10. Port E Data Register (PORTE)

7.5 Receive Operation

During receive operations, data from the TxD pin is shifted into the serial shift register. A completed word is parallel-loaded to a receive data register (RDR), which can be read through SCDRH/L. This double-buffered operation allows reception of the current character while the MCU reads the previous character.

The SCI receiver has seven status flags, summarized in Table 7-1.

Table 7-1. SCI Receiver Flags

Flag	Name	Set When	Interrupt Enable Bit
RDRF	Receive data register full	Character transferred from shift register to RDR	RIE
IDLE	Idle-line detected	Active transmit line goes idle	ILIE
OR	Overrun error	Character ready for RDR while previous character unread	RIE
NF	Noise error	Samples of data bit not unanimous	—
FE	Frame error	0 detected where stop bit expected	—
PF	Parity error	Calculated parity does not match data parity bit	—
RAF	Receiver active	A character is being received	—

Three of the flags can generate interrupt requests if the corresponding enable bits in SCCR2 are set. The status flags are set by the SCI logic in response to specific conditions in the receiver. These flags can be read (polled) at any time by software. Each bit except RAF is cleared by reading SCSR1 and SCDR sequentially.

- The receive data register full (RDRF) flag is set when the last bit of a character is received and data is transferred from the shift register to the RDR.
- The IDLE flag is set after a transition on the RxD line from an active state to an idle state. This prevents repeated interrupts during the time RxD remains idle.

7.7 Short Mode Idle Line Detection

This feature can increase system communication speed by reducing the amount of time between messages. Setting the ILT bit in SCCR1 allows the SCI receiver to detect the consecutive 1s of an idle period before the stop bit of an incoming character is received. If the last few bits of the character are 1s, they are counted as the first high bits in the frame of 1s comprising the idle period following the character.

NOTE: *Extra care may be needed to prevent premature detection of an idle line condition.*

7.8 Baud Rate Selection

The baud rate generator for the SCI includes a 13-bit modulus prescaler driven by the system crystal clock (EXTAL). Writing to the SCI baud rate register (SCBDH/L) selects the prescaler value. See **Figure 7-4**.

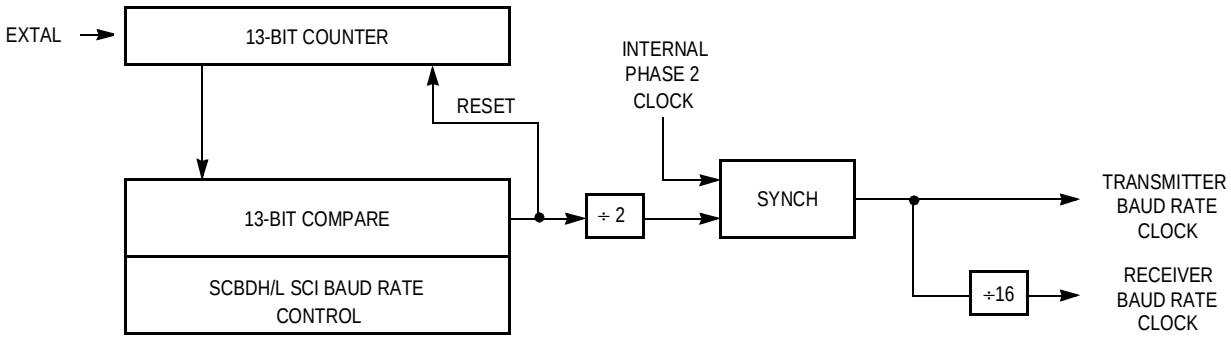


Figure 7-4. SCI Baud Generator Circuit Diagram

TE — Transmitter Enable Bit

When TE goes from 0 to 1, one unit of idle character time (logic 1) is queued as a preamble.

0 = Transmitter disabled
1 = Transmitter enabled

RE — Receiver Enable Bit

0 = Receiver disabled
1 = Receiver enabled

RWU — Receiver Wakeup Control

0 = Normal SCI receiver operation
1 = Wakeup is enabled and receiver interrupts are inhibited.

SBK — Send Break Bit

At least one character time of break is queued and sent each time SBK is written to 1. Multiple breaks may be sent if the transmitter is idle at the time the SBK bit is toggled on and off, as the baud rate clock edge could occur between writing the 1 and writing the 0 to SBK.

0 = Break generator off
1 = Break codes generated as long as SBK = 1

7.9.4 Serial Communication Status Register 1

The SCSR provides flags for various SCI conditions which can be polled or used to generate SCI system interrupts. To clear any set flag, read SCSR while the flag is set and then write to SCDR.

Address $0074

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
Reset:	1	1	0	0	0	0	0	0

Figure 7-9. SCI Status Register 1 (SCSR1)

8.6.2 Serial Peripheral Status Register

Address: $0029

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	SPIF	WCOL	0	MODF	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 8-4. Serial Peripheral Status Register (SPSR)

SPIF — SPI Transfer Complete Flag

SPIF is set upon completion of data transfer between the processor and the external device. If SPIF goes high, and if SPIE is set, a serial peripheral interrupt is generated. To clear the SPIF bit, read the SPSR with SPIF set, then access the SPDR. Unless SPSR is read (with SPIF set) first, attempts to write SPDR are inhibited.

WCOL — Write Collision Bit

Clearing the WCOL bit is accomplished by reading the SPSR (with WCOL set) followed by an access of SPDR.

0 = No write collision
1 = Write collision

MODF — Mode Fault Bit

To clear the MODF bit, read the SPSR (with MODF set), then write to the SPCR.

0 = No mode fault
1 = Mode fault

9.4.5 Pulse Accumulator Control Register

Address: $0026

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	PAEN	PAMOD	PEDGE	0	I4/O5	RTR1	RTR0
Reset:	0	0	0	0	0	0	0	0

Figure 9-7. Pulse Accumulator Control Register (PACTL)

I4/O5 — Input Capture 4/Output Compare 5 Bit
0 = Configure PA3 as OC5
1 = Configure PA3 as IC4

To configure PA3 as input compare 4, clear DDA3 and set I4/05. To configure PA3 as output compare 5, set DDA3 and clear I4/05. If the DDA3 bit is set (configuring PA3 as an output) and IC4 is enabled, writing a one to TI4/O5 causes an input capture. Writing to TI4/O5 has no effect when DDA3 is cleared and/or OC5 is enabled.

9.5 Input Capture (IC)

The input capture function records the time an external event occurs by latching the value of the free-running counter into one of the timer input capture (TIC) registers when a selected edge is detected at its associated timer input pin. Software can store latched values and use them to compute the period and duration of events. For example, by storing the times of successive edges of an incoming signal, software can determine the period and pulse width of a signal. To measure the period, two successive edges of the same polarity are captured. To measure pulse width, two alternate polarity edges are captured.

Capture requests are latched on the opposite half cycle of PH2 from when the timer counter is being incremented. This synchronization process introduces a delay between edge occurrence and counter value detection. Because these delays offset each other when the time between two edges is measured, they can be ignored. There is a similar delay for output compare between the actual compare point and when the output pin changes state.

9.6 Output Compare (OC)

The output compare (OC) function generates a programmed action when the 16-bit counter reaches a specified value. Each of the five output compare functions contains a separate 16-bit timer output compare (TOC) register and a dedicated 16-bit comparator. Each TOC register is set to $FFFF on reset. When an OC channel is enabled, the value in its TOC register is compared to the free-running counter value during each E-clock cycle. When the values match, the channel's output compare flag is set in timer interrupt flag 1 (TFLG1). If the channel's interrupt is enabled in the timer interrupt mask register 1 (TMSK1), an interrupt is generated. Also, the corresponding timer output pin is toggled or driven to a specified logic level. This pin activity occurs on each successful compare, whether or not the OCxF flag in the TFLG1 register was previously cleared.

The pin action for each of the OC channels [5:2] is controlled by a pair of bits (OMx and OLx) in the TCTL1 register and affects only the channel's associated pin. A successful OC1 compare can affect any or all five of the OC pins. The action taken when a match is found for OC1 is controlled by two 8-bit registers:

- Output compare 1 mask register (OC1M)
- Output compare 1 data register (OC1D)

OC1M specifies which port A outputs are to be used, and OC1D specifies the data placed on these port pins.

Although the M68HC11K series devices have four built-in pulse-width modulation (PWM) channels (**9.9 Pulse-Width Modulator (PWM)**), the output compare function can be used to produce an additional pulse-width modulated waveform. To produce a pulse of a specific duration:

- Write a value to the output compare register that represents the time the leading edge of the pulse is to occur.
- Use OC1D to select either a high or low output, depending on the polarity of the pulse being produced.

Timing System

The MULT bit in ADCTL determines whether one or four channels are converted. When MULT = 0, one channel is converted. The selected channel is sampled and the conversion results are written to ADR1; the same channel is sampled again, and the conversion results are stored in ADR2, and so on. In continuous mode, the same channel continues to be sampled and converted. Setting the MULT bit converts four different channels; each result register contains the conversion result of a different channel. In continuous mode, the same four channels are converted in each sequence.

ADCTL bits [3:0] select the particular channel(s) to be converted. See **Table 10-1**.

Table 10-1. A/D Converter Channel Selection

Channel Select Control Bits CD:CC:CB:CA	Channel Signal	Result Location When MULT = 1
0000	AN0	ADR1
0001	AN1	ADR2
0010	AN2	ADR3
0011	AN3	ADR4
0100	AN4	ADR1
0101	AN5	ADR2
0110	AN6	ADR3
0111	AN7	ADR4
10XX	Reserved	—
1100	V_{RH}(1)	ADR1
1101	V_{RL}(1)	ADR2
1110	(V_{RH})/2(1)	ADR3
1111	Reserved(1)	ADR4

1. Used for factory testing

Address: $0039

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ADPU	CSEL	IRQE	DLY(1)	CME	FCME	CR1	CR0
Reset:	0	0	0	1	0	0	0	0

1. DLY can be written only once in the first 64 cycles out of reset in normal modes or at any time in special modes.

Figure 10-3. System Configuration Options Register (OPTION)

ADPU — A/D Power-up
0 = A/D powered down
1 = A/D powered up

CSEL — Clock Select
0 = A/D and EEPROM use system E clock.
1 = A/D and EEPROM use internal RC clock.

10.4.2 A/D Control/Status Register

All bits in this register can be read or written except bit 7, which is a read-only status indicator, and bit 6, which always reads as 0. Writing to ADCTL initiates a conversion, aborting any conversion in progress.

Address: $0030

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CCF		SCAN	MULT	CD	CC	CB	CA
Write:								
Reset:	0	0	U	U	U	U	U	U

= Unimplemented U = Unaffected by reset

Figure 10-4. Analog-to-Digital Control/Status Register (ADCTL)

11.4.2 Input/Output Chip Select

The I/O chip select (CSIO) is programmable for a 4-Kbyte size located at addresses $1000–$1FFF or 8-Kbyte size located at addresses $0000–$1FFF. The default active-low polarity can be changed to active high by setting the IOPL bit in CSCTL. Default validity during high E clock can be changed to address valid time by setting the IOCSA bit in CSCTL. Clock stretching can be set from zero to three cycles (See **11.4.5 Clock Stretching**). CSIO is disabled out of reset.

Address: $005B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	IOEN	IOPL	IOCSA	IOSZ	GCSPR	PCSEN	PCSZA	PCSZB
Reset:	0	0	0	0	0	1	0	0

Figure 11-6. Chip-Select Control Register (CSCTL)

IOEN — I/O Chip-Select Enable Bit
0 = CSIO is disabled and port H bit 4 is GPIO.
1 = CSIO is enabled and uses port H bit 4.

IOPL — I/O Chip-Select Polarity Select Bit
0 = CSIO active low
1 = CSIO active high

IOCSA — I/O Chip-Select Address Valid Bit
0 = CSIO is valid during E-clock high time.
1 = CSIO is valid during address valid time.

IOSZ — I/O Chip-Select Size Select Bit
0 = CSIO size is four Kbytes at $1000–$1FFF.
1 = CSIO size is eight Kbytes at $0000–$1FFF.

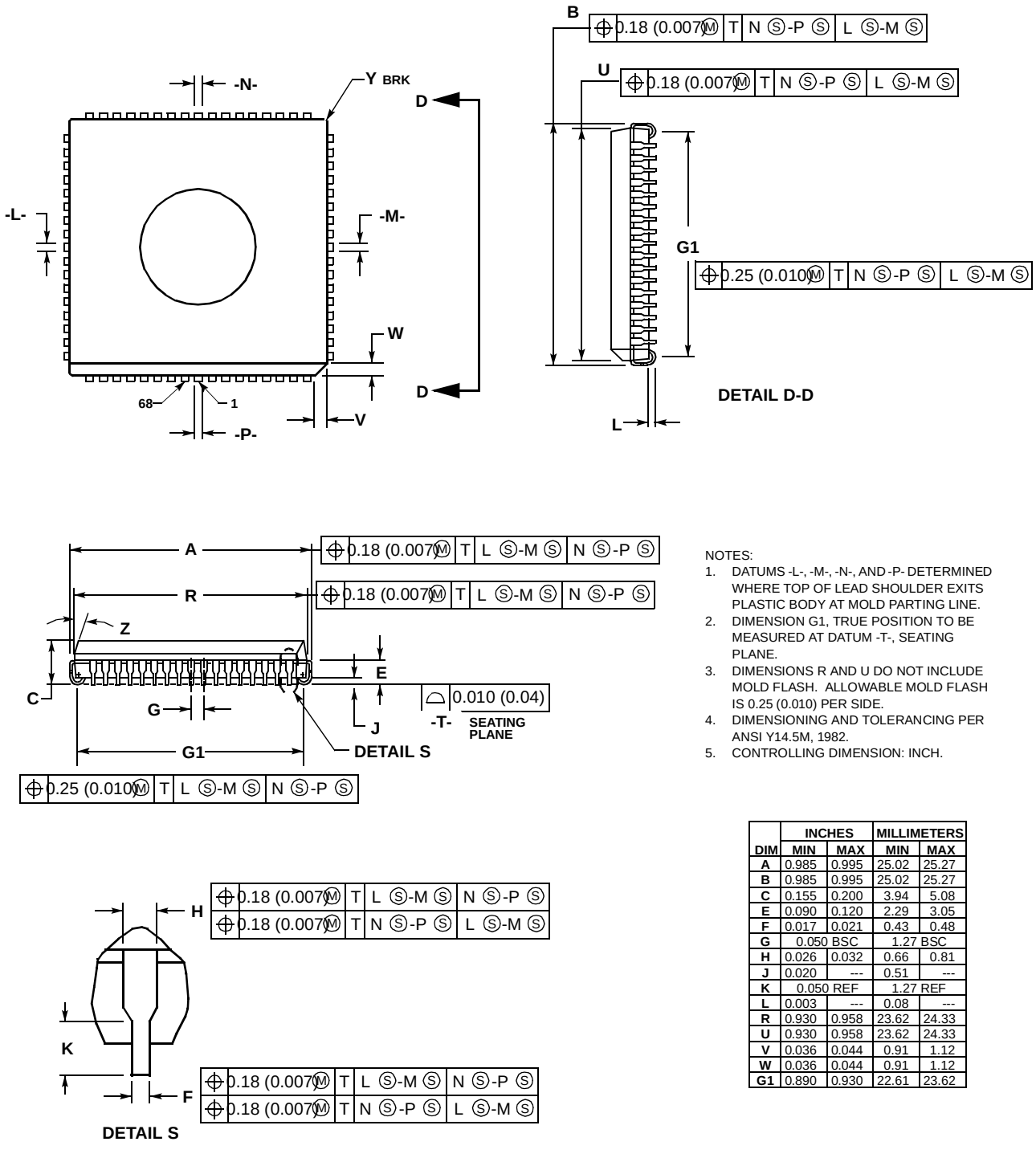
Mechanical Data

The diagrams included in this section show the latest package specifications available at the time of this publication. To make sure that you have the latest information, contact one of the following:

- Local Motorola Sales Office
- World Wide Web at http://www.motorola.com/semiconductors

Follow the World Wide Web on-line instructions to retrieve the current mechanical specifications.

13.8 68-Pin J-Cerquad (Case 779A)



NOTES:
1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.985	0.995	25.02	25.27
B	0.985	0.995	25.02	25.27
C	0.155	0.200	3.94	5.08
E	0.090	0.120	2.29	3.05
F	0.017	0.021	0.43	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.050 REF		1.27 REF	
L	0.003	---	0.08	---
R	0.930	0.958	23.62	24.33
U	0.930	0.958	23.62	24.33
V	0.036	0.044	0.91	1.12
W	0.036	0.044	0.91	1.12
G1	0.890	0.930	22.61	23.62