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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	4MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	62
Program Memory Size	24KB (24K x 8)
Program Memory Type	OTP
EEPROM Size	640 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.29x29.29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc711k4vfne4

MC68HC11K Family

Technical Data

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Section 9. Timing System

Port B provides the high-order address byte (Addr[15:8]), port F the low-order address byte (Addr[7:0]), port C the data bus (Data[7:0]), and port G pin 7 the read/write line (R/$\overline{W}$) which controls direction of data flow.

Additionally, the E clock output can be used to synchronize external decoders for enable signals.

Expanded mode also enables these two special features available only on the K4 Family devices:

1. Memory expansion uses port G[5:0] to increase the available external address space to 1 Mbyte.
2. Four chip-select lines on port H[7:4] simplify selection of external memory devices.

Both of these features are described in **Section 11. Memory Expansion and Chip Selects**.

4.5.3 Bootstrap Mode

Resetting the MCU in special bootstrap mode selects a reset vector to a special ROM bootloader program at addresses $BE00–$BFFF. The bootloader program is used to download code, such as programming algorithms, into on-chip RAM through the SCI. To do this:

1. Send a synchronization character (see **Table 4-2**) to the SCI receiver at the specified baud rate.
2. Download up to 768 bytes (1 Kbyte for KS2) of program data, which the CPU places into RAM starting at $0080 and also echoes back on the TxD signal. The bootloader program ends the download after the RAM is full or when the received data line is idle for at least four character times. See **Table 4-2**.

When loading is complete, the MCU jumps to location $0080 and begins executing the code. Interrupt vectors are directed to RAM, which allows the use of interrupts through a jump table. The SCI transmitter requires an external pullup resistor since it is part of port D, which the bootloader configures for wired-OR operation.

4.8.2.2 EEPROM Bulk Erase

```
BULKE   LDAB    #$06
        STAB    $003B   Set EELAT and ERASE.
        STAA    $0,X    Store any data to any EEPROM address
        LDAB    #$07
        STAB    $002B   Set EEPGM bit as well
                        to enable EEPROM programming voltage
        JSR     DLY10   Delay 10 ms
        CLR     $003B   Turn off programming voltage and set
                        to READ mode
```

4.8.2.3 EEPROM Row Erase

```
ROWE    LDAB    #$07
        STAB    $003B   Set EELAT, ERASE and ROW.
        STAA    $0,X    Store any data to any EEPROM address
                        in row
        LDAB    #$07
        STAB    $002B   Set EEPGM bit as well
                        to enable EEPROM programming voltage
        JSR     DLY10   Delay 10 ms
        CLR     $003B   Turn off programming voltage and set
                        to READ mode
```

4.8.2.4 EEPROM Byte Erase

```
BYTEE   LDAB    #$16
        STAB    $003B   Set EELAT, ERASE and BYTE.
        STAA    $0,X    Store any data to targeted EEPROM
                        address
        LDAB    #$17
        STAB    $002B   Set EEPGM bit as well
                        to enable EEPROM programming voltage
        JSR     DLY10   Delay 10 ms
        CLR     $003B   Turn off programming voltage and set
                        to READ mode
```

  - The RDRF, IDLE, OR, NF, FE, PF, and RAF receive-related status bits are cleared.

- Serial peripheral interface (SPI)
  - The SPI system is disabled by reset.
  - The port pins associated with this function default to being general-purpose I/O lines.
- Analog-to-digital (A/D) converter
  - The ADPU bit in the OPTION register is cleared, disabling the A/D system.
  - The conversion complete flag in the ADCTL register is also cleared.
- System
  - The external $\overline{\text{IRQ}}$ pin has the highest I-bit interrupt priority because PSEL[4:0] in the HPRIO register are initialized with the value %00110 (where % indicates a binary value).
  - The RBOOT, SMOD, and MDA bits in the HPRIO register reflect the status of the MODB and MODA inputs at the rising edge of reset.
  - The $\overline{\text{IRQ}}$ pin is configured for level-sensitive operation for wired-OR systems.
  - The DLY control bit in the OPTION register is set, enabling oscillator startup delay after recovery from stop mode.
  - The clock monitor system is disabled because the CME and FCME bits in the OPTION register are cleared.

5.5 Interrupts

The MCU has 18 interrupt vectors that support 22 interrupt sources. The 19 maskable interrupts are generated by on-chip peripheral systems. They are recognized when the I bit in the CCR is clear. The three non-maskable interrupt sources are illegal opcode trap, software interrupt, and $\overline{\text{XIRQ}}$ pin. **Table 5-5** lists the interrupt sources and vector assignments for each source.

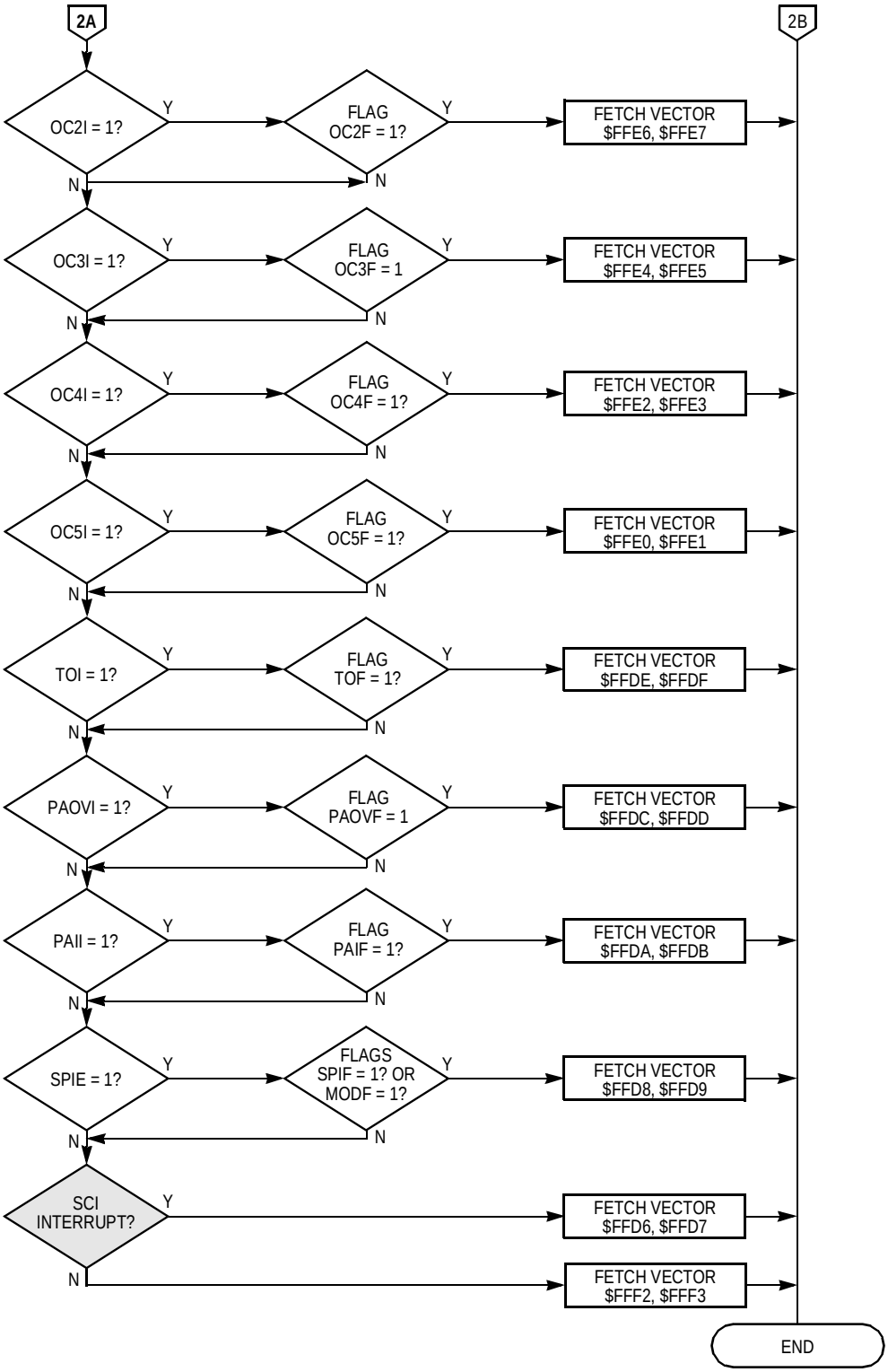


Figure 5-9. Interrupt Priority Resolution (Sheet 2 of 2)

to restart the system, a normal reset sequence results and all pins and registers are reinitialized.

To use the $\overline{\text{IRQ}}$ pin as a means of recovering from STOP, the I bit in the CCR must be clear ($\overline{\text{IRQ}}$ not masked). The $\overline{\text{XIRQ}}$ pin can be used to wake up the MCU from STOP regardless of the state of the X bit in the CCR, although the state of this bit does affect the recovery sequence. If X is clear ($\overline{\text{XIRQ}}$ not masked), the MCU executes a normal XIRQ service routine. If X is set ($\overline{\text{XIRQ}}$ masked or inhibited), then processing continues with the instruction that immediately follows the STOP instruction, and no $\overline{\text{XIRQ}}$ interrupt service is requested or pending.

Executing a STOP instruction requires special consideration when the clock monitor is enabled. Because the stop function halts all clocks, the clock monitor function will generate a reset sequence if it is enabled at the time the stop mode was initiated. To prevent this, clear the CME and FCME bits in the OPTION register before executing a STOP instruction to disable the clock monitor. After recovery from STOP, set the CME bit to enable the clock monitor.

Systems using the internal oscillator require a delay after restart upon leaving STOP to allow the oscillator to stabilize. If a stable external oscillator is used, the DLY control bit in the OPTION register can be used to bypass this startup delay (see **Figure 5-11**). Reset sets the DLY control bit; it can be cleared during initialization. Do not use reset to recover from STOP if the DLY is to be bypassed, since reset sets the DLY bit again, causing the restart delay. This same delay will follow a power-on reset, regardless of the state of the DLY control bit, but does not apply to a reset while the clocks are running.

Address: $0039

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ADPLE	DSEL	IRQE(1)	DLY(1)	CME	FCME(1)	CR1(1)	CR0(1)
Reset:	0	0	0	1	0	0	0	0

1. Can be written only once in first 64 cycles out of reset in normal modes or at any time in special modes

Figure 5-11. System Configuration Options Register (OPTION)

6.3 Port A

Port A provides the I/O lines for the timer functions and pulse accumulator. The eight port A bits (PA[7:0]) are configured as high-impedance general-purpose inputs out of reset. Writes to DDRA can change any of the bits to outputs. Writes to timer registers enable the various timer functions (see **Section 9. Timing System**).

Address: $0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Reset:	Undefined after reset							
Alternate Pin Function:	PAI	OC2	OC3	OC4	IC4/OC5	IC1	IC2	IC3
And/or:	OC1	OC1	OC1	OC1	OC1	—	—	—

Figure 6-1. Port A Data Register (PORTA)

Address: $0001

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0
Reset:	0	0	0	0	0	0	0	0

Figure 6-2. Port A Data Direction Register (DDRA)

DDA[7:0] — Data Direction for Port A Bits

0 = Input

1 = Output

6.11 Internal Pullup Resistors

M68HC11KS series devices contain selectable internal pullup resistors for ports B, F, G, and H. The resistors for each port are enabled by setting the corresponding bit in the PPAR register. PPAR itself must be enabled by setting the PAREN bit in the system configuration register (CONFIG). Refer to **Figure 6-17** and **Figure 6-18**.

Address: $002C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	HPPUE	GPPUE	FPPUE	BPPUE
Write:								
Reset:	0	0	0	0	1	1	1	1

Figure 6-17. Port Pullup Assignment Register (PPAR)

xPPUE — Port x Pin Pullup Enable Bits

Only active when enabled by the PAREN bit in the CONFIG register

0 = Port x pin on-chip pullup devices disabled

1 = Port x pin on-chip pullup devices enabled

NOTE: *FPPUE and BPPUE do not apply in expanded mode because port F and B are address outputs.*

Address: $003F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	ROMAD	1	CLKX	PAREN	NOSEC	NOCOP	ROMON	EEON
Write:								
Reset:	—	1	—	—	1	—	—	—

Figure 6-18. System Configuration Register (CONFIG)

NOTE: *CONFIG is writable once in normal modes and writable at any time in special modes.*

PAREN — Pullup Assignment Register Enable Bit

0 = PPAR register disabled

1 = PPAR register enabled; pullups can be enabled through PPAR

PE — Parity Enable Bit
0 = Parity disabled
1 = Parity enabled

PT — Parity Type Bit
0 = Parity even (even number of 1s causes parity bit to be 0, odd number of 1s causes parity bit to be 1)
1 = Parity odd (odd number of 1s causes parity bit to be 0, even number of 1s causes parity bit to be 1)

7.9.3 Serial Communications Control Register 2

Address $0073

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
Reset:	0	0	0	0	0	0	0	0

Figure 7-8. SCI Control Register 2 (SCCR2)

TIE — Transmit Interrupt Enable Bit
0 = TDRE interrupts disabled
1 = SCI interrupt is requested when the TDRE status flag is set.

TCIE — Transmit Complete Interrupt Enable Bit
0 = TC interrupts disabled
1 = SCI interrupt is requested when the TC status flag is set.

RIE — Receiver Interrupt Enable Bit
0 = RDRF and OR interrupts disabled
1 = SCI interrupt is requested when the RDRF flag or OR flag is set.

ILIE — Idle Line Interrupt Enable Bit
0 = IDLE interrupts disabled
1 = SCI interrupt is requested when the IDLE status flag is set.

9.4.2 Timer Interrupt Flag 2 Register

Address: $0025

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TOF	RTIF	PAOVF	PAIF	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

Figure 9-4. Timer Interrupt Flag 2 (TFLG2)

Clear each flag by writing a 1 to the corresponding bit position.

TOF — Timer Overflow Flag

Set when TCNT changes from $FFFF to $0000.

9.4.3 Timer Interrupt Mask 2 Register

Address: $0024

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
Reset:	0	0	0	0	0	0	0	0

Figure 9-5. Timer Interrupt Mask 2 (TMSK2)

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2.

TOI — Timer Overflow Interrupt Enable Bit

0 = Timer overflow interrupt disabled

1 = An interrupt request is generated when TOF is set.

9.6.2 Timer Input Capture 4/Output Compare 5 Register

	Bit 7	6	5	4	3	2	1	Bit 0
Address:	$001E — TI4/O5 (High)							
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1
Address:	$001F — TI4/O5 (Low)							
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1

Figure 9-14. Timer Input Capture 4/Output Compare 5 Register (TI4/O5)

Functions as the output compare register for OC5 when PA3 is configured for output compare 5. This register is 16-bit read-write. It can be used as a storage location if it is not used for output compare or input capture.

9.6.3 Timer Interrupt Flag 1 Register

Address: $0023

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F
Reset:	0	0	0	0	0	0	0	0

Figure 9-15. Timer Interrupt Flag 1 Register (TFLG1)

Clear each flag by writing a 1 to the corresponding bit position.

OCxF — Output Compare x Flag

Set each time the counter matches output compare x value.

I4/O5F — Input Capture 4/Output Compare 5 Flag

Set each time the counter matches output compare 5 value if OC5 is enabled.

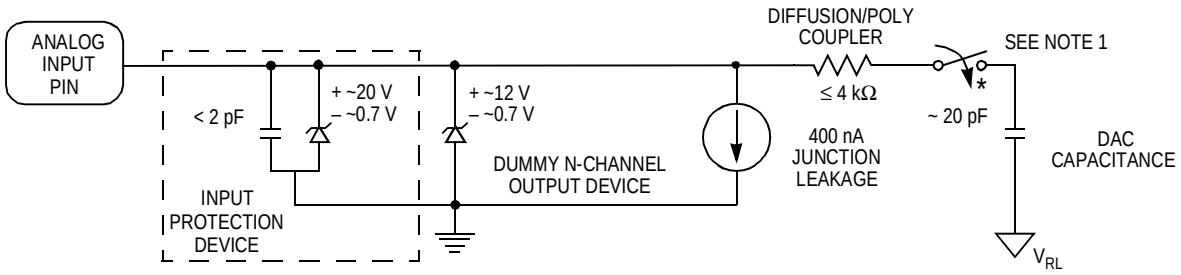
Timing System

10.5 Design Considerations

This section discusses design considerations.

10.5.1 A/D Input Pins

Port E pins can also be used as general-purpose digital inputs. Digital reads of port E pins are not recommended during the sample portion of an A/D conversion cycle, when the gate signal to the N-channel input is on. No P-channel devices are directly connected to either input pins or reference voltage pins, so voltages above V_{DD} do not cause a latchup problem, although current should be limited according to maximum ratings. Refer to **Figure 10-6**.



Note 1. This analog switch is closed only during the 12-cycle sample time.

Figure 10-6. Electrical Model of an A/D Input Pin (Sample Mode)

10.5.2 Operation in Stop and Wait Modes

If a conversion sequence is in progress when either the stop or wait mode is entered, the conversion of the current channel is suspended. When the MCU resumes normal operation, that channel is resampled and the conversion sequence is resumed. As the MCU exits the wait mode, the A/D circuits are stable and valid results can be obtained on the first conversion. However, in stop mode, all analog bias currents are disabled and it is necessary to allow a stabilization period when leaving stop mode. If stop mode is exited with a delay (DLY = 1), there is enough time for these circuits to stabilize before the first conversion. If stop mode is exited with no delay (DLY bit in OPTION register = 0), allow 10 ms for the A/D circuitry to stabilize to avoid invalid results.

11.4.3.3 General-Purpose Chip Select 1 Control Register

Address: $005D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	G1DG2	G1DPC	G1POL	G1AV	G1SZA	G1SZB	G1SCC	G1SZD
Reset:	0	0	0	0	0	0	0	0

Figure 11-9. General-Purpose Chip Select 1 Control Register (GPCS1C)

G1POL — General-Purpose Chip Select 1 Polarity Select Bit

0 = CSGP1 active low

1 = CSGP1 active high

G1AV — General-Purpose Chip Select 1 Address Valid Select Bit

0 = CSGP1 is valid during E high time.

1 = CSGP1 is valid during address valid time.

G1SZ[A:D] — General-Purpose Chip Select 1 Size Bits

They select the range of GPCS1. Refer to **Table 11-6**.

Table 11-6. General-Purpose Chip Select 1 Size Control

G1SZ[A:D]	Size (Bytes)	Valid Bits (MXGS1 = 0)	Valid Bits (MXGS1 = 1)
0 0 0 0	Disabled	None	None
0 0 0 1	2 K	G1A[15:11]	G1A[18:11]
0 0 1 0	4 K	G1A[15:11]	G1A[18:12]
0 0 1 1	8 K	G1A[15:13]	G1A[18:13]
0 1 0 0	16 K	G1A[15:14]	G1A[18:14]
0 1 0 1	32 K	G1A[15]	G1A[18:15]
0 1 1 0	64 K	None	G1A[18:16]
0 1 1 1	128 K	None	G1A[18:17]
1 0 0 0	256 K	None	G1A18
1 0 0 1	512 K	None	None
1 0 1 0	Follow window 1	None	None
1 0 1 1	Follow window 2	None	None
1100–1111	Default to 512 K	None	None

12.9 Peripheral Port Timing

Characteristic[1]	Symbol	1.0 MHz		2.0 MHz		3.0 MHz		4.0 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Frequency of operation (E clock)	f_o	dc	1.0	dc	2.0	dc	3.0	dc	4.0	MHz
E-clock period	t_{cyc}	1000	—	500	—	333	—	250	—	ns
Peripheral data setup time[2] MCU read of ports A, B, C, D, E, F, G, and H	t_{PDSU}	100		100		100		100		ns
Peripheral data hold time MCU read of ports A, B, C, D, E, F, G, and H	t_{PDH}	50	—	50	—	50	—	50	—	ns
Delay time, peripheral data write Standard devices MCU write to port A, B, G, and H MCU write to ports C, D, and F (t_{PWD} = 1/4 t_{cyc} + 100 ns) Extended voltage MCU write to port A, B, G, and H MCU write to ports C, D, and F (t_{PWD} = 1/4 t_{cyc} + 150 ns)	t_{PWD}	— — — —	200 350 250 400	— — — —	200 225 250 225	— — — —	200 183 250 233	— — — —	200 162 — —	ns

1. V_{DD} = 4.5 to 5.5 Vdc for standard devices, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H
   All timing measurements refer to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Ports C and D timing is valid only in active drive mode. (CWOM and DWOM bits are cleared in OPT2 and SPCR registers, respectively.)

12.11 Expansion Bus Timing

Num	Characteristic[1]	Symbol	2.0 MHz		3.0 MHz		4.0 MHz		Unit
			Min	Max	Min	Max	Min	Max	
	Frequency of operation (E clock)[2]	f_o	dc	2.0	dc	3.0	dc	4.0	MHz
1	Cycle time, $t_{cyc} = 1/f_o$	t_{cyc}	500	—	333	—	250	—	ns
2	Pulse width, E low, $PW_{EL} = 1/2\ t_{cyc} - 20$ ns	PW_{EL}	230	—	147	—	105	—	ns
3	Pulse width, E high[3] $PW_{EH} = 1/2\ t_{cyc} - 25$ ns	PW_{EH}	225	—	142	—	100	—	ns
4A 4B	E clock Rise time Fall time	 t_r t_f	 — —	 20 20	 — —	 20 18	 — —	 20 15	ns
9	Address hold time, $t_{AH} = 1/8\ t_{cyc} - 10$ ns	t_{AH}	53	—	32	—	21	—	ns
11	Address delay time, $t_{AD} = 1/8\ t_{cyc} + 40$ ns	t_{AD}	—	103	—	82	—	71	ns
12	Address valid time to E rise $t_{AV} = PW_{EL} - t_{AD}$	t_{AV}	128	—	65	—	34	—	ns
17	Read data setup time	t_{DSR}	30	—	30	—	20	—	ns
18	Read data hold time	t_{DHR}	0	—	0	—	0	—	ns
19	Write data delay time	t_{DDW}	—	40	—	40	—	40	ns
21	Write data hold time, $t_{DHW} = 1/8\ t_{cyc}$	t_{DHW}	63	—	42	—	31	—	ns
29	MPU address access time[3] $t_{ACCA} = t_{cyc} - t_f - t_{DSR} - t_{AD}$	t_{ACCA}	348	—	203	—	144	—	ns
39	Write data setup time[3] $t_{DSW} = PW_{EH} - t_{DDW}$	t_{DSW}	185	—	102	—	60	—	ns
50	E valid chip-select delay time	t_{ECSD}	—	40	—	40	—	40	ns
51	E valid chip-select access time[3] $t_{ECSA} = PW_{EH} - t_{ECSD} - t_{DSR}$	t_{ECSA}	155	—	72	—	40	—	ns
52	Chip select hold time	t_{CH}	0	20	0	20	0	20	ns
54	Address valid chip-select delay time $t_{ACSD} = 1/4\ t_{cyc} + 40$ ns	t_{ACSD}	—	165	—	123	—	103	ns
55	Address valid chip-select access time $t_{ACSA} = t_{cyc} - t_f - t_{DSR} - t_{ACSD}$[3]	t_{ACSA}	285	—	162	—	113	—	ns
56	Address valid to chip-select time	t_{AVCS}	10	—	10	—	10	—	ns
57	Address valid to data three-state time	t_{AVDZ}	—	10	—	10	—	10	ns

1. $V_{DD} = 5.0 \pm 10\%$, $V_{SS} = 0$ Vdc, $T_A = T_L$ to T_H, unless otherwise noted
   All timing measurements refer to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Input clocks with duty cycles other than 50% affect bus performance.
3. This parameter is affected by clock stretching. Add n(t_{cyc}) to parameter value, where n = 1, 2, or 3 depending on values written to CSCSTR register or n = 1 for STRCH = 1 on KS parts.

Section 14. Ordering Information

Use Table 14-1 to determine part numbers when placing an order.

Table 14-1. M68HC11K Family Devices

Device Number	ROM or EPROM	RAM	EEPROM	I/O	Chip Select	Slow Mode	Packages
MC68HC(L)11K0 MC68HC(L)11K1 MC68HC(L)11K4	0 0 24 K	768 768 768	0 640 640	37 37 62	Yes Yes Yes	No No No	84-pin PLCC(1) 80-pin QFP(2)
MC68HC711K4	24 K	768	640	62	Yes	No	84-pin J-cerquad(3) 84-pin PLCC 80-pin QFP
MC68HC11KS2	32 K	1 K	640	51	No	Yes	68-pin PLCC 80-pin LQFP(4)
MC68HC711KS2	32 K	1 K	640	51	No	Yes	68-pin PLCC 80-pin LQFP 68-pin J-cerquad

1. PLCC = Plastic leaded chip carrier
2. QFP = Quad flat pack
3. J-cerquad = Ceramic windowed version of PLCC
4. LQFP = Low-profile quad flat pack