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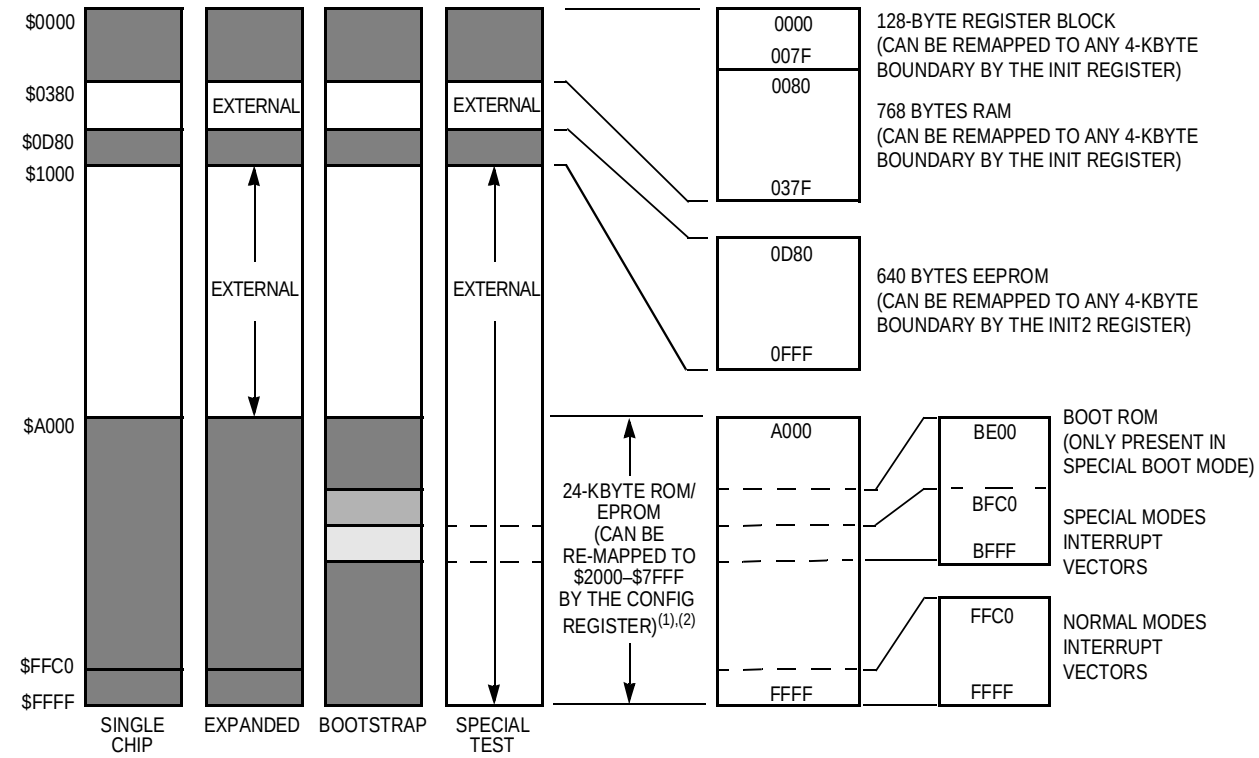
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	4MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	62
Program Memory Size	24KB (24K x 8)
Program Memory Type	OTP
EEPROM Size	640 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc711k4vfue4



Note 1.EPROM can be enabled in special test mode by setting the ROMON bit in the CONFIG register after reset.

Figure 4-3. M68HC11K4 Family Memory Map

Table 4-6. Register Mapping

REG[3:0]	Address
0000	$0000–$007F(1)
0001	$1000–$107F
0010	$2000–$207F
0011	$3000–$307F
0100	$4000–$407F
0101	$5000–$507F
0110	$6000–$607F
0111	$7000–$707F
1000	$8000–$807F
1001	$9000–$907F
1010	$A000–$A07F
1011	$B000–$B07F
1100	$C000–$C07F
1101	$D000–$D07F
1110	$E000–$E07F
1111	$F000–$F07F

1. Default locations out of reset.

Since the direct addressing mode accesses RAM more quickly and efficiently than other addressing modes, many applications will find the default locations of registers and on-board RAM at the bottom of memory to be the most advantageous.

When RAM and the registers are both mapped to different 4-K boundaries, the registers are mapped at $x000–$x07F, and RAM is moved to $x000–$x2FF ($x000–x3FF for the [7]11KS2).

registers to default values, then receives data from an external host and programs it into the EPROM. The value in the X index register determines programming delay time. The value in the Y index register is a pointer to the first address in EPROM to be programmed. The default starting address is $8000 for the M68HC11KS2.

When the utility program is ready to receive programming data, it sends the host a $FF character and waits for a reply. When the host sees the $FF character, it sends the EPROM programming data, starting with the first location in the EPROM array. After the MCU receives the last byte to be programmed and returns the corresponding verification data, it terminates the programming operation by initiating a reset. Refer to the Motorola application note entitled *MC68HC11 Bootstrap Mode,* document order number AN1060/D.

4.7.2 Programming the EPROM from Memory

In this method, software programs the EPROM one byte at a time. Each byte is read from memory, then latched and programmed into the EPROM using the EPROM programming control register (EPROG). This procedure can be done in any operating mode.

Address: $002B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	R	0	ELAT	EXCOL	EXROW	0	0	EPGM
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 4-8. EPROM Programming Control Register (EPROG)

MBE — Multiple-Byte Program Enable Bit

MBE is for factory use only and is accessible only in special test mode. When MBE is set, the MCU ignores address bit 5, so that bytes with ADDR5 = 0 and ADDR5 = 1 both get programmed with the same data.

0 = Normal programming
1 = Multiple-byte programming enabled

ELAT — EPROM Latch Control Bit

Setting ELAT latches the address and data of writes to the EPROM. The EPROM cannot be read. ELAT can be read at any time. ELAT can be written any time except when PGM = 1, which disables writes to ELAT.

0 = EPROM address and data bus configured for normal reads. EPROM cannot be programmed.

1 = EPROM address and data bus are configured for programming. Address and data of writes to EPROM are latched. EPROM cannot be read.

EXCOL — Select Extra Columns Bit

EXCOL is for factory use only and is accessible only in special test mode. When EXCOL equals 1, extra columns can be accessed at bit 7 and bit 0. Addresses use bits [11:5]. Bits [4:1] are ignored.

0 = User array selected

1 = Extra columns selected and user array disabled

EXROW — Select Extra Rows Bit

EXROW is for factory use only and is only accessible in special test mode. When EXROW equals 1, two extra rows are available. Addresses use bits [5:0]. Bits [11:6] are ignored.

0 = User array selected

1 = Extra rows selected and user array is disabled

EPGM — EPROM Programming Enable Bit

EPGM applies programming voltage (V_{PP}) to the EPROM. EPGM can be read at any time. EPGM can be written only when ELAT = 1.

0 = Programming voltage to EPROM array is disconnected

1 = Programming voltage to EPROM array is connected; ELAT cannot be changed.

4.9.2 System Configuration Options 2 Register

Address: $0038

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	LIRDV	CWOM	STRCH(1)	IRVNE	LSBF	SPR2	XDV1	XDV0
Reset:	0	0	0	—	0	0	0	0

1. Not available on M68HC11K devices

Figure 4-15. System Configuration Options 2 Register (OPT2)

XDV[1:0] — XOUT Clock Divide Select Bits

These two bits select the divisor for the XOUT clock frequency, as shown in **Table 4-10**. The divisor is set to 1 out of reset (XOUT = XTAL). It takes a maximum of 16 cycles after writing these bits for XOUT to stabilize. The phase relationship between XOUT and XTAL cannot be predicted.

Table 4-10. XOUT Frequencies

XDV[1:0]		EXTAL Divided By	Frequency at EXTAL = 8 MHz	Frequency at EXTAL = 12 MHz	Frequency at EXTAL = 16 MHz	Frequency at EXTAL = 16 MHz
0	0	1	8 MHz	12 MHz	16 MHz	20 MHz
0	1	4	2 MHz	3 MHz	4 MHz	5 MHz
1	0	6	1.33 MHz	2 MHz	2.67 MHz	3.33 MHz
1	1	8	1 MHz	1.5 MHz	2 MHz	2.5 MHz

7.5 Receive Operation

During receive operations, data from the TxD pin is shifted into the serial shift register. A completed word is parallel-loaded to a receive data register (RDR), which can be read through SCDRH/L. This double-buffered operation allows reception of the current character while the MCU reads the previous character.

The SCI receiver has seven status flags, summarized in Table 7-1.

Table 7-1. SCI Receiver Flags

Flag	Name	Set When	Interrupt Enable Bit
RDRF	Receive data register full	Character transferred from shift register to RDR	RIE
IDLE	Idle-line detected	Active transmit line goes idle	ILIE
OR	Overrun error	Character ready for RDR while previous character unread	RIE
NF	Noise error	Samples of data bit not unanimous	—
FE	Frame error	0 detected where stop bit expected	—
PF	Parity error	Calculated parity does not match data parity bit	—
RAF	Receiver active	A character is being received	—

Three of the flags can generate interrupt requests if the corresponding enable bits in SCCR2 are set. The status flags are set by the SCI logic in response to specific conditions in the receiver. These flags can be read (polled) at any time by software. Each bit except RAF is cleared by reading SCSR1 and SCDR sequentially.

- The receive data register full (RDRF) flag is set when the last bit of a character is received and data is transferred from the shift register to the RDR.
- The IDLE flag is set after a transition on the RxD line from an active state to an idle state. This prevents repeated interrupts during the time RxD remains idle.

FE — Framing Error Flag

FE is set when a 0 is detected where a stop bit (logic 1) was expected.

0 = Stop bit detected

1 = Logic 0 detected at the end of a character

PF — Parity Error Flag

PF is set if received data has incorrect parity. Clear PF by reading SCSR1.

0 = Parity disabled

1 = Parity enabled

7.9.5 Serial Communication Status Register 2

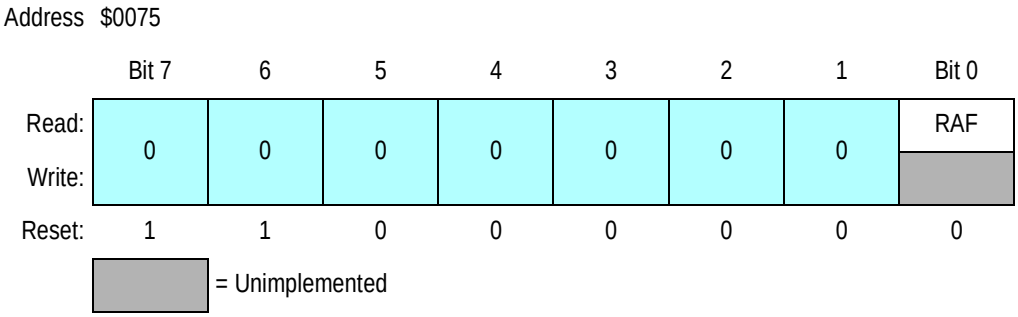


Figure 7-10. SCI Status Register 2 (SCSR2)

RAF — Receiver Active Flag

RAF is a read-only bit.

0 = Receiver is inactive.

1 = A character is being received.

A single MCU register, the serial peripheral data register (SPDR) is used both to read input data from the read buffer and to write output data to the transmit shift register.

Figure 8-1 shows the SPI block diagram.

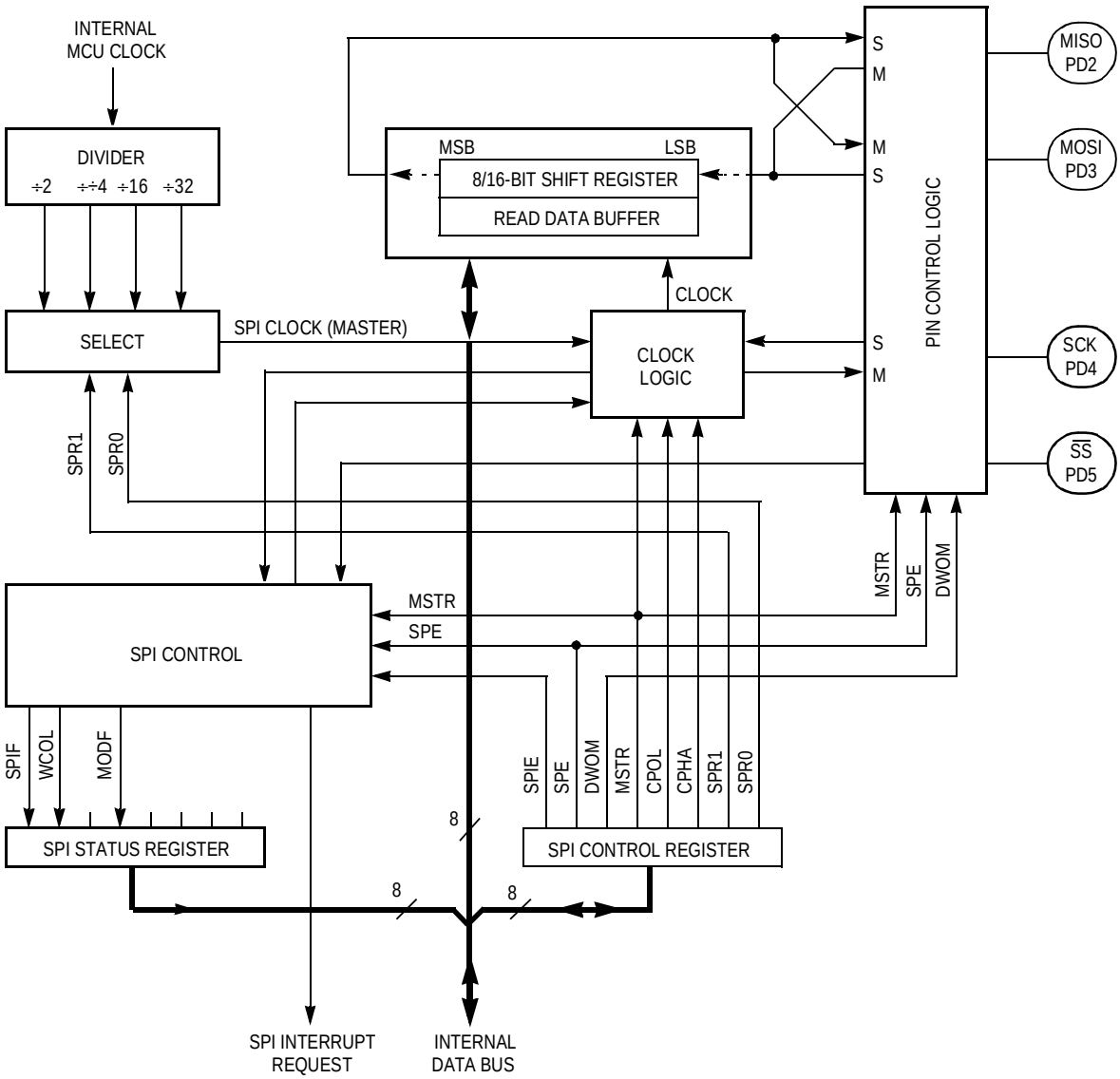


Figure 8-1. SPI Block Diagram

8.4.4 Slave Select ($\overline{SS}$)

The slave select ($\overline{SS}$) input is used to target specific devices in the SPI system. It must be pulled low on a targeted slave device prior to any communication with a master and must remain low for the duration of the transaction. $\overline{SS}$ must always be high on any device in master mode. Pulling $\overline{SS}$ low on a master mode device generates a mode fault error (see **8.5.1 Mode Fault Error**).

8.4.5 SPI Timing

Four possible timing relationships are available through control bits CPOL (clock polarity) and CPHA (clock phase) in the SPCR. These bits must be the same in both master and slave devices. The master device always places data on the MOSI line approximately a half-cycle before the SCK clock edge. This enables the slave device to latch the data. See **Figure 8-2**.

A write collision is normally a slave error because a slave has no control over when a master initiates a transfer. A master knows when a transfer is in progress, so there is no reason for a master to generate a write-collision error, although the SPI logic can detect write collisions in both master and slave devices.

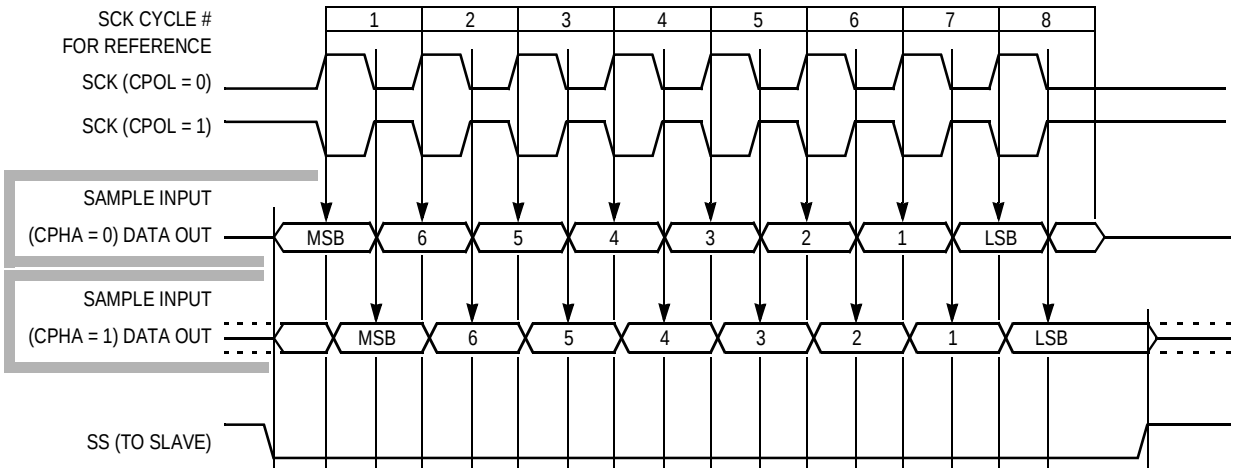


Figure 8-2. Data Clock Timing Diagram

9.2 Introduction

M68HC11 microcontrollers contain an extensive timing system to support a wide variety of timer-related functions. This section discusses the nature of the timing system and presents details of timer-related functions including:

- Input capture/output compare (IC/OC)
- Real-time interrupt (RTI)
- Pulse accumulator (PA)
- Pulse width modulation (PWM)

9.3 Timer Structure

As Figure 9-1 shows, the primary system clocks, including the E clock and the internal PH2 bus clock, are derived from the oscillator output divided by four.

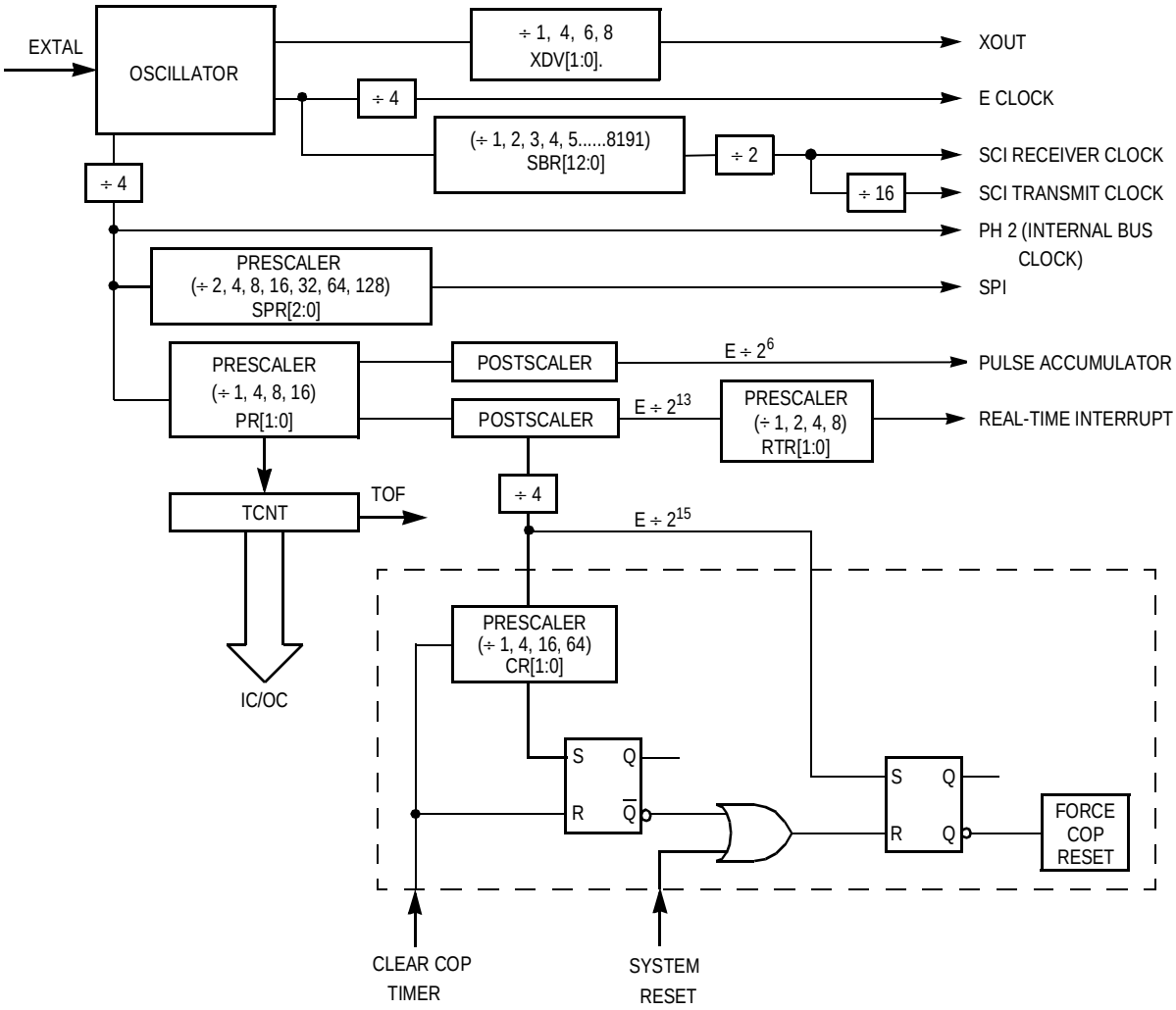


Figure 9-1. Timer Clock Divider Chains

- After a match occurs, change the appropriate OC1D bit to the opposite polarity, then add a value representing the width of the pulse to the original value and write it to the output compare register.

Because the pin state changes occur at specific values of the free-running counter, the pulse width can be controlled accurately to the resolution of the free-running counter, independent of software latencies. To generate an output signal of a specific frequency and duty cycle, repeat this pulse-generating procedure.

9.6.1 Timer Output Compare Registers

	Bit 7	6	5	4	3	2	1	Bit 0
Address:	$0016 — TOC1 (High)							
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1
Address:	$0017 — TOC1 (Low)							
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1
Address:	$0018 — TOC2 (High)							
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1
Address:	$0019 — TOC2 (Low)							
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1

Figure 9-13. Timer Output Compare Registers (TOC1–TOC4)

9.7.5 Pulse Accumulator Count Register

Address: $0027

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	0	0	0	0	0	0	0	0

Figure 9-26. Pulse Accumulator Count Register (PACNT)

In event counting mode, PACNT contains the count of external input events at the PAI input. In gated accumulation mode, PACNT is incremented by the pulse accumulator's E ÷ 64 clock when the PAI input is at the selected level. Counting is synchronized to the internal PH2 clock so that incrementing and reading occur during opposite half cycles. The counter is not affected by reset and can be read or written to at any time.

9.8 Real-Time Interrupt (RTI)

The real-time interrupt (RTI) feature generates hardware interrupts at a fixed periodic rate. The rate is determined by bits RTR[1:0] in the PACTL register, which further divide a clock running at E ÷ 2^{13} by 1, 2, 4 or 8. The resulting periods for various common crystal frequencies are shown in **Table 9-7**.

Every cycle of the RTI clock sets the RTIF bit in timer interrupt flag 2 (TFLG2) register. This flag can be polled to determine when RTI timeouts occur, or an interrupt can be generated if the RTII bit in the timer interrupt mask 2 (TMSK2) register is set. After reset, one entire real-time interrupt period elapses before the RTIF flag is set for the first time.

The clock source for the RTI function is a free-running clock that cannot be stopped or interrupted except by reset. The time between successive RTI timeouts is a constant that is independent of software latencies

associated with flag clearing and service. For this reason, an RTI period starts from the previous timeout, not from when RTIF is cleared.

9.8.1 Timer Interrupt Flag 2 Register

Address: $0025

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TOF	RTIF	PAOVF	PAIF	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

Figure 9-27. Timer Interrupt Flag 2 Register (TFLG2)

Clear each flag by writing a 1 to the corresponding bit position.

RTIF — Real-Time Interrupt Flag

The RTIF status bit is automatically set to 1 at the end of every RTI period.

9.8.2 Timer Interrupt Mask 2 Register

Address: $0024

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
Reset:	0	0	0	0	0	0	0	0

Figure 9-28. Timer Interrupt Mask 2 Register (TMSK2)

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2.

RTII — Real-time Interrupt Enable Bit

0 = RTIF interrupts disabled
1 = Interrupt requested when RTIF is set to 1

CON34 — Concatenate Channels 3 and 4 Bit

Channel 3 is the high-order byte, and channel 4 (port H, bit 3) is output.

0 = Channels 3 and 4 are separate 8-bit PWMs.
1 = Channels 3 and 4 are concatenated to create one 16-bit PWM.

CON12 — Concatenate Channels 1 and 2 Bit

Channel 1 is the high-order byte, and channel 2 (port H, bit 1) is output.

0 = Channels 1 and 2 are separate 8-bit PWMs.
1 = Channels 1 and 2 are concatenated to create one 16-bit PWM.

PCKA[2:1] — Prescaler for Clock A Bits

These bits select the frequency for clock A as shown in **Table 9-8**.

Table 9-8. Clock A Prescaler

PCKA[2:1]	Clock A Frequency
0 0	E
0 1	E/2
1 0	E/4
1 1	E/8

PCKB[3:1] — Prescaler for Clock B Bits

These bits select the frequency for clock B as shown in **Table 9-9**.

Table 9-9. Clock B Prescaler

PCKB[3:1]	Clock B Frequency
0 0 0	E
0 0 1	E/2
0 1 0	E/4
0 1 1	E/8
1 0 0	E/16
1 0 1	E/32
1 1 0	E/64
1 1 1	E/128

9.9.2.4 Pulse-Width Modulation Timer Enable Register

Address: $0063

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TPWSL	DISCP	0	0	PWEN4	PWEN3	PWEN2	PWEN1
Reset:	0	0	0	0	0	0	0	0

Figure 9-34. Pulse-Width Modulation Timer Enable Register (PWEN)

TPWSL — PWM Scaled Clock Test Bit — factory use only; only accessible in special test mode

0 = Normal operation

1 = Clock S is output to PWSCAL register (test only)

DISCP — Disable Compare Scaled E-Clock Bit — factory use only; only accessible in special test mode

0 = Normal operation

1 = Match of period does not reset associated count register (test only)

PWEN[4:1] — Pulse-Width Enable for Channels [4:1] Bits

0 = Channel disabled

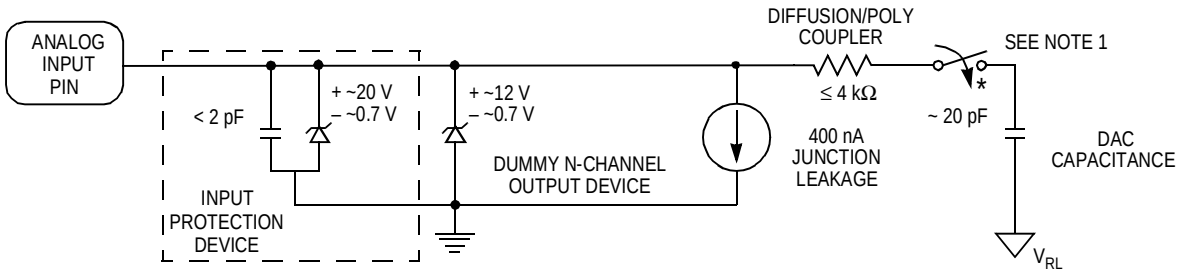
1 = Channel enabled at port H bits [3:0]

10.5 Design Considerations

This section discusses design considerations.

10.5.1 A/D Input Pins

Port E pins can also be used as general-purpose digital inputs. Digital reads of port E pins are not recommended during the sample portion of an A/D conversion cycle, when the gate signal to the N-channel input is on. No P-channel devices are directly connected to either input pins or reference voltage pins, so voltages above V_{DD} do not cause a latchup problem, although current should be limited according to maximum ratings. Refer to **Figure 10-6**.



Note 1. This analog switch is closed only during the 12-cycle sample time.

Figure 10-6. Electrical Model of an A/D Input Pin (Sample Mode)

10.5.2 Operation in Stop and Wait Modes

If a conversion sequence is in progress when either the stop or wait mode is entered, the conversion of the current channel is suspended. When the MCU resumes normal operation, that channel is resampled and the conversion sequence is resumed. As the MCU exits the wait mode, the A/D circuits are stable and valid results can be obtained on the first conversion. However, in stop mode, all analog bias currents are disabled and it is necessary to allow a stabilization period when leaving stop mode. If stop mode is exited with a delay (DLY = 1), there is enough time for these circuits to stabilize before the first conversion. If stop mode is exited with no delay (DLY bit in OPTION register = 0), allow 10 ms for the A/D circuitry to stabilize to avoid invalid results.

11.4.4.1 General-Purpose Chip Select 1 Control Register

Address: $005D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	G1DG2	G1DPC	G1POL	G1AV	G1SZA	G1SZB	G1SCC	G1SZD
Reset:	0	0	0	0	0	0	0	0

Figure 11-12. General-Purpose Chip Select 1 Control Register (GPCS1C)

G1DG2 — GPCS 1 Drives GPCS 2 Bit
0 = CSGP1 does not affect CSGP2.
1 = CSGP1 and CSGP2 are ORed and driven out of the CSGP2.

G1DPC — General-Purpose Chip Select 1 Drives Program Chip Select Bit
0 = CSGP1 does not affect CSPROG.
1 = CSGP1 and CSPROG are ORed and driven out of the CSPROG.

11.4.4.2 General-Purpose Chip Select 2 Control Register

Address: $005F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	G2DPC	G2POL	G2AV	G2SZA	G2SZB	G2SZC	G2SZD
Reset:	0	0	0	0	0	0	0	0

Figure 11-13. General-Purpose Chip Select 2 Control Register (GPCS2C)

G2DPC — General-Purpose Chip Select 2 Drives Program Chip Select Bit
0 = Does not affect program chip select
1 = CSGP2 and CSPROG are ORed and driven out of the CSPROG pin.

Development Support

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