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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	4MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	62
Program Memory Size	24KB (24K x 8)
Program Memory Type	OTP
EEPROM Size	640 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc711k4vfue4r

Section 3. Central Processor Unit (CPU)

List of Figures

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- Enhanced synchronous serial peripheral interface (SPI)
- 8-channel, 8-bit, analog-to-digital (A/D) converter
- Computer operating properly (COP) watchdog system to guard against infinite loops and other system problems
- Real-time interrupt timer
- Power-saving modes:
  - Slow mode reduces power consumption by slowing down internal operations.
  - Wait mode shuts down various system features selected by the user with power consumption typically dropping to 10–100 mW.
  - Stop mode also shuts down system clocks, typically reducing power consumption to about 1.5 mW.
- Package availability for ROM devices:
  - K versions:
    84-pin plastic leaded chip carrier (PLCC)
    80-pin quad flat pack (QFP)
  - KS versions:
    68-pin plastic leaded chip carrier (PLCC)
    80-pin low-profile quad flat pack (LQFP)
- Package availability for EPROM devices:
  - K versions:
    80-pin quad flat pack (QFP)
    84-pin J-cerquad (ceramic windowed version of PLCC)
    84-pin plastic leaded chip carrier (PLCC)
  - KS versions:
    68-pin J-cerquad (ceramic windowed version of PLCC)
    80-pin low-profile quad flat pack (LQFP)
    68-pin plastic leaded chip carrier (PLCC)

Section 3. Central Processor Unit (CPU)

3.1 Contents

3.2 Introduction

This section presents information on M68HC11 central processor unit (CPU) architecture, data types, addressing modes, the instruction set, and special operations, such as subroutine calls and interrupts.

The CPU employs memory-mapped input/output (I/O). There are no special instructions for I/O; all peripheral, I/O, and memory locations are simply addresses in the 64-Kbyte memory map. This architecture also enables access to operands from external memory locations with no execution time penalty.

3.3 CPU Registers

M68HC11 CPU registers are an integral part of the CPU and are not addressed as memory locations. The seven registers are shown in **Figure 3-1**.

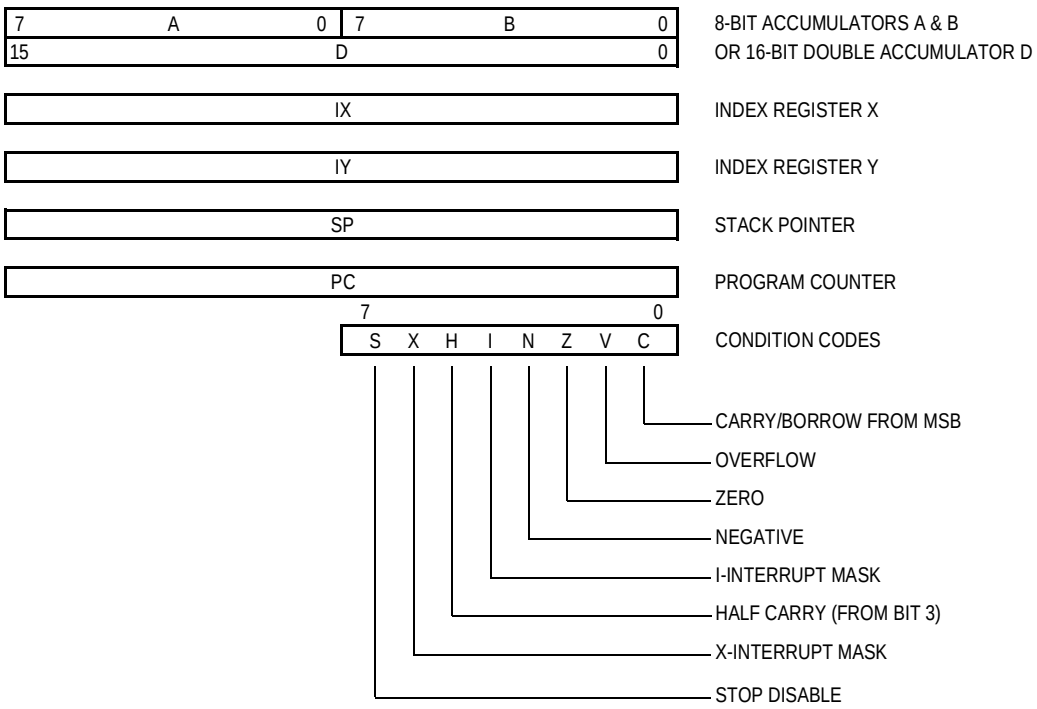


Figure 3-1. Programming Model

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0015	Timer Input Capture 3 Register Low (TIC3L) See page 192.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	Undefined after reset							
$0016	Timer Output Compare 1 High Register (TOC1H) See page 197.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	1	1	1	1	1	1	1	1
$0017	Timer Output Compare 1 Low Register (TOC1L) See page 197.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	1	1	1	1	1	1	1	1
$0018	Timer Output Compare 2 High Register (TOC2H) See page 197.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	1	1	1	1	1	1	1	1
$0019	Timer Output Compare 2 Low Register (TOC2L) See page 197.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	1	1	1	1	1	1	1	1
$001A	Timer Output Compare 3 High Register (TOC3H) See page 197.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	1	1	1	1	1	1	1	1
$001B	Timer Output Compare 3 Low Register (TOC3L) See page 197.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	1	1	1	1	1	1	1	1
$001C	Timer Output Compare 4 High Register (TOC4H) See page 197.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	1	1	1	1	1	1	1	1
$001D	Timer Output Compare 4 Low Register (TOC4L) See page 197.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	1	1	1	1	1	1	1	1

= Unimplemented R = Reserved U = Undefined

Figure 4-1. Register and Control Bit Assignments (Sheet 3 of 11)

4.6.4 Bootloader ROM

The bootloader program occupies 512 bytes of bootstrap ROM at addresses $BE00–$BFFF. It is active only in special modes when the RBOOT bit in the HPRIO register is set.

4.7 EPROM/OTPROM (M68HC711K4 and M68HC711KS2)

The M68HC711K4 devices include 24 Kbytes of on-chip EPROM (OTPROM in non-windowed packages). The M68HC711KS2 has 32 Kbytes of EPROM.

The two methods available to program the EPROM are:

- Downloading data through the serial communication interface (SCI) in bootstrap or special test mode
- Programming individual bytes from memory

Before proceeding with programming:

- Ensure that the CONFIG register ROMON bit is set.
- Ensure that the $\overline{\text{IRQ}}$ pin is pulled to a high level.
- Apply 12 volts to the $\overline{\text{XIRQ}}/V_{PP}$ pin.

Program the EPROM only at room temperature. Place an opaque label over the quartz window on windowed parts after programming.

4.7.1 Programming the EPROM with Downloaded Data

The MCU can download EPROM data through the SCI while in the special test or bootstrap modes. This can be done either with custom software, also downloaded through the SCI, or with a built-in utility program in bootstrap ROM. In either case, the 12-volt nominal programming voltage must be present on the $\overline{\text{XIRQ}}/V_{PP}$ pin.

To use the bootstrap ROM utility, download a 3-byte program consisting of a single jump instruction to $BF00, the starting address of the resident EPROM programming utility. The utility program sets the X and Y index

  - The RDRF, IDLE, OR, NF, FE, PF, and RAF receive-related status bits are cleared.

- Serial peripheral interface (SPI)
  - The SPI system is disabled by reset.
  - The port pins associated with this function default to being general-purpose I/O lines.
- Analog-to-digital (A/D) converter
  - The ADPU bit in the OPTION register is cleared, disabling the A/D system.
  - The conversion complete flag in the ADCTL register is also cleared.
- System
  - The external $\overline{\text{IRQ}}$ pin has the highest I-bit interrupt priority because PSEL[4:0] in the HPRIO register are initialized with the value %00110 (where % indicates a binary value).
  - The RBOOT, SMOD, and MDA bits in the HPRIO register reflect the status of the MODB and MODA inputs at the rising edge of reset.
  - The $\overline{\text{IRQ}}$ pin is configured for level-sensitive operation for wired-OR systems.
  - The DLY control bit in the OPTION register is set, enabling oscillator startup delay after recovery from stop mode.
  - The clock monitor system is disabled because the CME and FCME bits in the OPTION register are cleared.

5.5 Interrupts

The MCU has 18 interrupt vectors that support 22 interrupt sources. The 19 maskable interrupts are generated by on-chip peripheral systems. They are recognized when the I bit in the CCR is clear. The three non-maskable interrupt sources are illegal opcode trap, software interrupt, and $\overline{\text{XIRQ}}$ pin. **Table 5-5** lists the interrupt sources and vector assignments for each source.

A single MCU register, the serial peripheral data register (SPDR) is used both to read input data from the read buffer and to write output data to the transmit shift register.

Figure 8-1 shows the SPI block diagram.

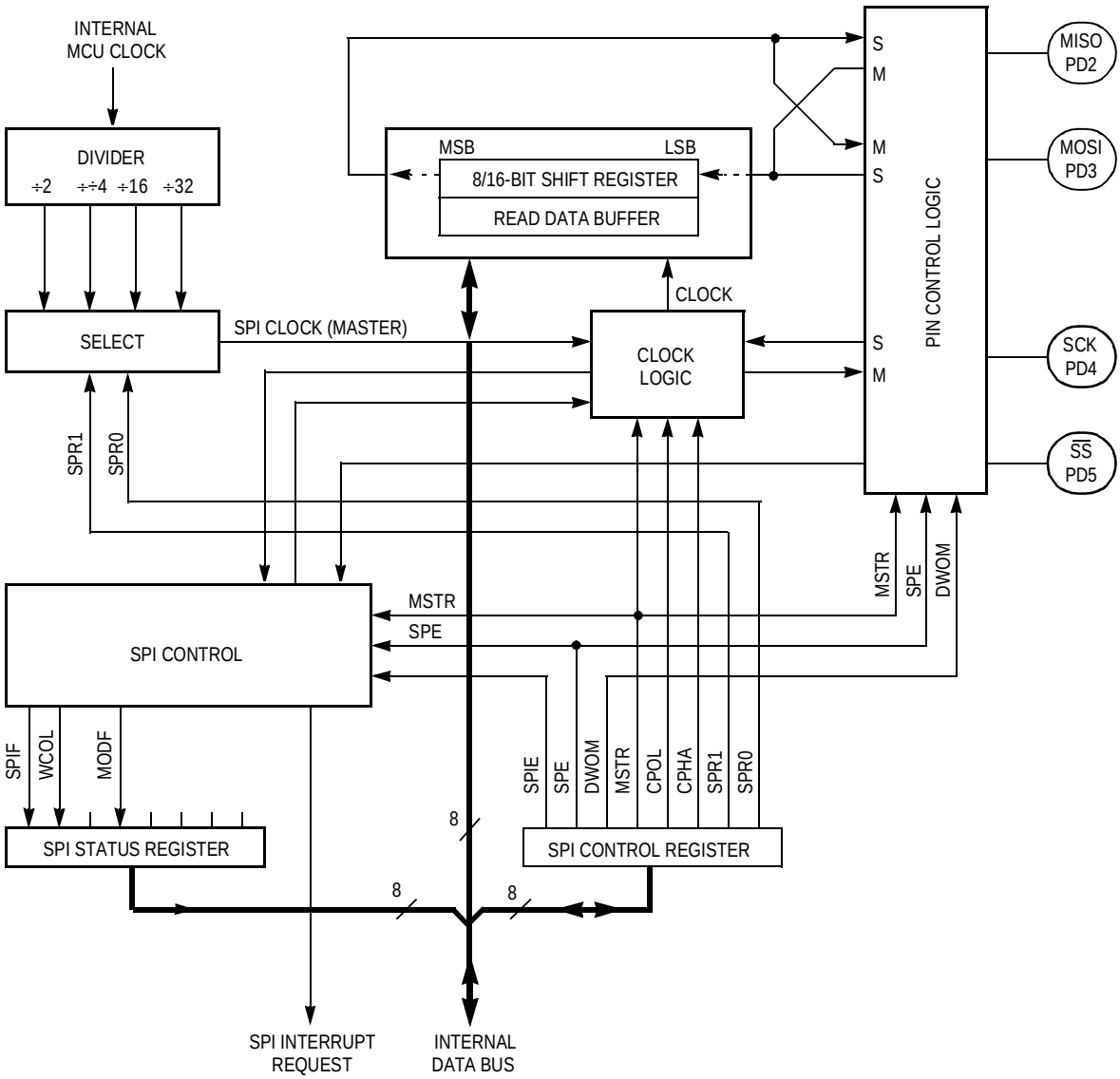


Figure 8-1. SPI Block Diagram

8.4.4 Slave Select ($\overline{SS}$)

The slave select ($\overline{SS}$) input is used to target specific devices in the SPI system. It must be pulled low on a targeted slave device prior to any communication with a master and must remain low for the duration of the transaction. $\overline{SS}$ must always be high on any device in master mode. Pulling $\overline{SS}$ low on a master mode device generates a mode fault error (see **8.5.1 Mode Fault Error**).

8.4.5 SPI Timing

Four possible timing relationships are available through control bits CPOL (clock polarity) and CPHA (clock phase) in the SPCR. These bits must be the same in both master and slave devices. The master device always places data on the MOSI line approximately a half-cycle before the SCK clock edge. This enables the slave device to latch the data. See **Figure 8-2**.

A write collision is normally a slave error because a slave has no control over when a master initiates a transfer. A master knows when a transfer is in progress, so there is no reason for a master to generate a write-collision error, although the SPI logic can detect write collisions in both master and slave devices.

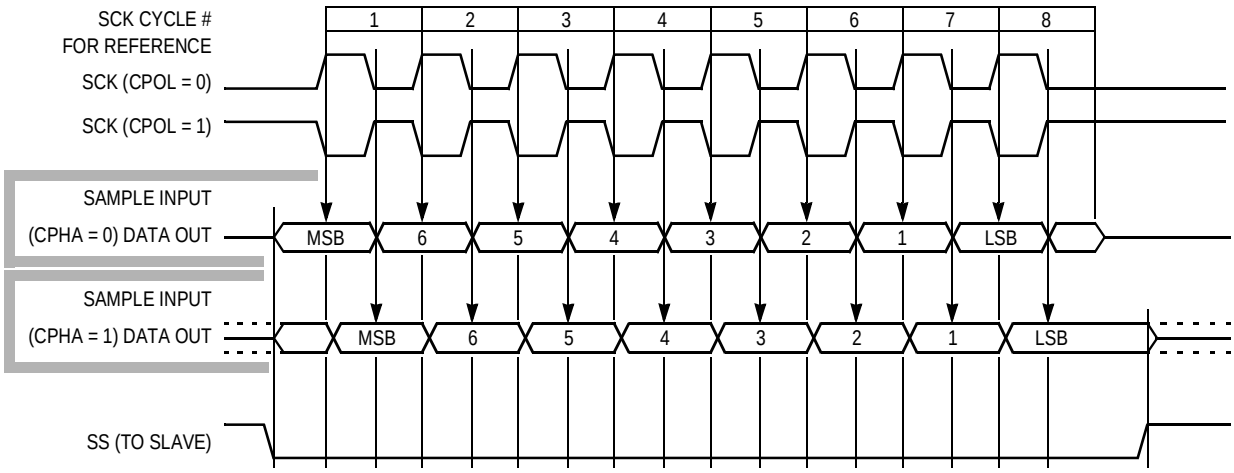


Figure 8-2. Data Clock Timing Diagram

The PH2 bus clock feeds four primary divider chains. The functions supplied by each of these chains are:

1. Serial peripheral interface (SPI)
2. Input capture/output compare (IC/OC)
3. Pulse accumulator (PA)
4. RTI and COP watchdog circuit

The SPI prescale factor is determined by bits SPR[2] in the system configuration options 2 (OPT2) register and SPR[1:0] in the serial peripheral control register (SPCR). See **8.6.1 Serial Peripheral Control Register** and **8.6.5 System Configuration Options 2**.

The input capture and output compare functions are based on a 16-bit free-running counter, which is driven by the PH2 clock divided by a programmable prescaler. Bits PR[1:0] of the timer interrupt mask 2 (TMSK2) register enable the user to select one of four divisors: 1, 4, 8, or 16. The output of this prescaler, referred to as the main timer, feeds the divider chains for the pulse accumulator, RTI, and COP circuits as well as the free-running counter. **Table 9-1** shows main timer frequencies and periods available from the most common crystal inputs.

Table 9-1. Main Timer Rates

EXTAL Frequencies						
EXTAL Freq.	**8.0 MHz**	**12.0 MHz**	**16.0 MHz**	**20.0 MHz**	**20.0 MHz**	**Other EXTAL**
E Clock Freq.	**2.0 MHz**	**3.0 MHz**	**4.0 MHz**	**5.0 MHz**	**5.0 MHz**	**EXTAL/4**
E Clock Period	**500 ns**	**333 ns**	**250 ns**	**200 ns**	**200 ns**	**1/E**
Control Bits PR[1:0]	**Main Timer Period (1 Count/Timer Overflow)**					**1 Count Timer Overflow**
0 0	500 ns 32.768 ms	333 ns 21.845 ms	250 ns 16.384 ms	200 ns 13.107 ms	167 ns 10.923 ms	1 ÷ E 2^{16} ÷ E
0 1	2.0 µs 131.07 ms	1.3 µs 87.381 ms	1.0 µs 85.536 ms	800 ns 52.429 ms	667 ns 43.961 ms	4 ÷ E 2^{18} ÷ E
1 0	4.0 µs 262.14 ms	2.667 µs 174.76 ms	2.0 µs 131.07 ms	1.6 µs 104.86 ms	1.333 µs 87.381 ms	8 ÷ E 2^{19} ÷ E
1 1	8.0 µs 524.29 ms	5.333 µs 349.53 ms	4.0 µs 262.14 ms	3.2 µs 209.72 ms	2.667 µs 174.76 ms	16 ÷ E 2^{20} ÷ E

- After a match occurs, change the appropriate OC1D bit to the opposite polarity, then add a value representing the width of the pulse to the original value and write it to the output compare register.

Because the pin state changes occur at specific values of the free-running counter, the pulse width can be controlled accurately to the resolution of the free-running counter, independent of software latencies. To generate an output signal of a specific frequency and duty cycle, repeat this pulse-generating procedure.

9.6.1 Timer Output Compare Registers

	Bit 7	6	5	4	3	2	1	Bit 0
Address:	$0016 — TOC1 (High)							
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1
Address:	$0017 — TOC1 (Low)							
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1
Address:	$0018 — TOC2 (High)							
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1
Address:	$0019 — TOC2 (Low)							
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1

Figure 9-13. Timer Output Compare Registers (TOC1–TOC4)

9.7.1 Port A Data Direction Register

Address: $0001

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0
Reset:	0	0	0	0	0	0	0	0

Figure 9-22. Port A Data Direction Register (DDRA)

The pulse accumulator uses port A, bit 7 as the PAI input, but the pin can also be used as general-purpose I/O or as an output compare.

NOTE: *Even when port A, bit 7 is configured as an output, the pin still drives the input to the pulse accumulator.*

DDA7 — Data Direction Control for Port A, Bit 7
0 = PA7 configured as an input
1 = PA7 configured as an output

9.7.2 Pulse Accumulator Control Register

Address: $0026

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	PAEN	PAMOD	PEDGE	0	I4/O5	RTR1	RTR0
Reset:	0	0	0	0	0	0	0	0

Figure 9-23. Pulse Accumulator Control Register (PACTL)

PAEN — Pulse Accumulator System Enable Bit
0 = Pulse accumulator disabled
1 = Pulse accumulator enabled

window overlaps any portion of internal registers, RAM, or EEPROM, that portion is repeated in all banks associated with that window. If a window overlaps (EP)ROM, the (EP)ROM is present in all banks with XA[18:16] = 0:0:0.

The reset vector most commonly resides in on-chip (EP)ROM at address $FFFE–$FFFF. However, if the (EP)ROM is disabled or mapped at address $2000–$7FFF, the reset vector is fetched from external memory at $FFFE–$FFFF. When expanded memory is enabled, the reset vector is fetched from external memory at $7FFE–$7FFF, regardless of the presence of on-chip (EP)ROM.

11.3.2 Control Registers

Expansion address lines are enabled by the port G assignment register (PGAR). The size and position of memory windows are controlled by the memory mapping size (MMSIZ) and memory mapping window base (MMWBR) registers, respectively. The memory mapping window control registers, MM1CR and MM2CR, select the particular bank or page of expanded memory present in the window(s) at a given time.

NOTE: *Throughout this manual, the registers are discussed by function. In the event that not all bits in a register are referenced, the bits that are not discussed are shaded.*

11.3.2.1 Port G Assignment Register

The port G assignment register (PGAR) sets each of port G pins 5:0 as either an input/output (I/O) pin or memory expansion address line. Clearing a bit configures the corresponding port G pin as GPIO; setting the bit configures the pin as an expansion address line. If neither bank uses a particular expansion address bit, the corresponding pin is available for GPIO.

NOTE: *A special case exists for the address lines that overlap the CPU address lines XA[15:13]. If these lines are selected as expansion address lines in PGAR, but are not used in either window, the corresponding CPU address line is still output on the appropriate pin.*

Address: $002D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	—	—	PGAR5	PGAR4	PGAR3	PGAR2	PGAR1	PGAR0
Reset:	0	0	0	0	0	0	0	0

Figure 11-1. Port G Assignment Register (PGAR)

PGAR[5:0] — Port G Pin Assignment Bits

0 = Corresponding port G pin is GPIO.

1 = Corresponding port G pin is expansion address line XA[18:13].

11.3.2.2 Memory Mapping Size Register

The memory mapping size register (MMSIZ) sets the size of the windows in use.

Address: $0056

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	MXGS2	MXGS1	W2SZ1	W2SZ0	0	0	W1SZ1	W1SZ0
Reset:	0	0	0	0	0	0	0	0

Figure 11-2. Memory Mapping Size Register (MMSIZ)

W2SZ[1:0] — Window 2 Size Bit

W1SZ[1:0] — Window 1 Size Bit

These bits enable the memory windows and determine their size, as shown in **Table 11-2**.

Table 11-2. Window Size Select

WxSZ[1:0]	Window Size
00	Window disabled
01	8 K — Window can have up to 64 8-Kbyte banks
10	16 K — Window can have up to 32 16-Kbyte banks
11	32 K — Window can have up to 16 32-Kbyte banks

11.4.3.3 General-Purpose Chip Select 1 Control Register

Address: $005D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	G1DG2	G1DPC	G1POL	G1AV	G1SZA	G1SZB	G1SCC	G1SZD
Reset:	0	0	0	0	0	0	0	0

Figure 11-9. General-Purpose Chip Select 1 Control Register (GPCS1C)

G1POL — General-Purpose Chip Select 1 Polarity Select Bit

0 = CSGP1 active low

1 = CSGP1 active high

G1AV — General-Purpose Chip Select 1 Address Valid Select Bit

0 = CSGP1 is valid during E high time.

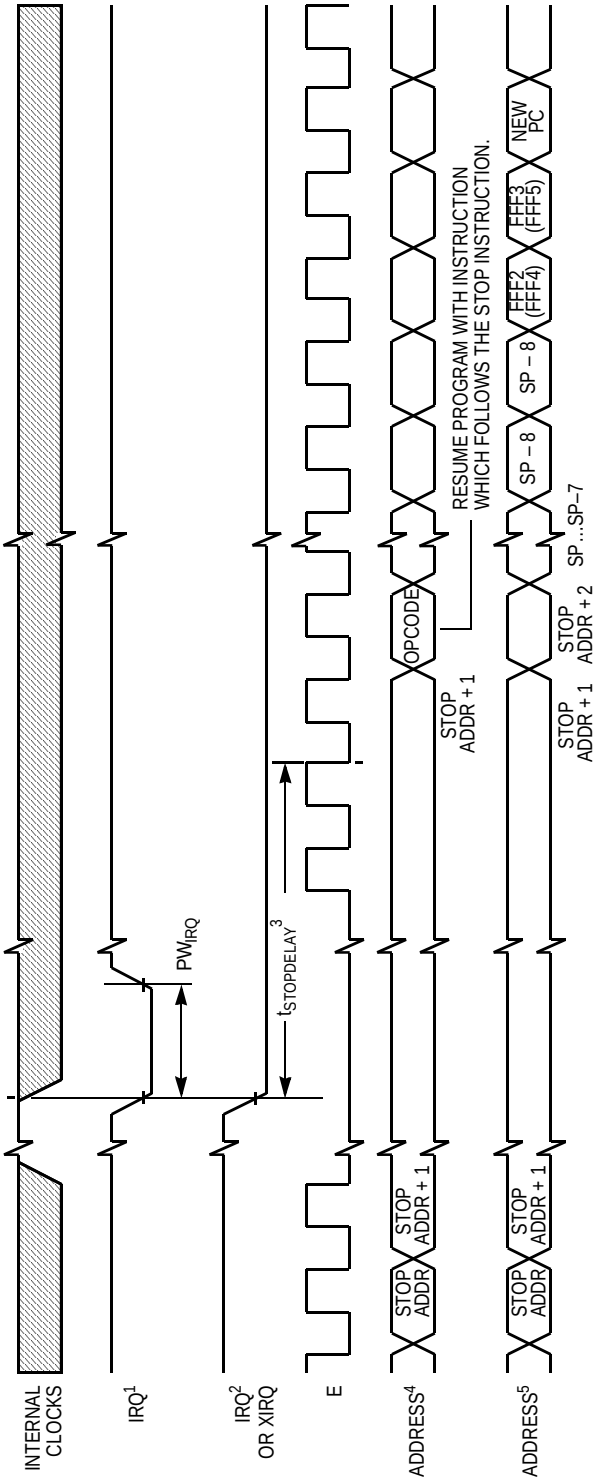
1 = CSGP1 is valid during address valid time.

G1SZ[A:D] — General-Purpose Chip Select 1 Size Bits

They select the range of GPCS1. Refer to **Table 11-6**.

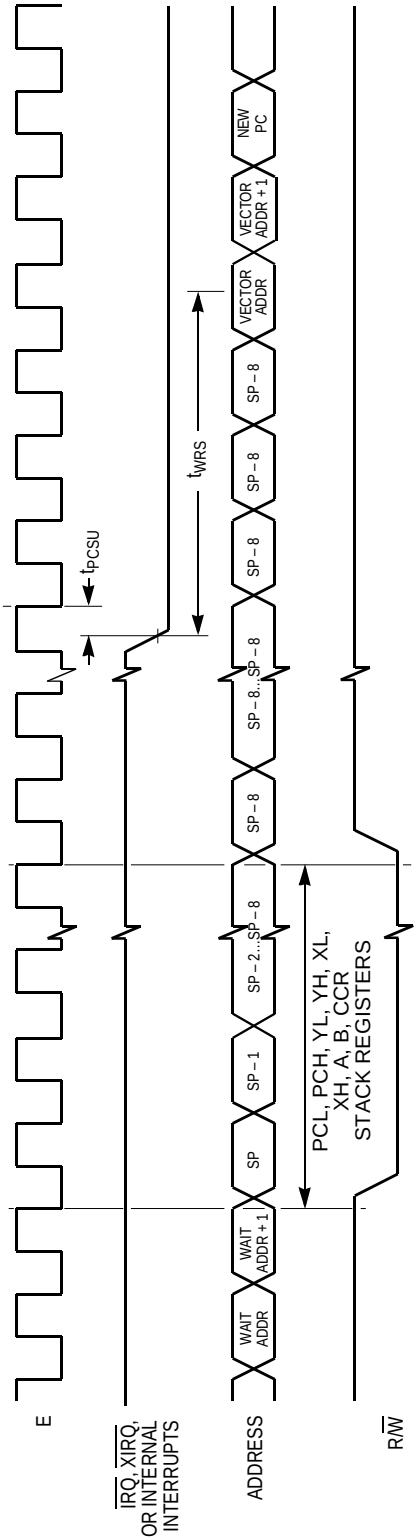
Table 11-6. General-Purpose Chip Select 1 Size Control

G1SZ[A:D]	Size (Bytes)	Valid Bits (MXGS1 = 0)	Valid Bits (MXGS1 = 1)
0 0 0 0	Disabled	None	None
0 0 0 1	2 K	G1A[15:11]	G1A[18:11]
0 0 1 0	4 K	G1A[15:11]	G1A[18:12]
0 0 1 1	8 K	G1A[15:13]	G1A[18:13]
0 1 0 0	16 K	G1A[15:14]	G1A[18:14]
0 1 0 1	32 K	G1A[15]	G1A[18:15]
0 1 1 0	64 K	None	G1A[18:16]
0 1 1 1	128 K	None	G1A[18:17]
1 0 0 0	256 K	None	G1A18
1 0 0 1	512 K	None	None
1 0 1 0	Follow window 1	None	None
1 0 1 1	Follow window 2	None	None
1100–1111	Default to 512 K	None	None



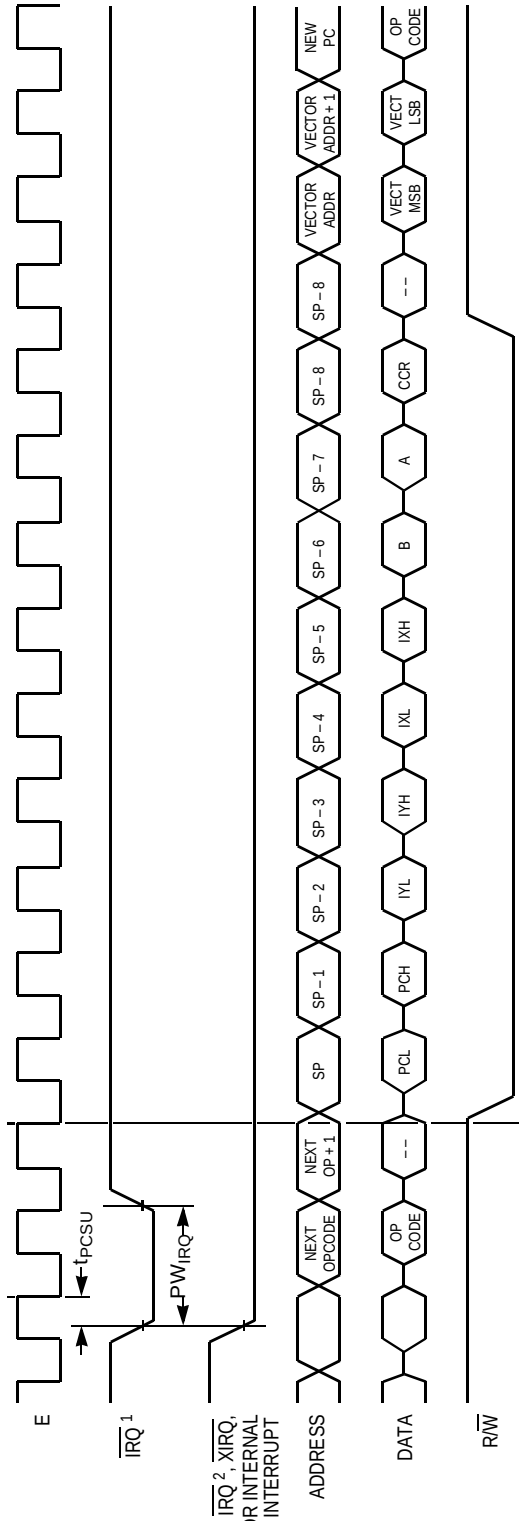
Notes:
1. Edge-sensitive $\overline{IRQ}$ pin (IRQE bit = 1)
2. Level-sensitive $\overline{IRQ}$ pin (IRQE bit = 0)
3. $t_{STOPDELAY}$ = 4064 t_{cyc} if DLY bit = 1 or 4 t_{cyc} if DLY = 0
4. $\overline{XIRQ}$ with X bit in CCR = 1
5. $\overline{IRQ}$ or $\overline{XIRQ}$ with X bit in CCR = 0

Figure 12-4. STOP Recovery Timing Diagram



Note: RESET also causes recovery from WAIT.

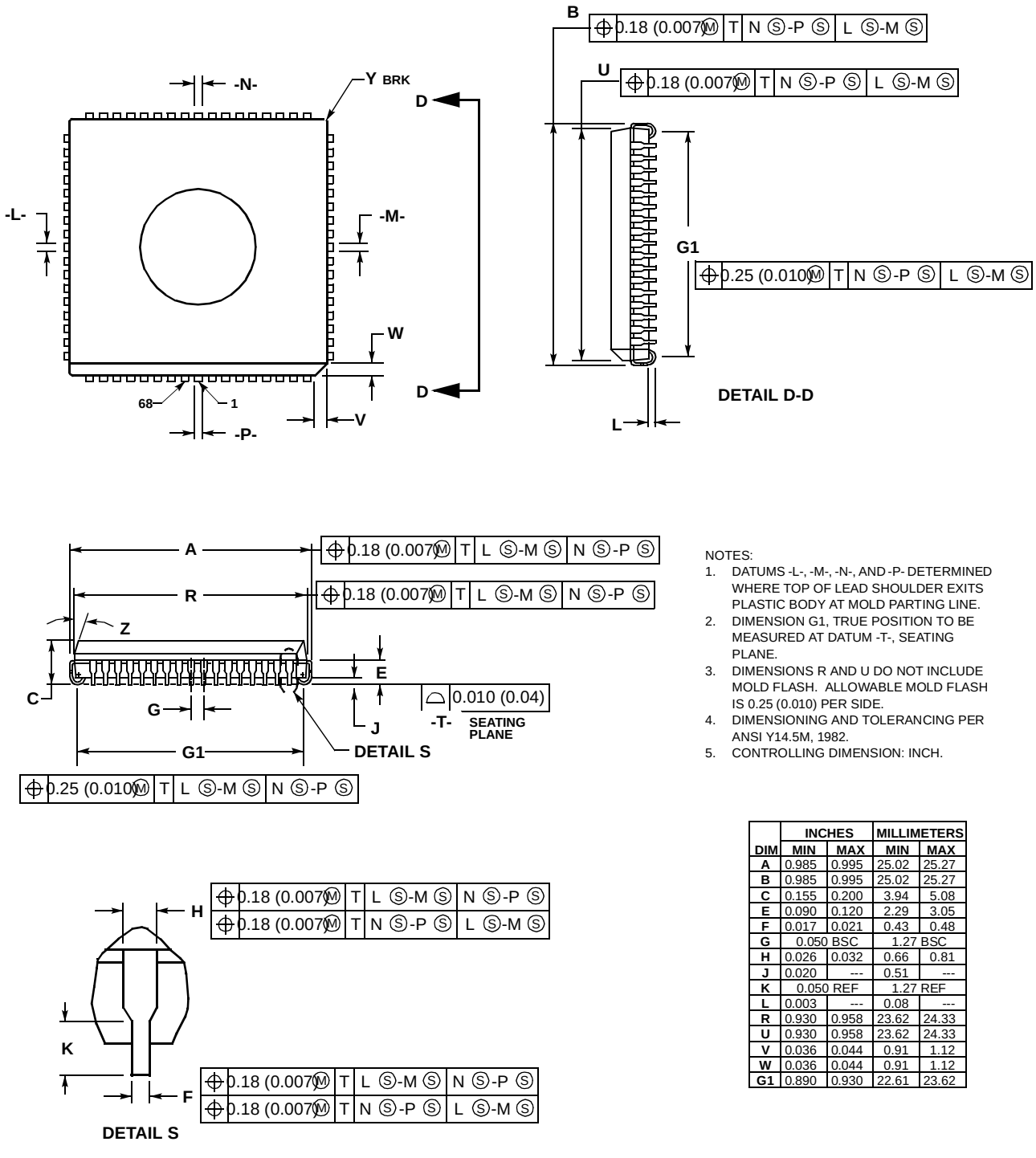
Figure 12-5. WAIT Recovery from Inerrupt Timing Diagram



Notes:
1. Edge-sensitive IRQ pin (IRQE bit = 1)
2. Level-sensitive IRQ pin (IRQE bit = 0)

Figure 12-6. Interrupt Timing Diagram

13.8 68-Pin J-Cerquad (Case 779A)



NOTES:
1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.985	0.995	25.02	25.27
B	0.985	0.995	25.02	25.27
C	0.155	0.200	3.94	5.08
E	0.090	0.120	2.29	3.05
F	0.017	0.021	0.43	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.050 REF		1.27 REF	
L	0.003	---	0.08	---
R	0.930	0.958	23.62	24.33
U	0.930	0.958	23.62	24.33
V	0.036	0.044	0.91	1.12
W	0.036	0.044	0.91	1.12
G1	0.890	0.930	22.61	23.62