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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	3MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.21x24.21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mchc711ks2cfne3

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.motorola.com/semiconductors

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
October, 2001	N/A	Original release	N/A

List of Sections

Section 3. Central Processor Unit (CPU)

required for wire-OR configuration. Software can change the triggering to edge sensitive.

$\overline{\text{XIRQ}}$ interrupts can be non-maskable after reset initialization. Out of reset, the X bit in the CCR is set, masking $\overline{\text{XIRQ}}$ interrupts. Once software clears the X bit, it cannot be reset, and the $\overline{\text{XIRQ}}$ interrupts become non-maskable. The $\overline{\text{XIRQ}}$ input is level sensitive only. $\overline{\text{XIRQ}}$ is often used as a power-loss detect interrupt.

Whenever $\overline{\text{IRQ}}$ or $\overline{\text{XIRQ}}$ is used with multiple interrupt sources, each source must drive the interrupt input with an open-drain type of driver to avoid contention between outputs. There should be a single pullup resistor near the MCU interrupt pin (typically 4.7 kΩ). There must also be an interlock mechanism at each interrupt source which holds the interrupt line low until the MCU recognizes and acknowledges the interrupt request. If any interrupt sources are still pending after the MCU services a request, the interrupt line will remain low, interrupting the MCU again as soon as the I bit in the MCU is cleared (normally upon return from an interrupt). Interrupt mechanisms are explained further in **Section 5. Resets and Interrupts**.

On EPROM devices, the $\overline{\text{XIRQ}}$ pin also functions as the high-voltage supply, V_{PP}, during EPROM or OTPROM programming.

CAUTION: *Ensure that the voltage level at this pin is equal to V_{DD} during normal operation to avoid programming accidents.*

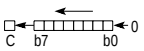
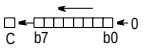
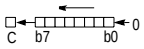
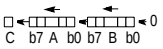
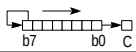
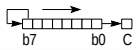
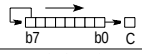
2.9 Mode Selection, Instruction Cycle Reference, and Standby Power (MODA/$\overline{\text{LIR}}$ and MODB/V_{STBY})

During reset, MODA and MODB select one of four operating modes:

1. Single-chip
2. Expanded
3. Bootstrap
4. Special test

For full descriptions of these modes, refer to **4.5 Operating Modes**.

Table 3-1. Instruction Set (Sheet 1 of 7)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
ABA	Add Accumulators	A + B ⇒ A	INH	1B	—	2	—	—	Δ	—	Δ	Δ	Δ	Δ
ABX	Add B to X	IX + (00 : B) ⇒ IX	INH	3A	—	3	—	—	—	—	—	—	—	—
ABY	Add B to Y	IY + (00 : B) ⇒ IY	INH	18 3A	—	4	—	—	—	—	—	—	—	—
ADCA (opr)	Add with Carry to A	A + M + C ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	89 99 B9 A9 18 A9	ii dd hh ll ff ff	2 3 4 4 5	—	—	Δ	—	Δ	Δ	Δ	Δ
ADCB (opr)	Add with Carry to B	B + M + C ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	C9 D9 F9 E9 18 E9	ii dd hh ll ff ff	2 3 4 4 5	—	—	Δ	—	Δ	Δ	Δ	Δ
ADDA (opr)	Add Memory to A	A + M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	8B 9B BB AB 18 AB	ii dd hh ll ff ff	2 3 4 4 5	—	—	Δ	—	Δ	Δ	Δ	Δ
ADDB (opr)	Add Memory to B	B + M ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	CB DB FB EB 18 EB	ii dd hh ll ff ff	2 3 4 4 5	—	—	Δ	—	Δ	Δ	Δ	Δ
ADDD (opr)	Add 16-Bit to D	D + (M : M + 1) ⇒ D	IMM DIR EXT IND,X IND,Y	C3 D3 F3 E3 18 E3	jj kk dd hh ll ff ff	4 5 6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
ANDA (opr)	AND A with Memory	A • M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	84 94 B4 A4 18 A4	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
ANDB (opr)	AND B with Memory	B • M ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	C4 D4 F4 E4 18 E4	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
ASL (opr)	Arithmetic Shift Left		EXT IND,X IND,Y	78 68 18 68	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
ASLA	Arithmetic Shift Left A		A INH	48	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ASLB	Arithmetic Shift Left B		B INH	58	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ASLD	Arithmetic Shift Left D		INH	05	—	3	—	—	—	—	Δ	Δ	Δ	Δ
ASR	Arithmetic Shift Right		EXT IND,X IND,Y	77 67 18 67	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
ASRA	Arithmetic Shift Right A		A INH	47	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ASRB	Arithmetic Shift Right B		B INH	57	—	2	—	—	—	—	Δ	Δ	Δ	Δ
BCC (rel)	Branch if Carry Clear	? C = 0	REL	24	rr	3	—	—	—	—	—	—	—	—
BCLR (opr) (msk)	Clear Bit(s)	M • ($\overline{mm}$) ⇒ M	DIR IND,X IND,Y	15 1D 18 1D	dd mm ff mm ff mm	6 7 8	—	—	—	—	Δ	Δ	0	—
BCS (rel)	Branch if Carry Set	? C = 1	REL	25	rr	3	—	—	—	—	—	—	—	—

NOTE: *Throughout this manual, the registers are discussed by function. In the event that not all bits in a register are referenced, the bits that are not discussed are shaded.*

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PORTA) See page 138.	Read: Write:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Reset:	Undefined after reset							
$0001	Port A Data Direction Register (DDRA) See page 138.	Read: Write:	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0
		Reset:	0	0	0	0	0	0	0	0
$0002	Port B Data Direction Register (DDRB) See page 139.	Read: Write:	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
		Reset:	0	0	0	0	0	0	0	0
$0003	Port F Data Direction Register (DDRF) See page 144.	Read: Write:	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0
		Reset:	0	0	0	0	0	0	0	0
$0004	Port B Data Register (PORTB) See page 139.	Read: Write:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
		Reset:	Undefined after reset							
$0005	Port F Data Register (PORTF) See page 144.	Read: Write:	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
		Reset:	Undefined after reset							
$0006	Port C Data Register (PORTC) See page 140.	Read: Write:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Reset:	Undefined after reset							
$0007	Port C Data Direction Register (DDRC) See page 141.	Read: Write:	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
		Reset:	0	0	0	0	0	0	0	0
$0008	Port D Data Register (PORTD) See page 142.	Read: Write:	0	0	PD5	PD4	PD3	PD2	PD1	PD0
		Reset:	0	0	U	U	U	U	U	U
$0009	Port D Data Direction Register (DDRD) See page 142.	Read: Write:	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Undefined

Figure 4-1. Register and Control Bit Assignments (Sheet 1 of 11)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0077	SCI Data Register (SCDR) See page 165.	Read: Write:	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0
		Reset:	Undefined after reset							
$0078	Reserved		R	R	R	R	R	R	R	R
to										
$007B	Reserved		R	R	R	R	R	R	R	R
$007C	Port H Data Register (PORTH) See page 146.	Read: Write:	PH7(1)	PH6(1)	PH5(1)	PH4(1)	PH3	PH2	PH1	PH0
		Reset:	Undefined after reset							
$007D	Port H Data Direction Register (DDRH) See page 146.	Read: Write:	DDH7(1)	DDH6(1)	DDH5(1)	DDH4(1)	DDH3	DDH2	DDH1	DDH0
		Reset:	0	0	0	0	0	0	0	0
$007E	Port G Data Register (PORTG) See page 145.	Read: Write:	PG7	PG6(1)	PG5(1)	PG4(1)	PG3(1)	PG2(1)	PG1(1)	PG0(1)
		Reset:	Undefined after reset							
$007F	Port G Data Direction Register (DDRG) See page 145.	Read: Write:	DDG7	DDG6(1)	DDG5(1)	DDG4(1)	DDG3(1)	DDG2(1)	DDG1(1)	DDG0(1)
		Reset:	0	0	0	0	0	0	0	0

1. Not available on M68HC11KS devices

= Unimplemented R = Reserved U = Undefined

Figure 4-1. Register and Control Bit Assignments (Sheet 11 of 11)

4.5 Operating Modes

The two normal modes of operation in the M68HC11K Family are:

- Single-chip mode — All port pins available for input/output (I/O); only on-board memory accessible
- Expanded mode — Access to internal and external memory; 25 I/O pins used for interface

The two special modes of operation are:

- Bootstrap mode — A variation of single-chip mode; executes a bootloader program in an internal bootstrap read-only memory (ROM)
- Test mode — A variation of the expanded mode used in production testing; allows privileged access to internal resources

The logic levels applied at reset to input pins MODA and MODB determine the operating mode. See **4.5.5 Mode Selection**.

4.5.1 Single-Chip Mode

In single-chip mode, the MCU functions as a self-contained microcontroller. In this mode, all address and data activity occurs within the MCU. Ports B, C, F, G, and H are available for general-purpose I/O because the external address and data buses are not required.

4.5.2 Expanded Mode

In expanded mode, the MCU uses ports B, C, F, and G to access a 64-Kbyte address space. This includes:

- The same on-chip memory addresses used in single-chip mode
- External memory
- Peripheral devices

Address: $0037

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EE3	EE2	EE1	EE0	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

Figure 4-7. EEPROM Mapping Register (INIT2)

NOTE: *INIT2 is writable once in normal modes and writable at any time in special modes.*

EE[3:0] — EEPROM Map Position Bits

These four bits determine the most-significant hexadecimal digit in the address range of the EEPROM, as shown in **Table 4-7**.

Table 4-7. EEPROM Map

EE[3:0]	Location
0000	$0D80–$0FFF
0001	$1D80–$1FFF
0010	$2D80–$2FFF
0011	$3D80–$3FFF
0100	$4D80–$4FFF
0101	$5D80–$5FFF
0110	$6D80–$6FFF
0111	$7D80–$7FFF
1000	$8D80–$8FFF
1001	$9D80–$9FFF
1010	$AD80–$AFFF
1011	$BD80–$BFFF
1100	$CD80–$CFFF
1101	$DD80–$DFFF
1110	$ED80–$EFFF
1111	$FD80–$FFFF

4.6.4 Bootloader ROM

The bootloader program occupies 512 bytes of bootstrap ROM at addresses $BE00–$BFFF. It is active only in special modes when the RBOOT bit in the HPRIO register is set.

4.7 EPROM/OTPROM (M68HC711K4 and M68HC711KS2)

The M68HC711K4 devices include 24 Kbytes of on-chip EPROM (OTPROM in non-windowed packages). The M68HC711KS2 has 32 Kbytes of EPROM.

The two methods available to program the EPROM are:

- Downloading data through the serial communication interface (SCI) in bootstrap or special test mode
- Programming individual bytes from memory

Before proceeding with programming:

- Ensure that the CONFIG register ROMON bit is set.
- Ensure that the $\overline{\text{IRQ}}$ pin is pulled to a high level.
- Apply 12 volts to the $\overline{\text{XIRQ}}/V_{PP}$ pin.

Program the EPROM only at room temperature. Place an opaque label over the quartz window on windowed parts after programming.

4.7.1 Programming the EPROM with Downloaded Data

The MCU can download EPROM data through the SCI while in the special test or bootstrap modes. This can be done either with custom software, also downloaded through the SCI, or with a built-in utility program in bootstrap ROM. In either case, the 12-volt nominal programming voltage must be present on the $\overline{\text{XIRQ}}/V_{PP}$ pin.

To use the bootstrap ROM utility, download a 3-byte program consisting of a single jump instruction to $BF00, the starting address of the resident EPROM programming utility. The utility program sets the X and Y index

ELAT — EPROM Latch Control Bit

Setting ELAT latches the address and data of writes to the EPROM. The EPROM cannot be read. ELAT can be read at any time. ELAT can be written any time except when PGM = 1, which disables writes to ELAT.

0 = EPROM address and data bus configured for normal reads. EPROM cannot be programmed.

1 = EPROM address and data bus are configured for programming. Address and data of writes to EPROM are latched. EPROM cannot be read.

EXCOL — Select Extra Columns Bit

EXCOL is for factory use only and is accessible only in special test mode. When EXCOL equals 1, extra columns can be accessed at bit 7 and bit 0. Addresses use bits [11:5]. Bits [4:1] are ignored.

0 = User array selected

1 = Extra columns selected and user array disabled

EXROW — Select Extra Rows Bit

EXROW is for factory use only and is only accessible in special test mode. When EXROW equals 1, two extra rows are available. Addresses use bits [5:0]. Bits [11:6] are ignored.

0 = User array selected

1 = Extra rows selected and user array is disabled

EPGM — EPROM Programming Enable Bit

EPGM applies programming voltage (V_{PP}) to the EPROM. EPGM can be read at any time. EPGM can be written only when ELAT = 1.

0 = Programming voltage to EPROM array is disconnected

1 = Programming voltage to EPROM array is connected; ELAT cannot be changed.

4.9 XOUT Pin Control

The XOUT pin provides a buffered XTAL signal to synchronize external devices with the MCU. It is enabled by the CLKX bit in the system configuration (CONFIG) register. The frequency of XOUT can be divided by one-of-four divisors selected by the XDV[1:0] bits in the system configuration options 2 (OPT2) register. The XOUT pin is not configured on all packages. Refer to the pin assignments in **Section 2. Pin Description**.

4.9.1 System Configuration Register

Address: $003F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ROMAD	1	CLKX	PAREN	NOSEC	NOCOP	ROMON	EEON
Reset:	—	1	—	—	1	—	—	—

Figure 4-14. System Configuration Register (CONFIG)

Writable once in normal modes and writable at any time in special modes

CLKX — XOUT Clock Enable Bit

The CLKX bit is a switch that enables a buffered clock running at the same frequency as a referenced crystal. This buffered clock is intended to synchronize external devices with the MCU.

0 = The XOUT pin is disabled.

1 = The X clock is driven out on the XOUT pin.

6.10 Port H

The state of port H pin 7 (PH7) at reset is mode dependent. In single-chip or bootstrap modes, it is a high-impedance input; its data direction can be changed through DDRH. In expanded and special test modes PH7 is the program chip select line, $\overline{\text{CSPROG}}$ at reset, but can be reconfigured for GPIO (see **11.4 Chip Selects**).

Port H pins (PH[6:0]) reset to high-impedance inputs in any mode. Data direction can be changed through DDRH. Except for the M68HC11KS devices, bits 6:4 can serve as chip select lines in expanded and special test modes (see **11.4 Chip Selects**). Pins 3:0 can be configured as pulse-width modulator outputs (see **9.9 Pulse-Width Modulator (PWM)**) in any mode.

All eight port H pins have selectable internal pullup resistors (see **6.11 Internal Pullup Resistors**).

Address: $007C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PH7(1)	PH6(1)	PH5(1)	PH4(1)	PH3	PH2	PH1	PH0
Reset:	0	0	0	0	0	0	0	0
Alternate Pin Function:	CSPROG	CSPG2	CSPG1	CSIO	PW4	PS3	PS2	PS1

1. Not available on KS devices

Figure 6-15. Port H Data Register (PORTH)

Address: $007D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDH7(1)	DDH6(1)	DDH5(1)	DDH4(1)	DDH3	DDH2	DDH1	DDH0
Reset:	0	0	0	0	0	0	0	0

1. Not available on KS devices

Figure 6-16. Port H Data Direction Register (DDRH)

DDH[7:0] — Data Direction for Port H Bits

0 = Input

1 = Output

CPOL — Clock Polarity Bit

When the clock polarity bit is cleared and data is not being transferred, the SCK pin of the master device has a steady state low value. When CPOL is set, SCK idles high.

CPHA — Clock Phase Bit

The clock phase bit, in conjunction with the CPOL bit, controls the clock-data relationship between master and slave. The CPHA bit selects one of two different clocking protocols.

SPR[1:0] — SPI Clock Rate Select Bits

On a master device, these two bits in conjunction with SPR2 in the OPT2 register select the baud rate to be used as SCK. See **Table 8-1**. These bits have no effect in slave mode.

Table 8-1. SPI+ Baud Rates

EXTAL Frequencies						
EXTAL Freq.	**8.0 MHz**	**12.0 MHz**	**16.0 MHz**	**20.0 MHz**	**24.0 MHz**	**Other EXTAL**
E Clock Freq.	**2.0 MHz**	**3.0 MHz**	**4.0 MHz**	**5.0 MHz**	**6.0 MHz**	**EXTAL ÷ 4**
Control Bits SPR[2:0]	**SPI Baud Rate**					**E Clock Divide by**
0 0 0	1.0 MHz	1.5 MHz	2.0 MHz	2.5 MHz	3.0 MHz	2
0 0 1	500 kHz	750 kHz	1.0 MHz	1.3 kHz	1.5 MHz	4
0 1 0	125 kHz	187.5 kHz	250 kHz	312.5 kHz	375.0 kHz	16
0 1 1	62.5 kHz	93.8 kHz	125 kHz	156.3 kHz	187.5 kHz	32
1 0 0	250 kHz	375 kHz	500 kHz	625 kHz	750.0 kHz	8
1 0 1	125 kHz	187.5 kHz	250 kHz	312.5 kHz	375.0 kHz	16
1 1 0	31.3 kHz	46.9 kHz	62.5 kHz	78.1 kHz	93.8 kHz	64
1 1 1	15.6 kHz	23.4 kHz	31.3 kHz	39.1 kHz	46.9 kHz	128

9.2 Introduction

M68HC11 microcontrollers contain an extensive timing system to support a wide variety of timer-related functions. This section discusses the nature of the timing system and presents details of timer-related functions including:

- Input capture/output compare (IC/OC)
- Real-time interrupt (RTI)
- Pulse accumulator (PA)
- Pulse width modulation (PWM)

11.4.3.1 Memory Mapping Size Register

Address: $0056

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	MXGS2	MXGS1	W2SZ1	W2SZ0	0	0	W1SZ1	W1SZ0
Reset:	0	0	0	0	0	0	0	0

Figure 11-7. Memory Mapping Size Register (MMSIZ)

MXGS2 — Memory Expansion Select for GPCS 2 Bit
0 = GPCS 2 based on 64-Kbyte CPU address
1 = GPCS 2 based on expansion address

MXGS1 — Memory Expansion Select for GPCS 1 Bit
0 = GPCS 1 based on 64-Kbyte CPU address
1 = GPCS 1 based on expansion address

11.4.3.2 General-Purpose Chip Select 1 Address Register

Address: $005C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	G1A18	G1A17	G1A16	G1A15	G1A14	G1A13	G1A12	G1A11
Reset:	0	0	0	0	0	0	0	0

Figure 11-8. General-Purpose Chip Select 1 Address Register (GPCS1A)

G1A[18:11] — General-Purpose Chip Select 1 Address Bits
They select the starting address of GPCS1. Refer to **Table 11-6**.

12.2 Introduction

This section contains electrical parameters for standard and extended voltage devices. When applicable, extended voltage parameters are shown separately. Diagrams apply to both standard and extended voltage devices.

12.3 Maximum Ratings for Standard Devices

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

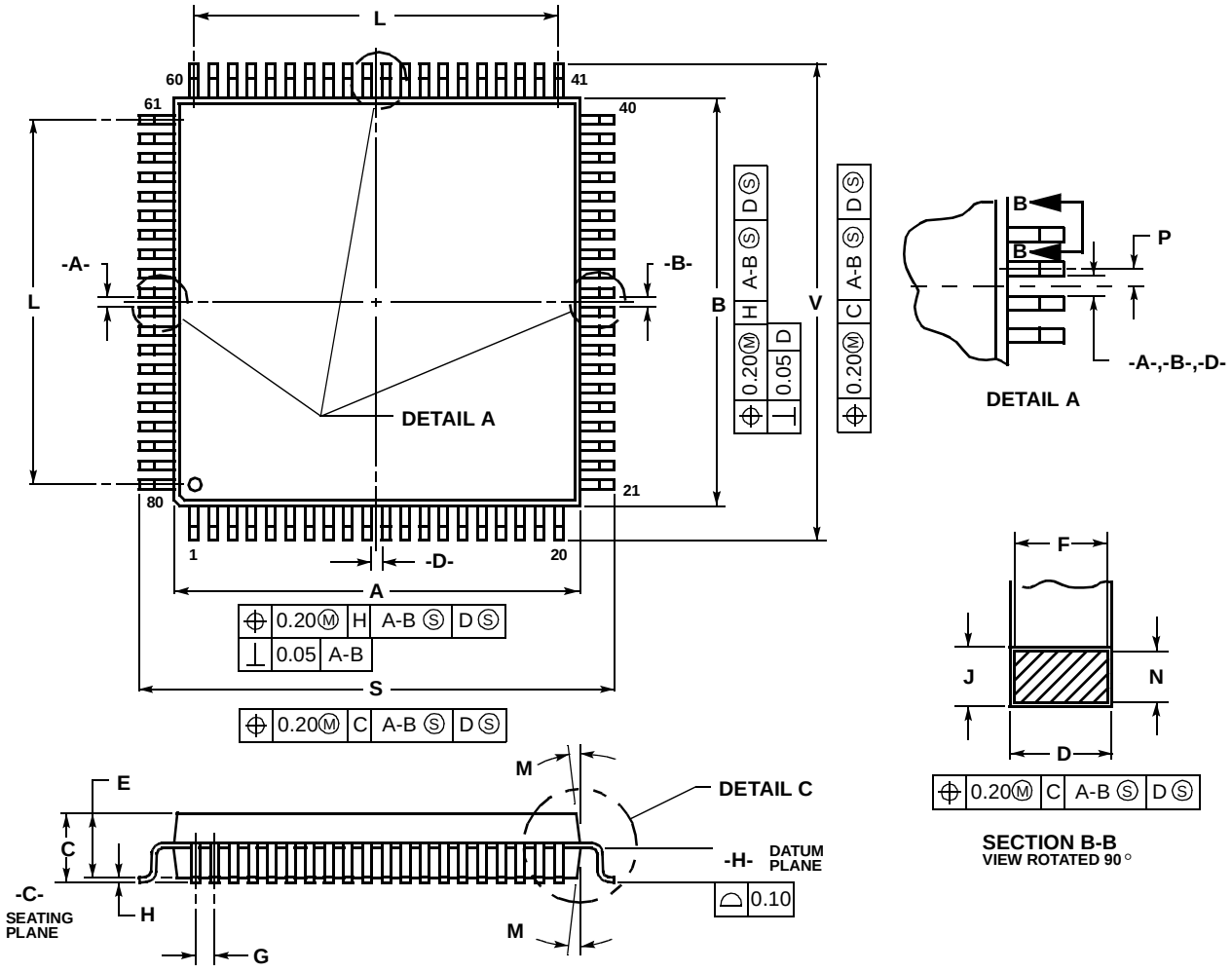
NOTE: *This device is not guaranteed to operate properly at the maximum ratings. Refer to* ***12.6 Electrical Characteristics*** *for guaranteed operating conditions.*

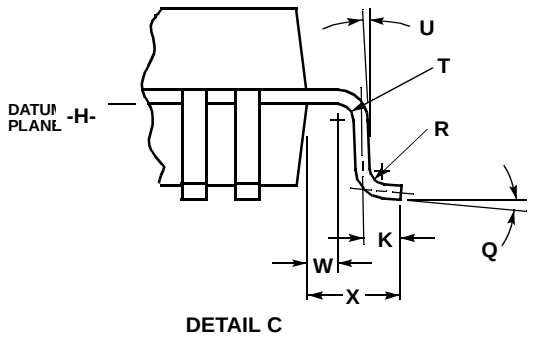
Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +7.0	V
Input voltage	V_{In}	–0.3 to +7.0	V
Current drain per pin(1) excluding V_{DD}, V_{SS}, AV_{DD}, V_{RH}, and V_{RL}	I_D	25	mA
Storage temperature	T_{STG}	–55 to +150	°C

1. One pin at a time, observing maximum power dissipation limits

NOTE: *This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{In} and V_{Out} be constrained to the range $V_{SS} \le (V_{In}$ or $V_{Out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either V_{SS} or V_{DD}).*

13.5 80-Pin Quad Flat Pack (Case 841B)

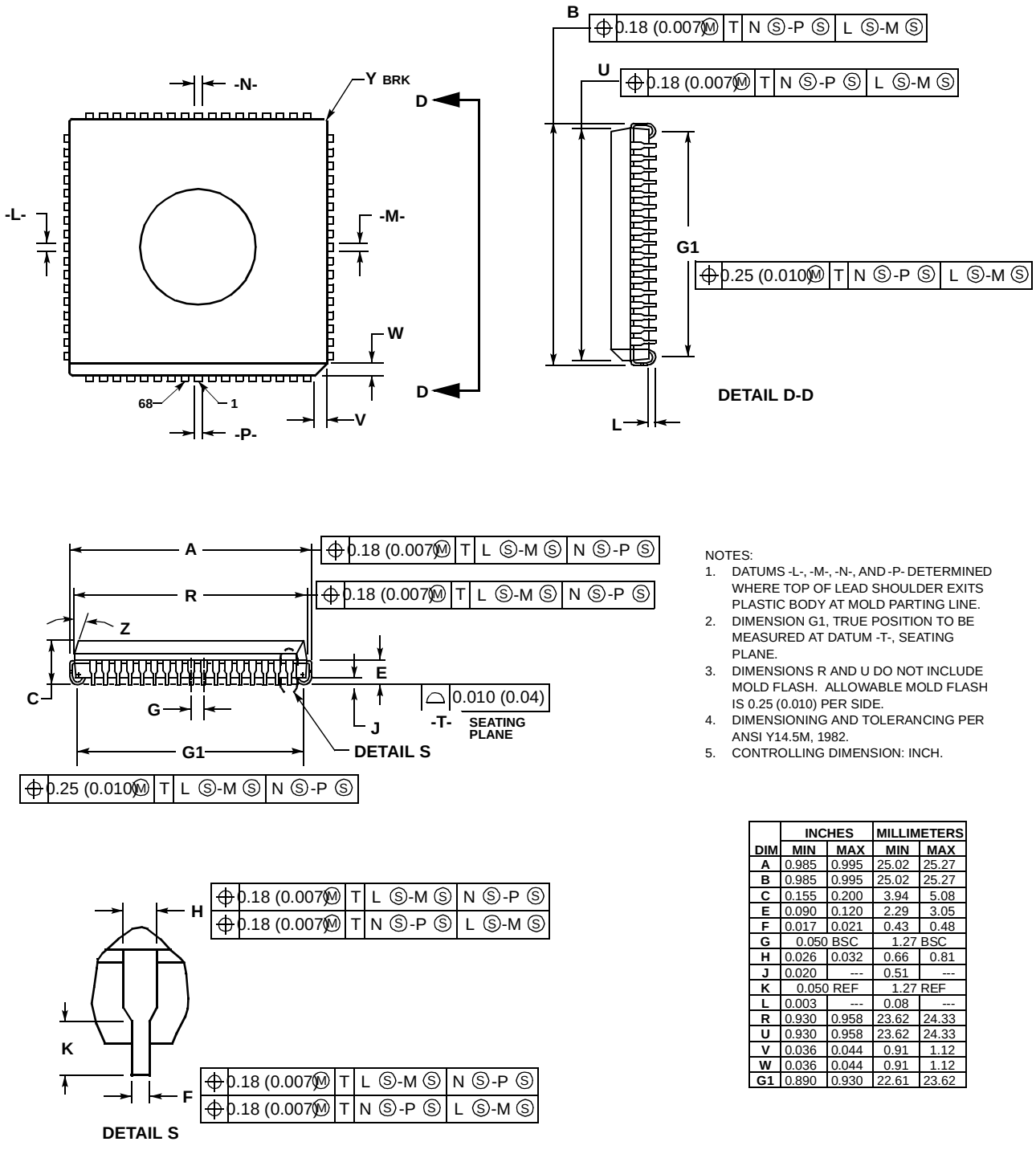




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS	
DIM	MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5°	10°
N	0.13	0.17
P	0.325 BSC	
Q	0°	7°
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0°	---
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	

13.8 68-Pin J-Cerquad (Case 779A)



NOTES:
1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.985	0.995	25.02	25.27
B	0.985	0.995	25.02	25.27
C	0.155	0.200	3.94	5.08
E	0.090	0.120	2.29	3.05
F	0.017	0.021	0.43	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.050 REF		1.27 REF	
L	0.003	---	0.08	---
R	0.930	0.958	23.62	24.33
U	0.930	0.958	23.62	24.33
V	0.036	0.044	0.91	1.12
W	0.036	0.044	0.91	1.12
G1	0.890	0.930	22.61	23.62

T