Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	4MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.21x24.21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mchc711ks2cfne4

Table of Contents

Section 1. General Description

Section 2. Pin Description

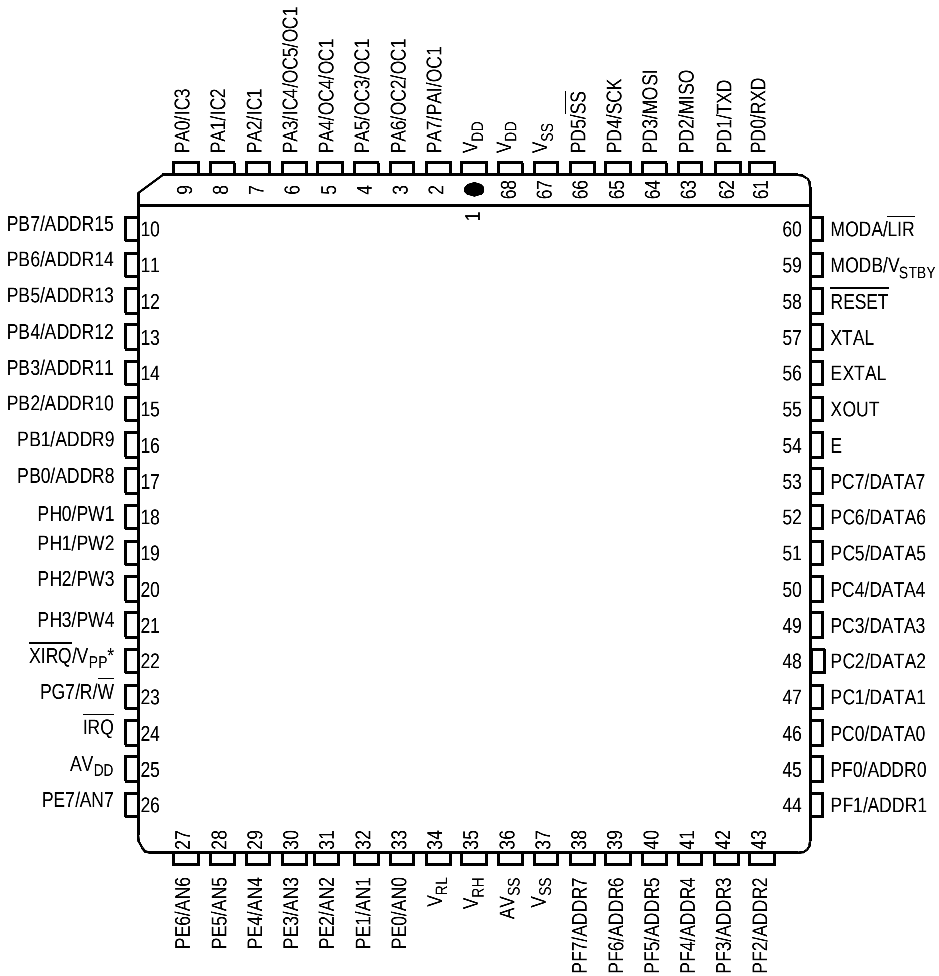
Section 12. Electrical Characteristics

Section 13. Mechanical Data

Section 14. Ordering Information

Section 15. Development Support

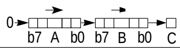
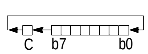
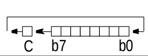
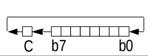
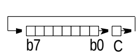
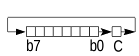
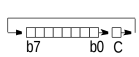
Index



* V_{PP} applies only to EPROM devices.

Figure 2-3. Pin Assignments for M6811KS 68-Pin PLCC/J-Cerquad

Table 3-1. Instruction Set (Sheet 5 of 7)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
LSRD	Logical Shift Right Double		INH	04	—	3	—	—	—	—	0	Δ	Δ	Δ
MUL	Multiply 8 by 8	A ∗ B ⇒ D	INH	3D	—	10	—	—	—	—	—	—	—	Δ
NEG (opr)	Two's Complement Memory Byte	0 – M ⇒ M	EXT IND,X IND,Y	70 60 18 60	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
NEGA	Two's Complement A	0 – A ⇒ A	A INH	40	—	2	—	—	—	—	Δ	Δ	Δ	Δ
NEGB	Two's Complement B	0 – B ⇒ B	B INH	50	—	2	—	—	—	—	Δ	Δ	Δ	Δ
NOP	No operation	No Operation	INH	01	—	2	—	—	—	—	—	—	—	—
ORAA (opr)	OR Accumulator A (Inclusive)	A + M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	8A 9A BA AA 18 AA	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
ORAB (opr)	OR Accumulator B (Inclusive)	B + M ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	CA DA FA EA 18 EA	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
PSHA	Push A onto Stack	A ⇒ Stk,SP = SP – 1	A INH	36	—	3	—	—	—	—	—	—	—	—
PSHB	Push B onto Stack	B ⇒ Stk,SP = SP – 1	B INH	37	—	3	—	—	—	—	—	—	—	—
PSHX	Push X onto Stack (Lo First)	IX ⇒ Stk,SP = SP – 2	INH	3C	—	4	—	—	—	—	—	—	—	—
PSHY	Push Y onto Stack (Lo First)	IY ⇒ Stk,SP = SP – 2	INH	18 3C	—	5	—	—	—	—	—	—	—	—
PULA	Pull A from Stack	SP = SP + 1, A ⇐ Stk	A INH	32	—	4	—	—	—	—	—	—	—	—
PULB	Pull B from Stack	SP = SP + 1, B ⇐ Stk	B INH	33	—	4	—	—	—	—	—	—	—	—
PULX	Pull X From Stack (Hi First)	SP = SP + 2, IX ⇐ Stk	INH	38	—	5	—	—	—	—	—	—	—	—
PULY	Pull Y from Stack (Hi First)	SP = SP + 2, IY ⇐ Stk	INH	18 38	—	6	—	—	—	—	—	—	—	—
ROL (opr)	Rotate Left		EXT IND,X IND,Y	79 69 18 69	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
ROLA	Rotate Left A		A INH	49	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ROLB	Rotate Left B		B INH	59	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ROR (opr)	Rotate Right		EXT IND,X IND,Y	76 66 18 66	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
RORA	Rotate Right A		A INH	46	—	2	—	—	—	—	Δ	Δ	Δ	Δ
RORB	Rotate Right B		B INH	56	—	2	—	—	—	—	Δ	Δ	Δ	Δ
RTI	Return from Interrupt	See Figure 3-2	INH	3B	—	12	Δ	↓	Δ	Δ	Δ	Δ	Δ	Δ
RTS	Return from Subroutine	See Figure 3-2	INH	39	—	5	—	—	—	—	—	—	—	—

4.2 Introduction

This section presents the elements involved in configuring the M68HC11K/KS Family microcontrollers (MCUs), including:

- A list of the control registers, see **4.3 Control Registers**
- Special registers that control system initialization, see **4.4 System Initialization**
- Description of the four operating modes and how they're selected, see **4.5 Operating Modes**
- Memory maps of the K Family, see **4.6 Memory Map**
- Information on programming EPROM (erasable, programmable read-only memory) and EEPROM (electrically erasable, programmable read-only memory), see **4.7 EPROM/OTPROM (M68HC711K4 and M68HC711KS2)** and **4.8 EEPROM and the CONFIG Register**

4.3 Control Registers

The heart of the M68HC11 Family of MCUs is a special register block which controls the peripheral functions. In the K Family, this block is 128 bytes. The default location of this block is the first 128 bytes of memory, but software can map it to any 4-Kbyte boundary (see **4.6.1 Control Registers and RAM**).

Certain bits and registers that control initialization and the basic operation of the MCU are protected against writes in normal operating modes except under special circumstances. Some bits cannot be written at all; others can be written only once and/or within the first 64 bus cycles after any reset. The special operating modes override these restrictions. These bits and registers are discussed in **4.4 System Initialization**.

Normal and special operating modes are discussed in **4.5 Operating Modes**. The write-restricted registers and bits are summarized in **Table 4-1**.

Figure 4-1 lists the entire 128-byte register block in ascending order by address, using the default memory block assignment $0000–$007F.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$006C	Pulse Width Modulation Timer Duty Cycle 1 Register (PWDTY1) See page 219.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$006D	Pulse Width Modulation Timer Duty Cycle 2 Register (PWDTY2) See page 219.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$006E	Pulse Width Modulation Timer Duty Cycle 3 Register (PWDTY3) See page 219.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$006F	Pulse Width Modulation Timer Duty Cycle 4 Register (PWDTY4) See page 219.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$0070	SCI Baud Rate Control Register High (SCBDH) See page 158.	Read: Write:	BTST	BSPL	0	SBR12	SBR11	SBR10	SBR9	SBR8
		Reset:	0	0	0	0	0	0	0	0
$0071	SCI Baud Rate Control Register Low (SCBDL) See page 158.	Read: Write:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		Reset:	0	0	0	0	0	1	0	0
$0072	SCI Control Register 1 (SCCR1) See page 160.	Read: Write:	LOOPS	WOMS	0	M	WAKE	ILT	PE	PT
		Reset:	U	U	0	0	0	0	0	0
$0073	SCI Control Register 2 (SCCR2) See page 161.	Read: Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Reset:	0	0	0	0	0	0	0	0
$0074	SCI Status Register 1 (SCSR1) See page 162.	Read: Write:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Reset:	0	0	0	0	0	0	0	0
$0075	SCI Status Register 2 (SCSR2) See page 164.	Read: Write:	0	0	0	0	0	0	0	RAF (Write: unimplemented)
		Reset:	1	1	0	0	0	0	0	0
$0076	SCI Data Register (SCDR) See page 165.	Read: Write:	R8	T8	0	0	0	0	0	0
		Reset:	Undefined after reset							

(gray) = Unimplemented R = Reserved U = Undefined

Figure 4-1. Register and Control Bit Assignments (Sheet 10 of 11)

registers to default values, then receives data from an external host and programs it into the EPROM. The value in the X index register determines programming delay time. The value in the Y index register is a pointer to the first address in EPROM to be programmed. The default starting address is $8000 for the M68HC11KS2.

When the utility program is ready to receive programming data, it sends the host a $FF character and waits for a reply. When the host sees the $FF character, it sends the EPROM programming data, starting with the first location in the EPROM array. After the MCU receives the last byte to be programmed and returns the corresponding verification data, it terminates the programming operation by initiating a reset. Refer to the Motorola application note entitled *MC68HC11 Bootstrap Mode,* document order number AN1060/D.

4.7.2 Programming the EPROM from Memory

In this method, software programs the EPROM one byte at a time. Each byte is read from memory, then latched and programmed into the EPROM using the EPROM programming control register (EPROG). This procedure can be done in any operating mode.

Address: $002B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	R	0	ELAT	EXCOL	EXROW	0	0	EPGM
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 4-8. EPROM Programming Control Register (EPROG)

MBE — Multiple-Byte Program Enable Bit

MBE is for factory use only and is accessible only in special test mode. When MBE is set, the MCU ignores address bit 5, so that bytes with ADDR5 = 0 and ADDR5 = 1 both get programmed with the same data.

0 = Normal programming
1 = Multiple-byte programming enabled

The procedures for both writing and erasing involve these five steps:

1. **Set the EELAT bit in PPROG**. If erasing, also set the ERASE bit and the appropriate BYTE and ROW bits.
2. **Write data to the appropriate EEPROM address**. If erasing, any data will work. To erase a row, write to any location in the row. To erase the entire EEPROM, write to any location in the array. This step is done before applying the programming voltage because setting the EEPGM bit inhibits writes to EEPROM addresses.
3. **Set the EEPGM bit in PPROG,** keeping EELAT set. If erasing, also set the ERASE bit and the appropriate BYTE and ROW bits.
4. **Delay for 10 ms**.
5. **Clear the PPROG register** to turn off the high voltage and reconfigure the EEPROM address and data buses for normal operation.

The following examples demonstrate programming a single EEPROM byte, erasing the entire EEPROM, erasing a row (16 bytes), and erasing a single byte.

4.8.2.1 EEPROM Programming

On entry, accumulator A contains the data to be written and X points to the address to be programmed.

```
EEPROG   LDAB   #$02
         STAB   $003B    Set EELAT bit to enable EEPROM
                         latches.
         STAA   $0,X     Store data to EPROM address
         LDAB   #$03
         STAB   $002B    Set EPGM bit with ELAT=1
                         to enable EEPROM programming voltage
         JSR    DLY10    Delay 10 ms
         CLR    $003B    Turn off programming voltage and set
                         to READ mode
```

4.8.3 CONFIG Register Programming

The CONFIG register is implemented with EEPROM cells, so EEPROM procedures are required to change it. CONFIG can be programmed or erased (including byte erase) while the MCU is operating in any mode, provided that PTCON in BPROT is clear.

Address: $0035

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BULKP	LVPEN	BPRT4	PTCON	BPRT3	BPRT2	BPRT1	BPRT0
Reset:	1	1	1	1	1	1	1	1

Figure 4-12. Block Protect Register (BPROT)

PTCON — Protect for CONFIG Bit

0 = CONFIG register can be programmed or erased normally.

1 = CONFIG register cannot be programmed or erased.

To change the value in the CONFIG register, complete this procedure. Do not initiate a reset until the procedure is complete.

- Erase the CONFIG register.
- Program the new value to the CONFIG address.
- Initiate reset.

4.8.4 RAM and EEPROM Security

The NOSEC bit in the CONFIG register enables and disables an optional security feature which protects the contents of EEPROM and RAM from unauthorized access. This is done by restricting operation to single-chip modes, preventing the memory locations from being monitored externally. Single-chip modes do not allow visibility of the internal address and data buses. Resident programs, however, have unlimited access to the internal EEPROM and RAM and can read, write, or transfer the contents of these memories.

Section 7. Serial Communications Interface (SCI)

7.1 Contents

7.2 Introduction

The serial communications interface (SCI) is a universal asynchronous receiver transmitter (UART) employing a standard non-return-to-zero (NRZ) format. Several baud rates are available. The SCI transmitter and receiver are independent, but they use the same data format and baud rate.

CPOL selects an active high or low clock edge. CPHA selects one of two transfer formats. When CPHA is cleared, the shift clock is ORed with $\overline{SS}$. Each slave's $\overline{SS}$ pin must be pulled high before it writes the next output byte to its data register. If a slave writes to its data register while $\overline{SS}$ is low, a write collision error occurs. When CPHA is set, $\overline{SS}$ may be left low for several SPI characters. When there is only one SPI slave MCU, its $\overline{SS}$ line may be tied to V_{SS} if CPHA = 1 at all times.

The SPI configuration determines the characteristics of a transfer in progress. For a master, a transfer begins when data is written to SPDR and ends when SPIF is set. For a slave with CPHA cleared, a transfer starts when $\overline{SS}$ goes low and ends when $\overline{SS}$ returns high. In this case, SPIF is set at the middle of the eighth SCK cycle when data is transferred from the shifter to the parallel data register, but the transfer is still in progress until $\overline{SS}$ goes high. For a slave with CPHA set, transfer begins when the SCK line goes to its active level, which is the edge at the beginning of the first SCK cycle. The transfer ends when SPIF is set. SCK in a slave must be inactive for at least two E-clock cycles between byte transfers.

8.5 SPI System Errors

Two types of errors can be detected by the SPI system:

- A mode fault error can occur when multiple devices attempt to act in master mode simultaneously.
- A write collision error results from an attempt to write data to the SPDR while a transmission is in progress.

8.5.1 Mode Fault Error

A mode fault error occurs when the $\overline{SS}$ input line of an SPI system configured as a master goes to active low, usually because two devices have attempted to act as master at the same time. The resulting contention between push-pull CMOS pin drivers can cause them permanent damage. The mode fault disables the drivers in an attempt to protect them. The MSTR control bit in the SPCR and all four DDRD

CPOL — Clock Polarity Bit

When the clock polarity bit is cleared and data is not being transferred, the SCK pin of the master device has a steady state low value. When CPOL is set, SCK idles high.

CPHA — Clock Phase Bit

The clock phase bit, in conjunction with the CPOL bit, controls the clock-data relationship between master and slave. The CPHA bit selects one of two different clocking protocols.

SPR[1:0] — SPI Clock Rate Select Bits

On a master device, these two bits in conjunction with SPR2 in the OPT2 register select the baud rate to be used as SCK. See **Table 8-1**. These bits have no effect in slave mode.

Table 8-1. SPI+ Baud Rates

EXTAL Frequencies						
EXTAL Freq.	**8.0 MHz**	**12.0 MHz**	**16.0 MHz**	**20.0 MHz**	**24.0 MHz**	**Other EXTAL**
E Clock Freq.	**2.0 MHz**	**3.0 MHz**	**4.0 MHz**	**5.0 MHz**	**6.0 MHz**	**EXTAL ÷ 4**
Control Bits SPR[2:0]	**SPI Baud Rate**					**E Clock Divide by**
0 0 0	1.0 MHz	1.5 MHz	2.0 MHz	2.5 MHz	3.0 MHz	2
0 0 1	500 kHz	750 kHz	1.0 MHz	1.3 kHz	1.5 MHz	4
0 1 0	125 kHz	187.5 kHz	250 kHz	312.5 kHz	375.0 kHz	16
0 1 1	62.5 kHz	93.8 kHz	125 kHz	156.3 kHz	187.5 kHz	32
1 0 0	250 kHz	375 kHz	500 kHz	625 kHz	750.0 kHz	8
1 0 1	125 kHz	187.5 kHz	250 kHz	312.5 kHz	375.0 kHz	16
1 1 0	31.3 kHz	46.9 kHz	62.5 kHz	78.1 kHz	93.8 kHz	64
1 1 1	15.6 kHz	23.4 kHz	31.3 kHz	39.1 kHz	46.9 kHz	128

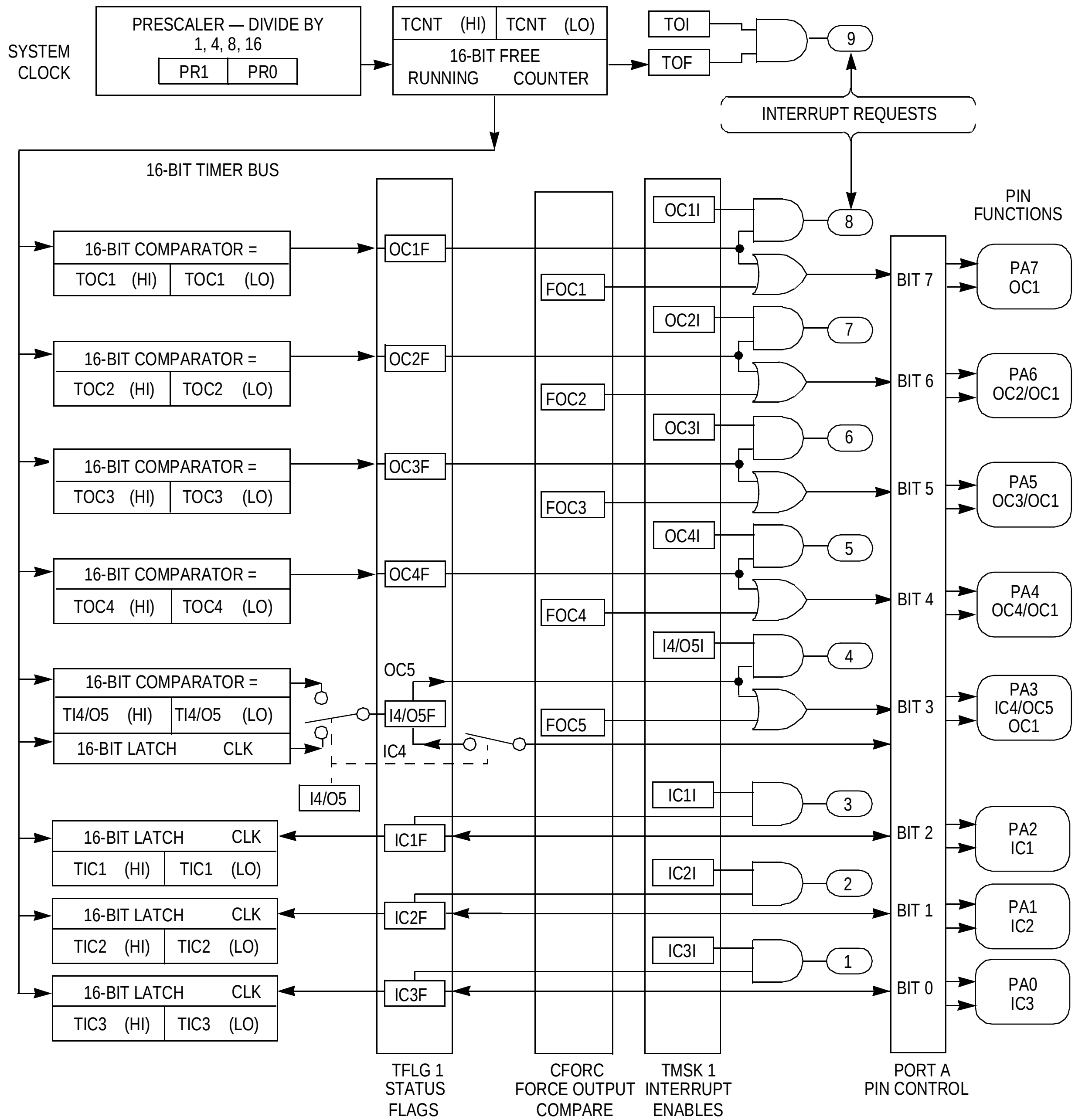


Figure 9-2. Capture/Compare Block Diagram

	Bit 7	6	5	4	3	2	1	Bit 0
Address: $001A— TOC3 (High)								
Read: / Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1
Address: $001B — TOC3 (Low)								
Read: / Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1
Address: $001C— TOC4 (High)								
Read: / Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1
Address: $001D — TOC4 (Low)								
Read: / Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1

Figure 9-13. Timer Output Compare Registers (TOC1–TOC4) (Continued)

All output compare registers are 16-bit read-write. Any of these registers can be used as a storage location if it is not used for output compare or input capture.

12.2 Introduction

This section contains electrical parameters for standard and extended voltage devices. When applicable, extended voltage parameters are shown separately. Diagrams apply to both standard and extended voltage devices.

12.3 Maximum Ratings for Standard Devices

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

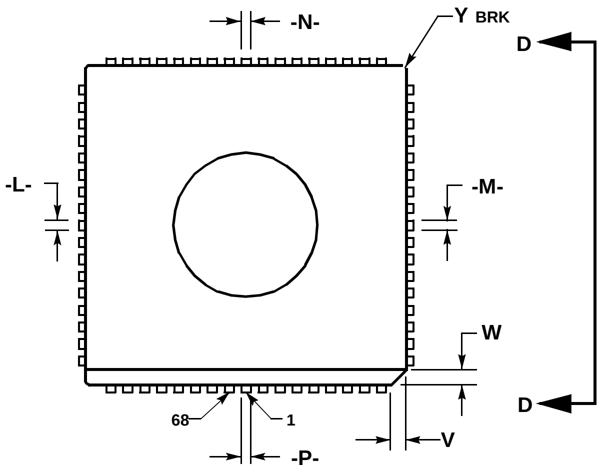
NOTE: *This device is not guaranteed to operate properly at the maximum ratings. Refer to* ***12.6 Electrical Characteristics*** *for guaranteed operating conditions.*

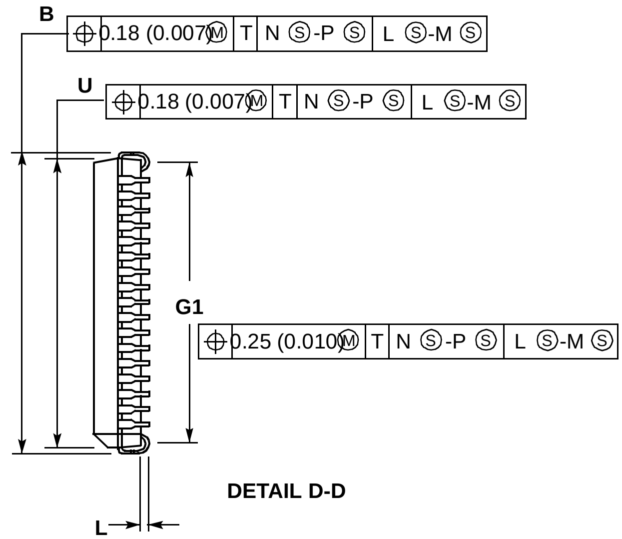
Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +7.0	V
Input voltage	V_{In}	–0.3 to +7.0	V
Current drain per pin[1] excluding V_{DD}, V_{SS}, AV_{DD}, V_{RH}, and V_{RL}	I_D	25	mA
Storage temperature	T_{STG}	–55 to +150	°C

1. One pin at a time, observing maximum power dissipation limits

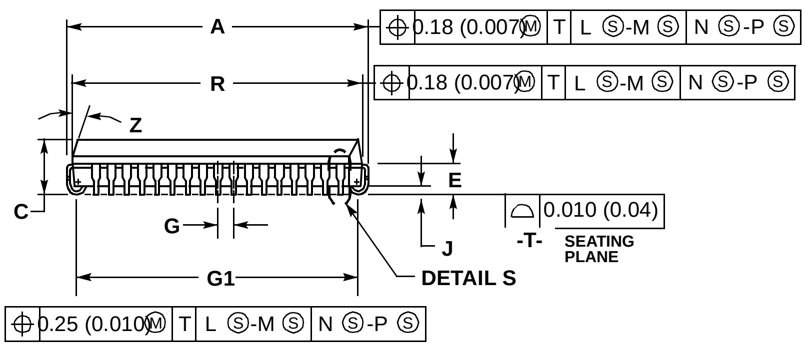
NOTE: *This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{In} and V_{Out} be constrained to the range $V_{SS} \leq (V_{In}$ or $V_{Out}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either V_{SS} or V_{DD}).*

13.8 68-Pin J-Cerquad (Case 779A)



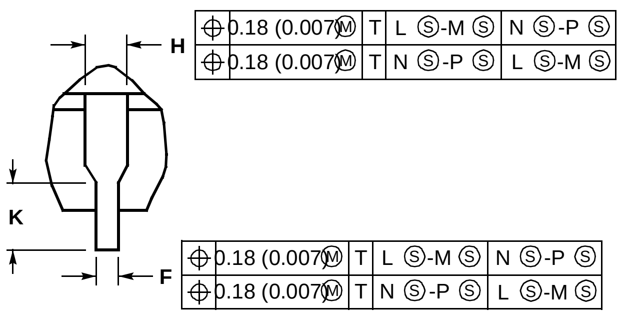


DETAIL D-D



NOTES:
1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.985	0.995	25.02	25.27
B	0.985	0.995	25.02	25.27
C	0.155	0.200	3.94	5.08
E	0.090	0.120	2.29	3.05
F	0.017	0.021	0.43	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.050 REF		1.27 REF	
L	0.003	---	0.08	---
R	0.930	0.958	23.62	24.33
U	0.930	0.958	23.62	24.33
V	0.036	0.044	0.91	1.12
W	0.036	0.044	0.91	1.12
G1	0.890	0.930	22.61	23.62



DETAIL S