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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	3MHz
Connectivity	SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	640 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.21x24.21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mchc711ks2vfne3

List of Sections

Section 4. Operating Modes and On-Chip Memory

1.4 Features

M68HC11K Family features include:

- 8-bit opcodes and data
- 16-bit addressing
- Two 8-bit accumulators, which can be concatenated to form one 16-bit accumulator
- On-board memory:
  - 24 Kbytes or 32 Kbytes of ROM, EPROM, or OTPROM
  - 768 bytes or 1 Kbyte of static RAM (random-access memory)
  - 640 bytes of EEPROM
  - 128-byte register block
- Dual-function I/O lines — Any pins used for the microcontroller's peripheral functions can be configured as general-purpose I/O lines.
- Non-multiplexed address and data buses
- 68HC11K4 offers:
  - 1 Mbyte of address space, using on-chip memory mapping logic
  - Four programmable chip selects (expanded modes)
- 16-bit timer system:
  - Three input capture (IC) channels, record event timing by storing the value of the timing system's 16-bit free-running counter when an input signal transition occurs.
  - Four output compare (OC) channels, provide timed outputs by signaling when the free-running counter reaches a predetermined number.
  - One IC or OC channel (software selectable)
- 8-bit pulse accumulator
- Four 8-bit pulse-width modulation (PWM) outputs
- Enhanced asynchronous serial communications interface (SCI)

- Enhanced synchronous serial peripheral interface (SPI)
- 8-channel, 8-bit, analog-to-digital (A/D) converter
- Computer operating properly (COP) watchdog system to guard against infinite loops and other system problems
- Real-time interrupt timer
- Power-saving modes:
  - Slow mode reduces power consumption by slowing down internal operations.
  - Wait mode shuts down various system features selected by the user with power consumption typically dropping to 10–100 mW.
  - Stop mode also shuts down system clocks, typically reducing power consumption to about 1.5 mW.
- Package availability for ROM devices:
  - K versions:
    84-pin plastic leaded chip carrier (PLCC)
    80-pin quad flat pack (QFP)
  - KS versions:
    68-pin plastic leaded chip carrier (PLCC)
    80-pin low-profile quad flat pack (LQFP)
- Package availability for EPROM devices:
  - K versions:
    80-pin quad flat pack (QFP)
    84-pin J-cerquad (ceramic windowed version of PLCC)
    84-pin plastic leaded chip carrier (PLCC)
  - KS versions:
    68-pin J-cerquad (ceramic windowed version of PLCC)
    80-pin low-profile quad flat pack (LQFP)
    68-pin plastic leaded chip carrier (PLCC)

Table 4-6. Register Mapping

REG[3:0]	Address
0000	$0000–$007F(1)
0001	$1000–$107F
0010	$2000–$207F
0011	$3000–$307F
0100	$4000–$407F
0101	$5000–$507F
0110	$6000–$607F
0111	$7000–$707F
1000	$8000–$807F
1001	$9000–$907F
1010	$A000–$A07F
1011	$B000–$B07F
1100	$C000–$C07F
1101	$D000–$D07F
1110	$E000–$E07F
1111	$F000–$F07F

1. Default locations out of reset.

Since the direct addressing mode accesses RAM more quickly and efficiently than other addressing modes, many applications will find the default locations of registers and on-board RAM at the bottom of memory to be the most advantageous.

When RAM and the registers are both mapped to different 4-K boundaries, the registers are mapped at $x000–$x07F, and RAM is moved to $x000–$x2FF ($x000–x3FF for the [7]11KS2).

both EELAT and EPGM during the same write operation results in neither bit being set.

4.8.1 EEPROM Registers

This section describes the EEPROM registers:

- Block protect register (BPROT)
- EEPROM programming control register (PPROG)
- System configuration options register (OPTION)

The EEPROM programming control register (PPROG) controls programming and erasing. The block protect register (BPROT) can prevent inadvertent writes to (or erases of) blocks of EEPROM and the CONFIG register. The CSEL bit in the system configuration options register (OPTION) selects an on-chip oscillator clock for programming and erasing when operating at frequencies below 1 MHz.

4.8.1.1 EEPROM Programming Control Register

Address: $003B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	ODD	EVEN	LVPI	BYTE	ROW	ERASE	EELAT	EEPGM
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 4-9. EEPROM Programming Control Register (PPROG)

ODD — Program Odd Rows in Half of EEPROM Bit

This bit is accessible only in test mode.

EVEN — Program Even Rows in Half of EEPROM Bit

This bit is accessible only in test mode.

execution of the illegal opcode, which can lead to stack overflow, the service routine should reinitialize the stack pointer.

5.5.1.3 Software Interrupt (SWI)

SWI cannot be masked by virtue of the fact that it is a software instruction. It is not inhibited by the global mask bits in the CCR. Execution of SWI sets the I mask bit, so other interrupts are inhibited until user software clears the I bit or SWI terminates with an RTI instruction.

5.5.2 Maskable Interrupts

All maskable interrupts are generated by on-chip peripherals, with the exception of the $\overline{\text{IRQ}}$ pin. This input can be connected through a wired-OR network to external devices. When one of these devices pulls $\overline{\text{IRQ}}$ low, a software accessible interrupt flag is set. When enabled, this flag causes a constant request for interrupt service. After the flag is cleared, the service request is released. $\overline{\text{IRQ}}$ is low-level sensitive by default, but can be set for falling-edge sensitivity by the IRQE bit in the OPTION register (see **Figure 5-6**).

Address: $0039

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ADPU	CSEL	IRQE(1)	DLY(1)	CME	FCME(1)	CR1(1)	CR0(1)
Reset:	0	0	0	1	0	0	0	0

1. Can be written only once in first 64 cycles out of reset in normal modes or at any time in special modes

Figure 5-6. System Configuration Options Register (OPTION)

IRQE — Configure IRQ for Edge-Sensitive Operation Bit

This bit can be written only once during the first 64 E-clock cycles after reset in normal modes.

0 = Low-level recognition
1 = Falling-edge recognition

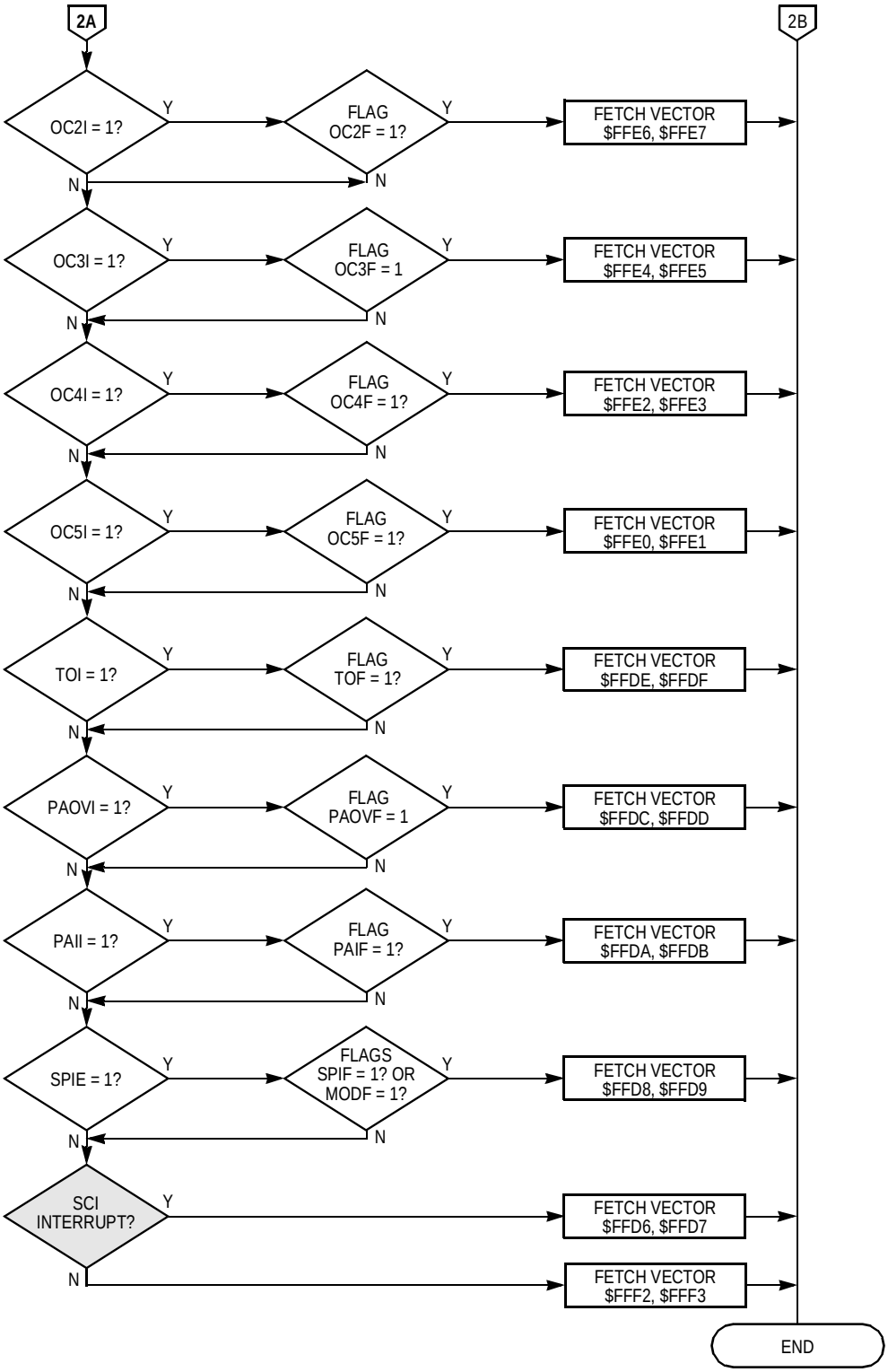


Figure 5-9. Interrupt Priority Resolution (Sheet 2 of 2)

5.8.1 Wait Mode

The WAI opcode places the MCU in the wait condition, during which the CPU registers are stacked and CPU processing is suspended until a qualified interrupt is detected. The interrupt can be an external $\overline{\text{IRQ}}$, an $\overline{\text{XIRQ}}$, or any of the internally generated interrupts, such as the timer or serial interrupts. The on-chip crystal oscillator remains active throughout the wait standby period.

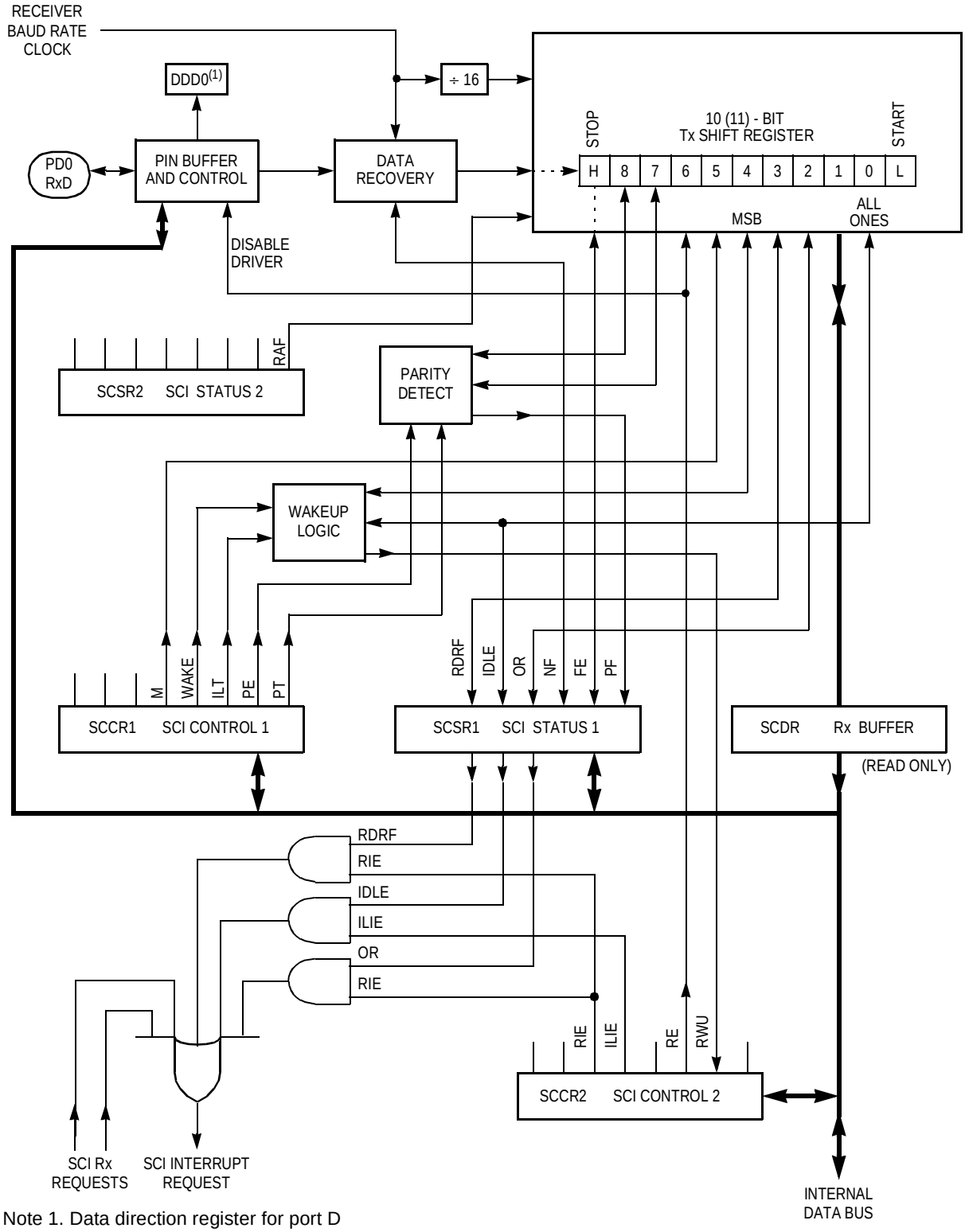
The reduction of power in the wait condition depends on how many internal clock signals driving on-chip peripheral functions can be shut down. The CPU is always shut down during WAIT. While in the wait state, the address/data bus repeatedly runs read cycles to the address where the CCR contents were stacked. The MCU leaves the wait state when it senses any interrupt that has not been masked.

The free-running timer system is shut down only if maskable interrupts are disabled (I bit is set) and the COP system is disabled (NOCOP is set). Other systems can be shut down through the software-controlled configuration control bits, including the SPI system (SPE control bit), the SCI transmitter (TE bit), and the SCI receiver (RE bit). Net power reduction in WAIT depends on which of these features is disabled.

5.8.2 Stop Mode

The STOP instruction halts all system clocks, including the crystal oscillator, thereby minimizing power consumption. The S bit in the CCR must be cleared to place the MCU in the stop condition; otherwise, the stop opcode is treated as a no-operation (NOP). To exit STOP and resume normal processing, a logic low level must be applied to one of the external interrupt pins ($\overline{\text{IRQ}}$ or $\overline{\text{XIRQ}}$) or to the $\overline{\text{RESET}}$ pin. A pending edge-triggered $\overline{\text{IRQ}}$ can also bring the CPU out of stop.

Because all clocks are stopped in this mode, all internal peripheral functions also stop. RAM and register contents are preserved as long as V_{DD} power is maintained. The CPU state and I/O pin levels are static and are not altered by STOP, so the MCU resumes processing seamlessly after the system is reactivated by an interrupt. However, if a reset is used



Note 1. Data direction register for port D

Figure 7-3. SCI Receiver Block Diagram

8.6.4 Port D Data Direction Register

Address: $0009

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
Reset:	0	0	0	0	0	0	0	0

Figure 8-6. Port D Data Direction Register (DDRD)

DDD5 Bit

Bit 5 of the port D data register (PD5) is dedicated as the slave select ($\overline{SS}$) input. In SPI slave mode, DDD5 has no meaning or effect. In SPI master mode, DDD5 affects PD5 as follows:

0 = PD5 is an error-detect input to the SPI.
1 = PD5 is configured as a general-purpose output line.

DDD[4:2] Bits

When the SPI is enabled, SPI input pins remain functioning regardless of the state of the corresponding DDD[4:2] bits. For SPI output pins, however, the corresponding DDD[4:2] bits must be set or the pins will function as general-purpose inputs.

The free-running counter begins incrementing from $0000 as the MCU comes out of reset and continues to the maximum count, $FFFF. At the maximum count, the counter rolls over to $0000, sets the timer overflow flag (TOF) in the timer interrupt flag 2 (TFLG2) register, and continues to increment. The value in this counter can be read in the timer counter (TCNT) register, but cannot be written or changed except by reset.

The pulse accumulator, described in **9.7 Pulse Accumulator (PA)**, derives its clock by post-scaling the main timer so that the output frequency is always E clock divided by 64. This clock drives an 8-bit counter while the pulse accumulator is operating in event counting mode.

RTI is a programmable periodic interrupt circuit that can be used to pace the execution of software routines, as described in **9.8 Real-Time Interrupt (RTI)**. The clock driving this function is also derived from the clock driving the free-running counter. The post-scaler output of this chain runs at a frequency of E clock divided by 2^{13}.

The COP watchdog timer (**5.3.3 Computer Operating Properly (COP) System**) further divides the RTI clock by four to drive its circuitry at a frequency of E clock divided by 2^{15}.

9.4 Input Capture and Output Compare Overview

The M68HC11K series features:

- Three input capture channels
- Four output compare channels
- One channel that can be selected to perform either input capture or output compare

Each of the three input capture functions has its own 16-bit input capture register (time capture latch) and each of the output compare functions has its own 16-bit compare register. All timer functions, including the timer overflow and RTI, have their own interrupt controls and separate interrupt vectors.

9.5.3 Timer Interrupt Flag 1 Register

Address: $0023

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F
Reset:	0	0	0	0	0	0	0	0

Figure 9-10. Timer Interrupt Flag 1 Register (TFLG1)

Clear each flag by writing a 1 to the corresponding bit position.

ICxF — Input Capture x Flag

Set each time a selected active edge is detected on the corresponding input capture line.

I4/O5F — Input Capture 4/Output Compare 5 Flag

Set each time a selected active edge is detected on the IC4 line if IC4 is enabled.

9.5.4 Timer Interrupt Mask 1 Register

Address: $0022

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I
Reset:	0	0	0	0	0	0	0	0

Figure 9-11. Timer Interrupt Mask 1 Register (TMSK1)

Bits in TMSK1 correspond bit for bit with flag bits in TFLG1.

ICxI — Input Capture Interrupt Enable Bit

If the ICxI enable bit is set when the ICxF flag bit is set, a hardware interrupt sequence is requested.

9.7.4 Timer Interrupt Mask 2 Register

Address: $0024

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
Reset:	0	0	0	0	0	0	0	0

Figure 9-25. Timer Interrupt Mask 2 (TMSK2)

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2.

PAOVF — Pulse Accumulator Overflow Flag

The PAOVF status bit is set each time the pulse accumulator count rolls over from $FF to $00.

PAOVI — Interrupt Enable Bit

If PAOVI is set, an interrupt request is also generated. If PAOVI is cleared, pulse accumulator overflow interrupts are inhibited, and PAOVF must be polled by user software to determine when an overflow has occurred. In either case, software must clear PAOVF by writing a 1 to bit 5 in the TFLG2 register.

PAIF — Pulse Accumulator Input Edge Flag

The PAIF status bit is automatically set each time a selected edge is detected at the PA7 pin.

PAII — Interrupt Enable Bit

If PAII is set, an interrupt request is also generated. If PAII is cleared, pulse accumulator input interrupts are inhibited, and PAIF must be polled by user software to determine when an input edge has been detected. In either case, software must clear PAIF by writing a 1 to bit 5 in the TFLG2 register.

CCF — Conversions Complete Flag

Set when all four A/D result registers contain valid conversion results. Cleared when the ADCTL register is overwritten, starting a new conversion sequence. In continuous mode, CCF is set at the end of the first conversion sequence.

SCAN — Continuous Scan Control Bit

0 = Conversion process stops after each of the four result registers is written.
1 = Conversions are performed continuously.

MULT — Multiple Channel/Single Channel Control Bit

0 = A single channel specified by the four channel select bits CD:CA is sampled and converted four times.
1 = Each of four channels is converted and the results written to a different result register.

NOTE: *When the multiple-channel continuous scan mode is used, extra care is needed in the design of circuitry driving the A/D inputs. The charge on the capacitive DAC array before the sample time is related to the voltage on the previously converted channel. A charge share situation exists between the internal DAC capacitance and the external circuit capacitance. Although the amount of charge involved is small, the rate at which it is repeated is every 64 µs for an E clock of 2 MHz. The RC charging rate of the external circuit must be balanced against this charge sharing effect to avoid errors in accuracy. Refer to the M68HC11 Reference Manual, Motorola document order number M68HC11RM/AD, for further information.*

CD:CA — Channel Selects D:A Bits

Refer to **Table 10-1**. In multiple channel mode (MULT = 1), the two least significant channel select bits (CB and CA) have no meaning and the CD and CC bits specify which group of four channels is to be converted.

11.4.1 Program Chip Select

The program chip select signal accesses external memory in the main program area within the MCU's 64-Kbyte memory map. Program chip select validity is fixed at address valid timing and polarity is fixed at active low. The chip-select control register (CSCTL) contains bits to enable $\overline{\text{CSPROG}}$, determine its priority over the general-purpose chip selects, and set its effective address range. Clock stretching can be set from zero to three cycles.

Address: $005B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	IOEN	IOPL	IOCSA	IOSZ	GCSPR	PCSEN	PCSZA	PCSZB
Reset:	0	0	0	0	0	1	0	0

Figure 11-5. Chip-Select Control Register (CSCTL)

GCSPR — General-Purpose Chip Select Priority Bit

0 = Program chip select has priority over general-purpose chip selects

1 = General-purpose chip selects have priority over program chip select

PCSEN — Program Chip Select Enable Bit

0 = CSPROG disabled and port H bit 7 available as GPIO

1 = CSPROG enabled out of reset and uses port H bit 7 pin

PCSZA and PCSZB — Program Chip Select Size A Bit and Program Chip Select Size B Bit

These bits determine the address range of $\overline{\text{CSPROG}}$, as shown in **Table 11-5**.

Table 11-5. Program Chip Select Size

PCSZA	PCSZB	Size (Bytes)	Address Range
0	0	64 K	$0000–$FFFF
0	1	32 K	$8000–$FFFF
1	0	16 K	$C000–$FFFF
1	1	8 K	$E000–$FFFF

12.10 Analog-to-Digital Converter Characteristics

Characteristic[1]	Parameter	Min	Absolute	Max		Unit
				$f_o \leq 2.0$ MHz	$f_o > 2.0$ MHz[2]	
Resolution	Number of bits resolved by A/D converter	—	8	—	—	Bits
Non-linearity	Maximum deviation from the ideal A/D transfer characteristics	—	—	± 1/2	± 1	LSB
Zero error	Difference between the output of an ideal and an actual for zero input voltage	—	—	± 1/2	± 1	LSB
Full scale error	Difference between the output of an ideal and an actual A/D for full-scale input voltage	—	—	± 1/2	± 1	LSB
Total unadjusted error	Maximum sum of non-linearity, zero error, and full-scale error[3]	—	—	± 1/2	± 1 1/2	LSB
Quantization error	Uncertainty because of converter resolution	—	—	± 1/2	± 1/2	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	—	—	± 1	± 2	LSB
Conversion range	Analog input voltage range	V_{RL}	—	V_{RH}	V_{RH}	V
V_{RH}	Maximum analog reference voltage[3]	V_{RL}	—	V_{DD} + 0.1	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage[3]	V_{SS} –0.1	—	V_{RH}	V_{RH}	V
ΔV_R	Minimum difference between V_{RH} and V_{RL}[3]	3	—	—	—	V
Conversion time	Total time to perform a single analog-to-digital conversion: E clock Internal RC oscillator	— —	32 —	— t_{cyc} + 32	— t_{cyc} + 32	t_{cyc} µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes		Guaranteed			
Zero Input reading	Conversion result when $V_{In} = V_{RL}$	00	—	—	—	Hex
Full Scale reading	Conversion result when $V_{In} = V_{RH}$	—	—	FF	FF	Hex

Continued

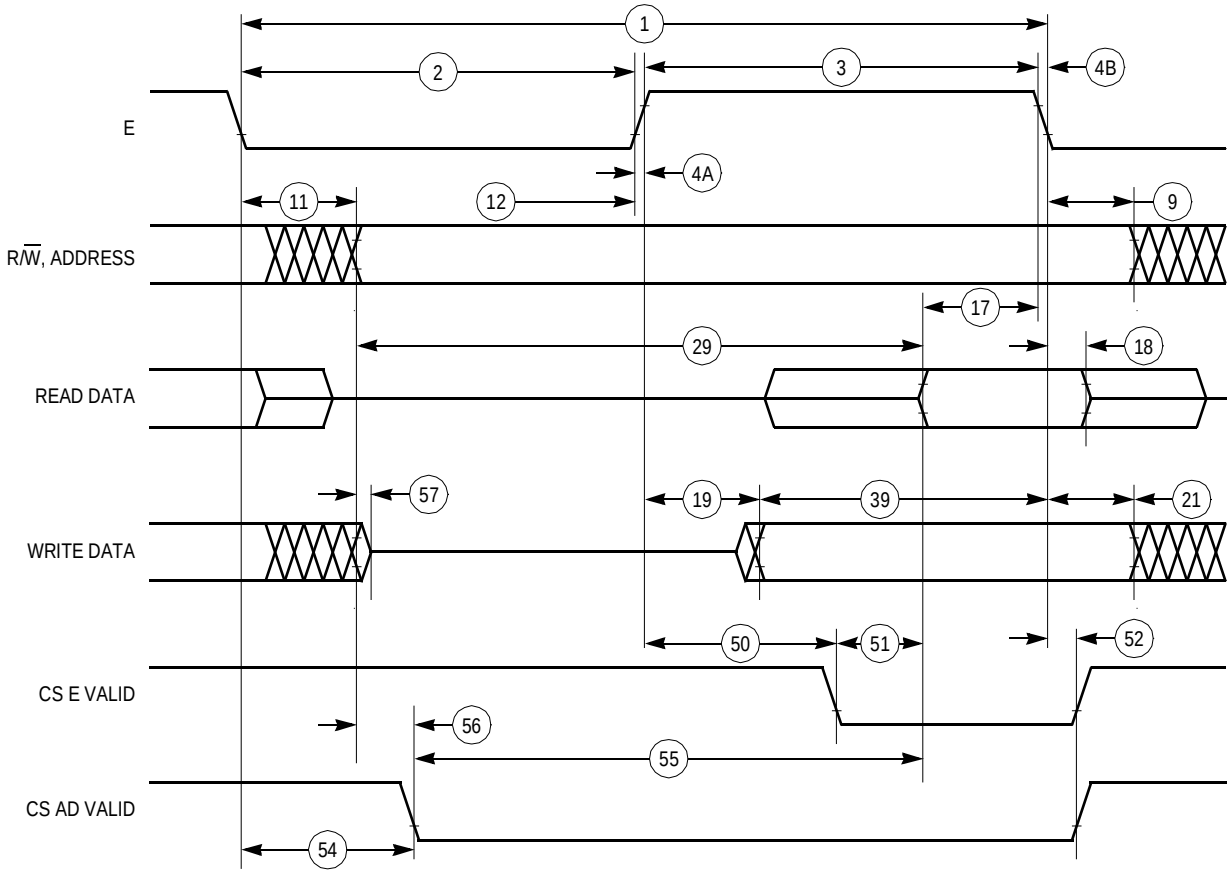


Figure 12-9. Expansion Bus Timing

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